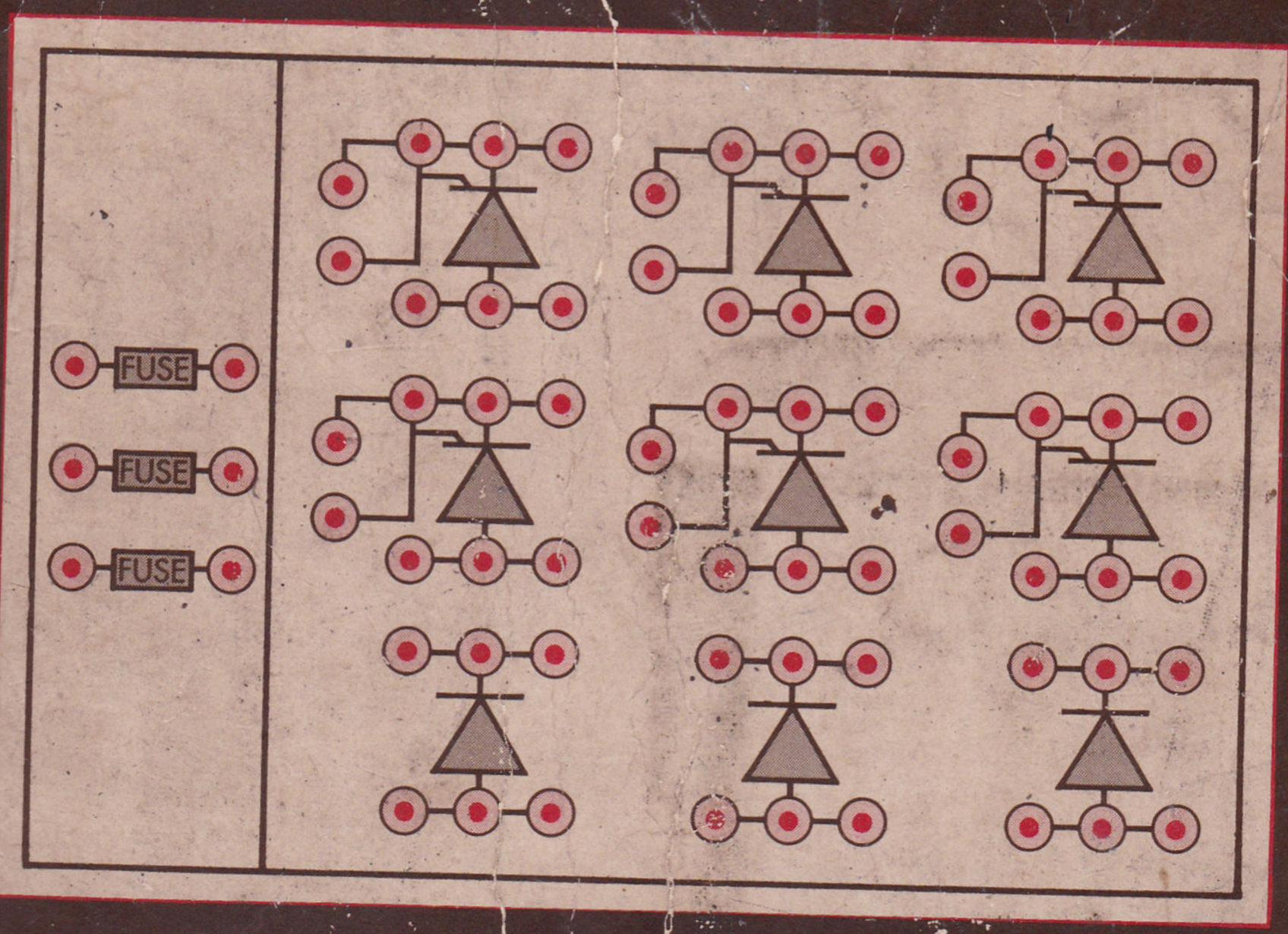
POWER ELECTRONICS LABORATORY

EXPERIMENTS AND ORGANIZATION

Thyristors • Transistors • GTOs • MOSFETs



O P ARORA

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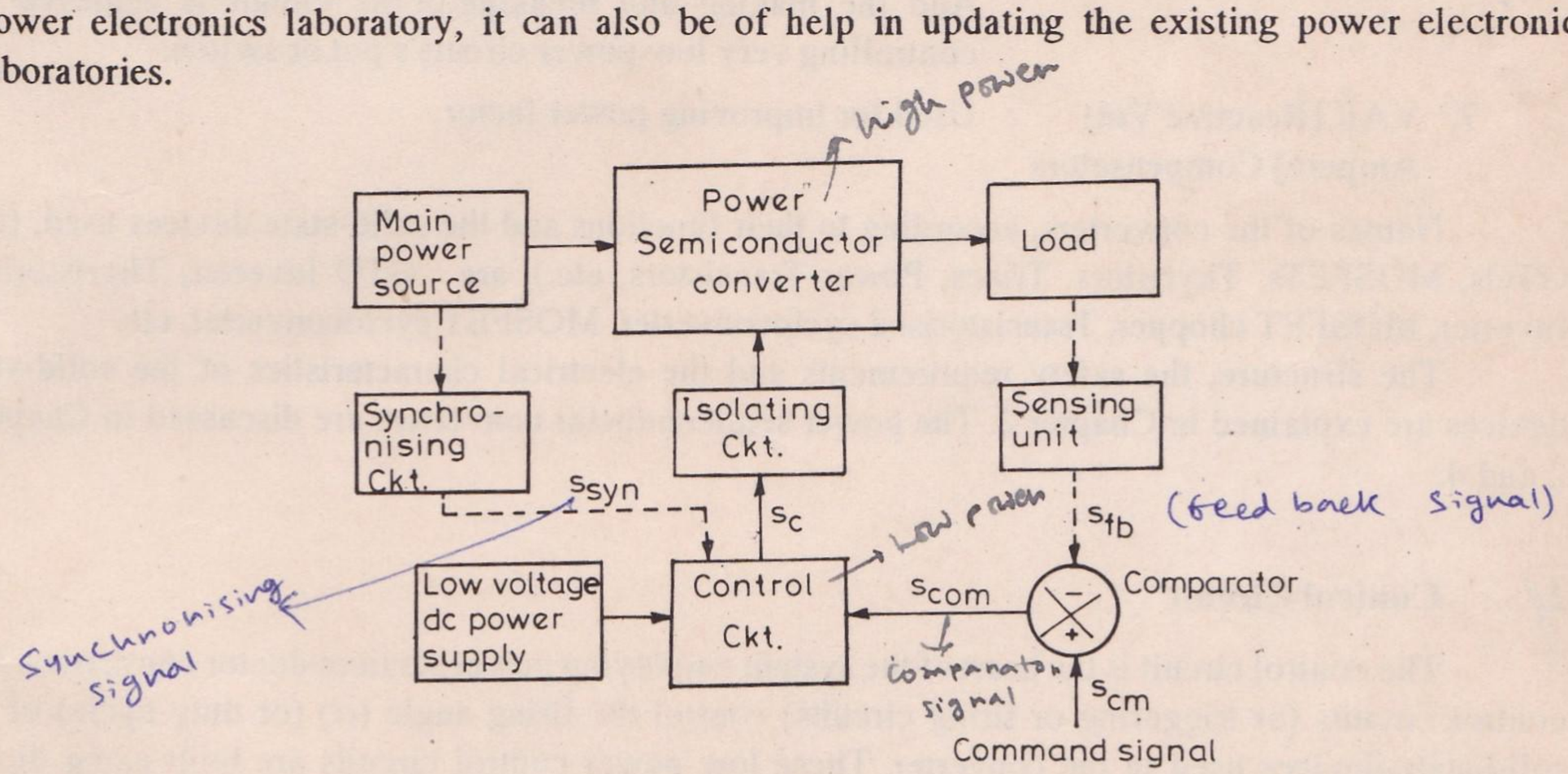
1

INTRODUCTION

The power semiconductor converters are now being very widely used because of the advantages, such as high efficiency, long life, low maintenance, compact size and low power consumption of their control circuits. In recent years power electronics has become an integral part of μG and PG course in electrical and electronic engineering.

Although, power electronics is taught in almost all the engineering colleges and polytechnics, very few colleges can, however, boast of having a modern and well-developed power electronics laboratory. This book offers practical suggestions for the organisation and development of Power Electronics Laboratory and for conducting the experiments. While it will be useful in setting up a power electronics laboratory, it can also be of help in updating the existing power electronics laboratories.



FIG·1·1: BLOCK DIAGRAM OF A SYSTEM EMPLOYING A POWER SEMICONDUCTOR CONVERTER

Fig. 1.1 shows the block diagram of a system employing semiconductor converter. The controlled power flows from main (ac/dc) power source to a load (*R*-load, *R-L* load or ac/dc-motor

load) through a power semiconductor converter. And the on-off duration (duty-cycle) of the solid-state devices, used in the power semiconductor converter, are controlled by the control (also called firing or triggering) circuit.

The signals shown by broken lines (----) are synchronising and feedback signals. The power supplies and loading arrangements of the system employing semiconductor converter are discussed in Chapter 3. The function and construction of different blocks of Fig. 1.1 are the following :

1. Power Semiconductor Converters

The power semiconductor converters are classified according to their functions and the solid state devices used. Names of the converters, according to their functions, are :

1. Ac Regulators : Convert a fixed ac voltage to a variable ac voltage, without change in the frequency
2. Choppers : Convert a fixed dc voltage into a variable dc voltage.
3. Line Commutated Converters (or Rectifiers) : Convert a fixed ac voltage to a variable/fixed dc voltage
4. Inverters : Convert a fixed dc voltage into a variable/fixed ac voltage of fixed/variable frequency.
5. Cycloconverters : Convert a fixed frequency ac voltage into a variable frequency ac voltage.
6. Static Circuit Breakers : Used for sparkless making and breaking of high current circuits. And the making and breaking of the circuit is achieved by controlling very low power circuit's pot or switch.
7. VAR (Reactive Volt Ampere) Compensators : Used for improving power factor.

Names of the converters, according to their functions and the solid-state devices used, (i.e., GTOs, MOSFETs, Thyristors, Triacs, Power Transistors, etc.), are : GTO Inverter, Thyristorised Inverter, MOSFET chopper, Transistorised cycloconverter, MOSFET cycloconverter, etc.

The structure, the safety requirements and the electrical characteristics of the solid-state devices are explained in Chapter 2. The power semiconductor converters are discussed in Chapters 2 and 4.

2. Control Circuit

The control circuit is the heart of the system employing power semiconductor converters. The control circuits (or triggering or firing circuits) control the firing angle (α) (or duty cycle) of the solid-state-devices used in the converter. These low power control circuits are built using digital circuits, analog circuits, microcomputers (microprocessor, personnel computer), etc. Therefore, the basic knowledge of the electronics is necessary for designing the control circuit of converters. Some commonly used electronic components and their circuits are given in Appendices 3 and 4, respectively.

The control signal (output signal (S_c) of the control circuit) is controlled by the command signal, feedback signal (S_{fb}) and synchronising signal (S_{syn}). In some power converter circuits, the

synchronising circuit and/or sensing circuit (feedback circuit) are not required. For example, the synchronising signal is not required in chopper circuit.

The control signals may be modulated by high frequency pulses ($\simeq$ 10 Khz) at the last stage, but just before the pulse-amplifier circuits of the firing circuits of thyristorised converters. The high frequency switching is essential to reduce the gate power dissipation of the solid-state devices and the size of pulse transformers.

The pulse amplifier circuits are required at the output stage of the control circuit because generally, the output of the *IC*s (integrated circuits) cannot trigger the solid-state-devices of converters due to their low power.

3. Isolating Circuit

The low power and low voltage control circuit is electrically isolated from the high power circuit (or power semiconductor converter circuit) for the safety of control circuit and the operator of the command signal. The following three types of driver circuits, with isolation from power circuit, are commonly used :

1. Pulse-Transformer and Transistor driver circuit
2. MOSFET driver circuit
3. Optocoupler driver circuit.

Pulse-transformer and transistor driver circuit can be handled more easily and are more reliable. The isolated driver circuits of the power semiconductor converters are explained with circuit diagrams in Experiment 3.1 of Chapter 4.

4. Synchronising Circuit

Generally, the low voltage (> 3*V* but < 12 *V*) output potential-transformer is used for getting synchronising signal and for providing the isolation between main power source and control circuit. The low voltage of the potential-transformer is fed to the ZCD (zero-crossing-detector) or rectifier. The control circuit is designed in such a way that the control signal (S_c) can be obtained at fixed firing angle or triggering angle from the zero-cross-over point of the synchronising signal.

5. Sensing Unit

The sensing unit is used in closed loop operation or for monitoring and protecting the system. The sensing devices convert the magnitude of a physical quantity or the condition of load into an electrical signal which is proportional to the magnitude of the physical quantity or dependent of load condition. The sensing devices, sense certain parameters (such as current, voltage, speed, displacement, temperature, intensity of the illumination, etc.), of the load and/or of the power converter. The low power and voltage output signal (S_{fb}) of the sensing unit is compared with the command signal (S_{cm}) in the comparator unit as shown in Fig. 1.1. And the output signal (S_{com}) of the comparator controls the action of the control circuit. For the safety of the sensing unit and the control circuit, the isolation is required between the sensing unit and power circuit (converter and load).

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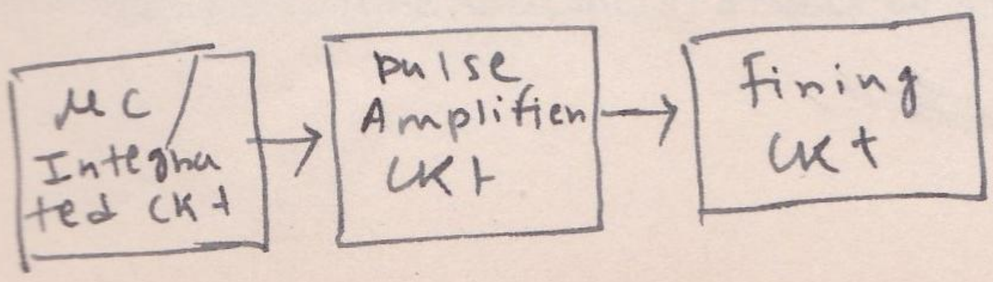


2

INTRODUCTION TO POWER ELECTRONICS

2.1 SEMICONDUCTOR DEVICES

Now-a-days, Solid State Devices such as Power Transistors, Thyristors, Triacs, GTO-Thyristors, Power MOSFETs are commonly used in Power Controllers. A photograph of some of the Power Semiconductor Devices is shown in Fig. 2.1 (a). The operation and characteristics of these devices are briefly described here.

2.1.1 Power Transistors

The power transistors are available upto the rating of 120*V*, 750*A* and 1000*V*, 60*A*. Transistor is a bipolar solid-state current controlled device. Depending on their structure, transistors are classified as NPN and PNP transistors. A transistor has three terminals: emitter, base and collector. Generally, NPN transistors are used, so here only NPN transistor will be discussed. Fig. 2.1(b) shows the structure and electric symbol of a power NPN transistor. Power transistors are used as switches and the on-state voltage drop is of the order of 1.0 volt.

2.1.1.1 *Collector Characteristic Curves*

Fig. 2.2 shows circuit diagram and collector characteristics (I_C– V_{CE}) characteristics with I_B as a parameter) of a NPN transistor with common emitter configuration.

The PNP transistor has similar characteristics with reversed direction of current and voltage, as shown in Fig. 2.2 (b).

$I_C \propto I_B$

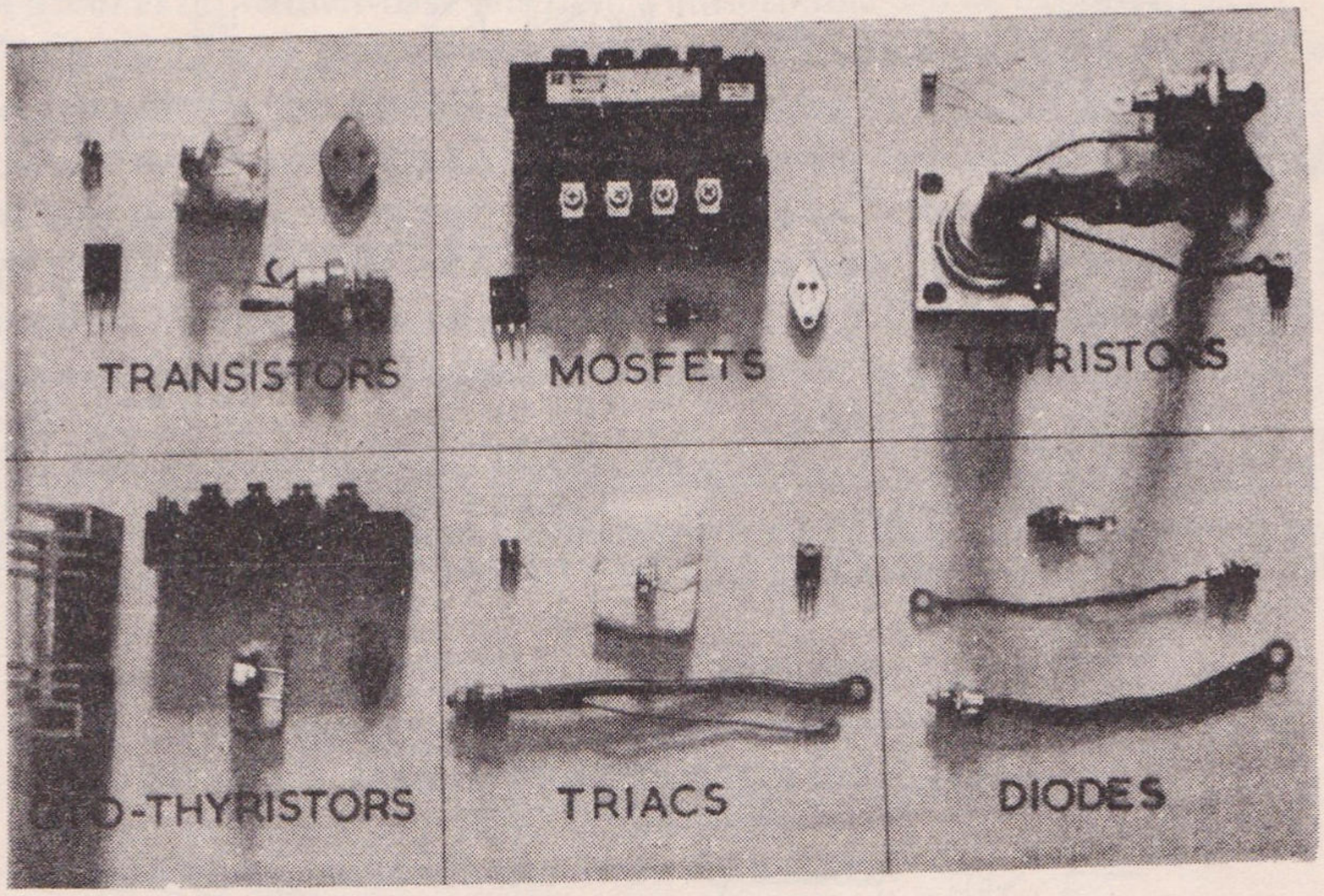
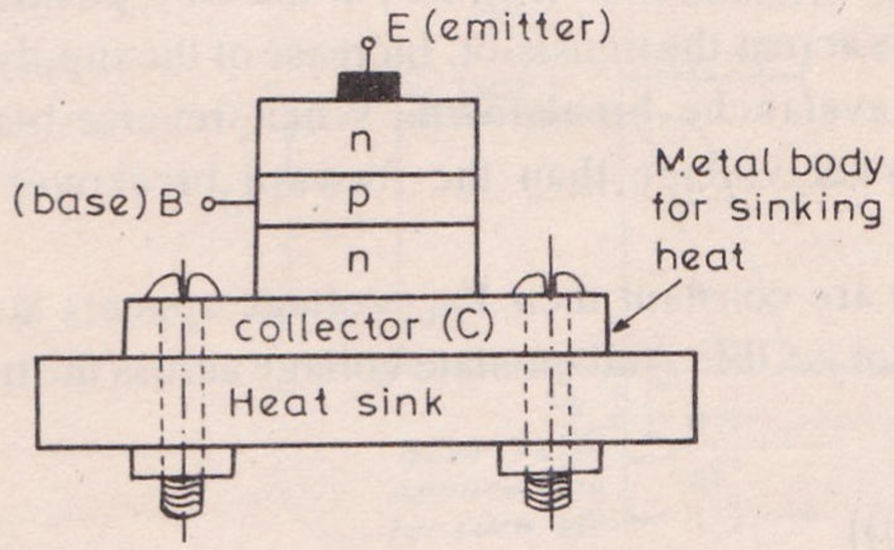
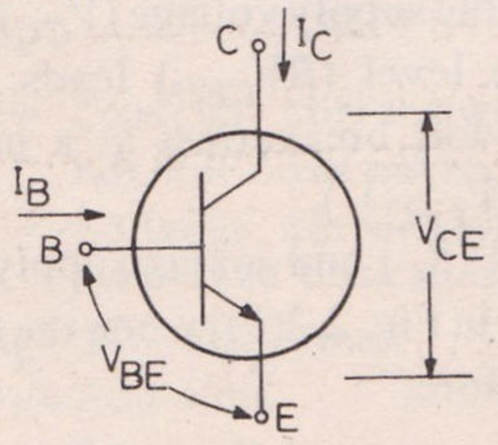


FIG. 2-1(a) : PHOTO ILLUSTRATING SOME POWER SEMICONDUCTOR DEVICES

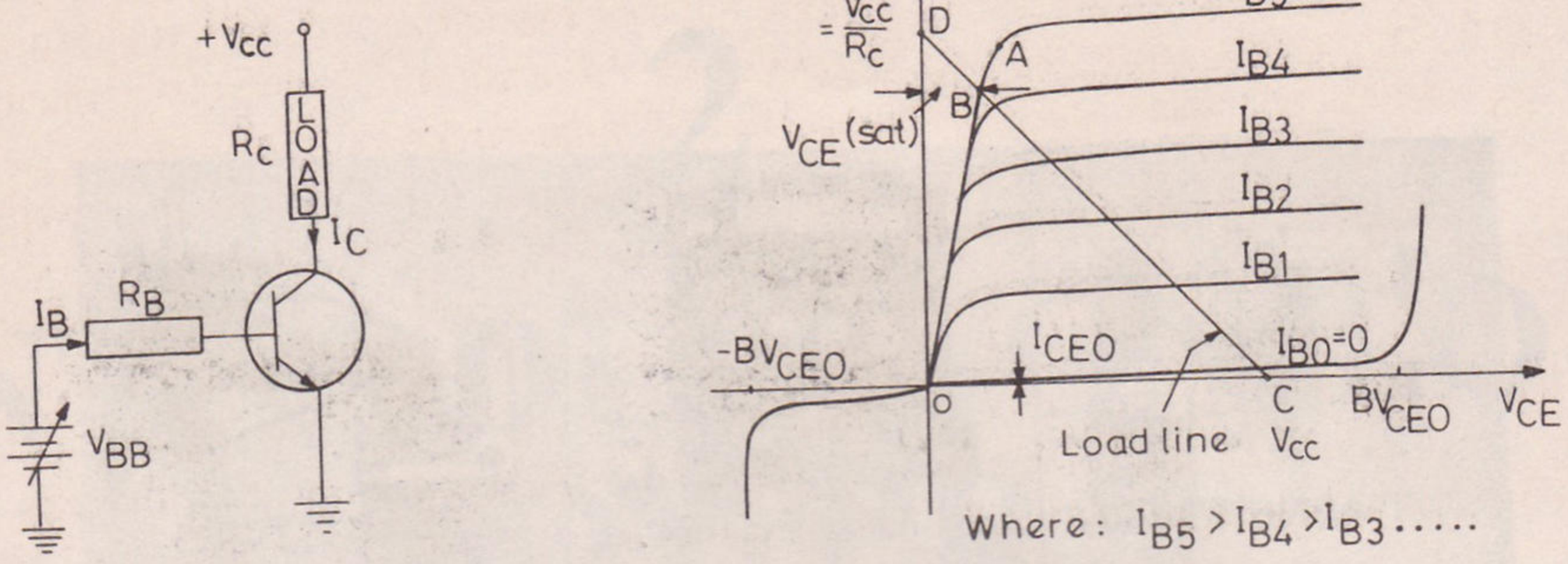


(a) STRUCTURE



(b) CIRCUIT SYMBOL

FIG. 2-1(b) : STRUCTURE AND CIRCUIT SYMBOL OF AN NPN POWER TRANSISTOR



(a) CIRCUIT DIAGRAM

(b) COLLECTOR CHARACTERISTICS CURVES WITH LOAD LINE

FIG. 2·2 CIRCUIT AND COLLECTOR CHARACTERISTICS CURVES

WHERE:

BV_{CEO} = COMMON EMITTER OPEN BASE, COLLECTOR FORWARD BREAKOVER VOLTAGE.

$-BV_{CEO}$ = COMMON EMITTER OPEN BASE, COLLECTOR REVERSE BREAKOVER VOLTAGE.

I_{CEO} = COLLECTOR LEAKAGE CURRENT OF COMMON EMITTER CONFIGURATION FOR OPEN BASE

(2.1)

or $I_C = \beta I_B$

where β = current gain of a transistor.

The current gains (β) of the power transistors are typically 10 to 20. The curve OBA in Fig. 2.2(*b*) is called Saturation Curve and its right side region is called Active-Region. During the conduction period the power transistor must be operated in the saturation region (curve OBA), so that the on-state voltage drop across the transistor is small.

A leakage current (I_{CEO}) flows without the Base current (I_B), i.e., in the OFF position of the transistor. The whole supply voltage (V_{CC}) appears across the transistor. Increase of the supply voltage beyond a certain level (BV_{CEO}) leads to an avalanche breakdown. When reverse-biased the collector-emitter will breakdown at a much lower voltage than the forward breakover voltage ($|BV_{CEO}| > |-BV_{CEO}|$).

If the load (R_C) and mains supply (V_{CC}) are constant then V_{CC} voltage appears across the transistor [point C in Fig. 2.2(*b*)] when the transistor is OFF. And on-state voltage across the transistor is V_{CE} (sat), therefore,

$$I_C = \frac{V_{CC}}{R_C}$$ ['*D*' point shown in Fig. 2.2(b)]

CD line is called Load Line, and it cuts the saturation curve (OBA) at point *B*. The power transistor in the Power Electronic Controller, is operated as a Controlled Switch, so the base current (I_B) must be either zero (I_{BO}) for off-state or within I_{B4} and I_{B5} for on-state.

2.1.1.2 *Commutation Process*

The transistor is turned-off by making the base current zero (I_B=0), it's turn-off time can be reduced by applying a largest possible negative base drive but taking care that avalanche breakdown does not occur at the emitter-base junction. Turn-off time can be expressed as :

Turn-off time (t_{off}) = Storage-time (t_s) + Fall-time (t_f). Turn-off time, with and without negative gate pulse in the turn-off period, is illustrated in Fig. 2.3. When in the on-state, the base current should be just enough to keep it under saturation, because the large number of extra carriers flood the base region in the heavily saturated transistor. After the base voltage is switched off, the transistor remains unchanged until all extra carriers leave the base region. Time delay due to this reason is called storage-time or saturation-delay time (t_s). But a negative base drive in the off-period (t_{off}) reduces the storage-time because it sweeps out the minority carrier from the base as shown in Fig. 2.3(d).

Transistorised Power Controller can be operated at higher frequency than thyristorised power controller because switching times of transistors are less than 2 microseconds (μsec).

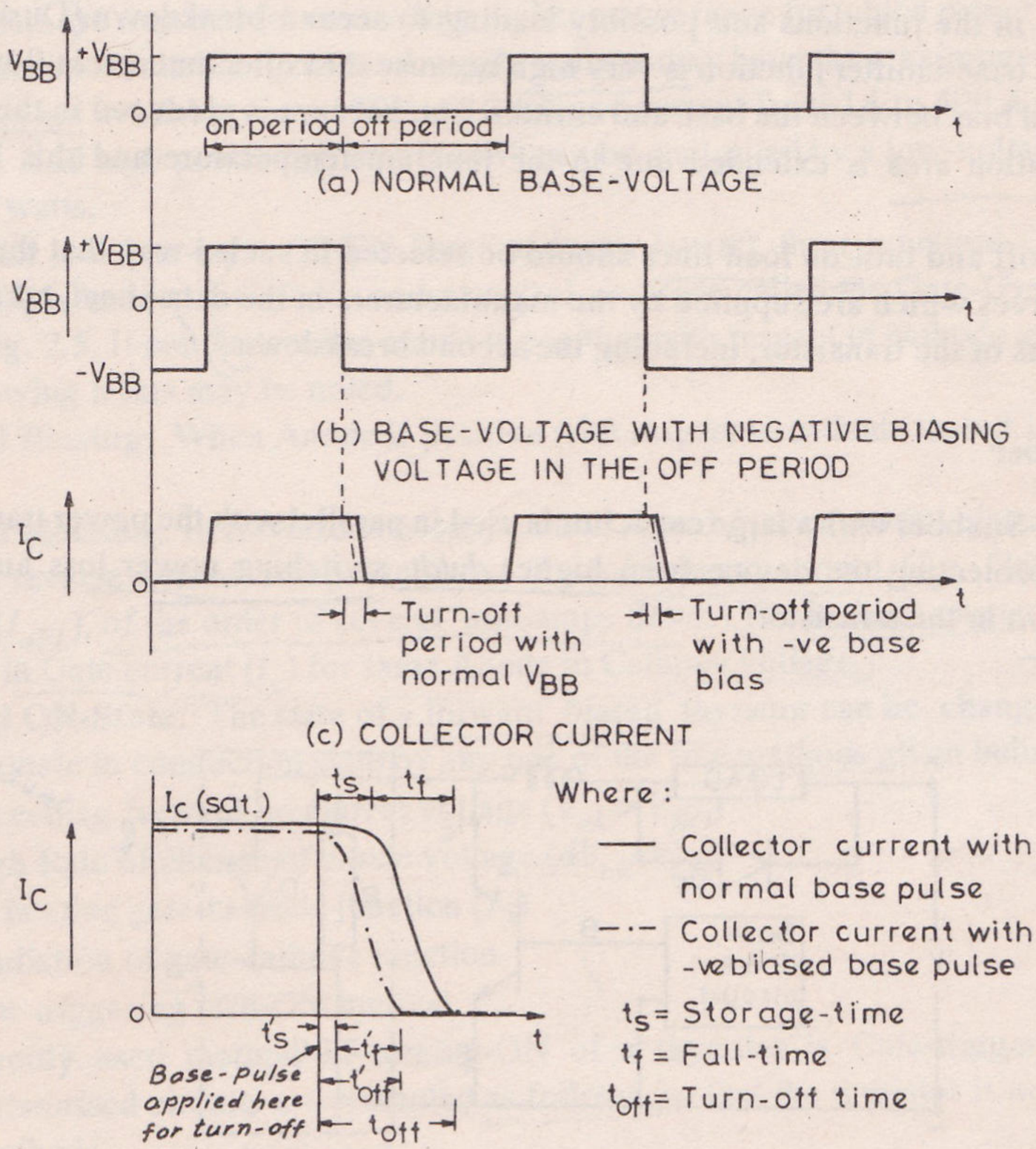


FIG. 2-3: TURN-OFF PROCESS OF A POWER TRANSISTOR WITH AND WITHOUT NEGATIVE BASE-PULSE

2.1.1.3 *Protection of a Power Transistor*

As shown in Fig. 2.1(a), Power-Transistors are mounted on the Heat-Sink which removes the heat from the body of transistors, so that their temperature remains below the permissible value and junctions are not damaged due to high temperature. Generally, aluminium is used for making the Heat-Sink. Sometimes aluminium tubes are also attached with Heat-Sink for flowing water or oil through them and/or fans for cooling the Heat-Sink. Polarised-Snubber circuit is connected across the transistor for controlling power loss, dV/dt and second breakdown in the transistor during the device switching period.

Second Breakdown

The Second Breakdown in the transistor can be caused by the localised heating effects during switching period (turn-on and turn-off). This second breakdown in the transistor is different from the avalanche breakdown (i.e., first breakdown). During turn-on, if inductor (L) in series of transistor is absent, the rate of the change of the collector current (dI_C/dt) is very high. And it produces high temperature in the junctions and possibly leading to second breakdown. During turn-off, the current density in base-emitter junction is very high because the collector current flows in small area due to the forward bias between the base and emitter. The hot spot is produced in this small area and current concentration area is extended due to the junction temperature and this leads to second breakdown.

The turn-off and turn-on load lines should be selected in such a way that they lie within the specified area curves which are supplied by the manufacturers in the data-sheet, taking into account various limitations of the transistor, including the second breakdown.

Polarised-Snubber

Polarised-Snubber with a large capacitor is used in parallel with the power transistor as shown in Fig. 2.4, for protecting the device from higher dv/dt, switching power loss and also to avoid second-breakdown in the transistor.

R = Snubber Resistance

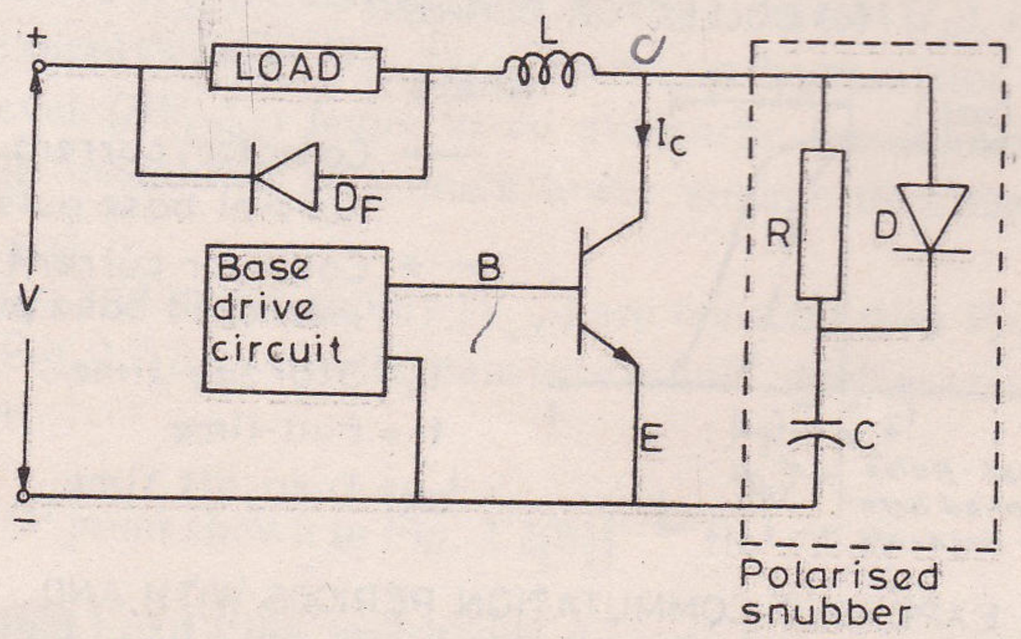


FIG. 2·4: POWER TRANSISTOR CHOPPER CIRCUIT WITH POLARISED-SNUBBER

Let the transistor be off, and the capacitor (C) be charged through Load, and inductor (L) of about 2μH and Diode (D) upto the supply voltage (V). When the base drive pulse is applied, the load current is gradually increased due to pressure of Inductor (L) and the transistor works under prescribed di/dt rating, which avoids second breakdown. If the source has enough inductance, then external inductance (L) can be omitted. The snubber capacitor C will be discharged through the transistor and the snubber resistance (R) in the on-state of the transistor. And the energy stored in the capacitor is wasted mainly in the resistor (R). When turn-off state of the transistor is required, a negative base drive is applied. The load current is transferred from the transistor to the snubber circuit and the collector emitter voltage (V_{CE}) increases slowly, at the charging rate of the capacitor (dV_c/dt), which depends on the value of the capacitor and the load. The capacitor will be charged to the supply voltage (V) after a small overshoot, the load current will flow through Free-Wheeling diode D_F. In the absence of the snubber circuit, V_{CE} will increase when I_C just begins to fall. So with high V_{CE} and high I_C existing simultaneously, the transistor can either be damaged permanently or can be turned-on again due to the high power dissipation in the transistor due to second breakdown.

2.1.2 Thyristor (SCR : Silicon Controlled Rectifier) and its Characteristics

Thyristors are required for controlling higher power range for which power transistors are not available. A transistor suitable for normal supply voltage may have the maximum rating of 10A and 1KV. Thyristors are available from 100V to 10 KV and current from 1A to 500 A (maximum power rating 5 MWs). And high power thyristor (5MW) can be controlled by a low-voltage supply ($\approx 12V$) of 1A and few watts.

Thyristor is a four-layer (PNPN Semiconductor layers), three junctions (J_1, J_2 and J_3) and three terminals (A-Anode, K-Cathode and a control electrode called the Gate-G) solid-state device, as shown in Fig. 2.5. It conducts when anode is positive with respect to cathode and gate is forward bias. The following terms may be noted.

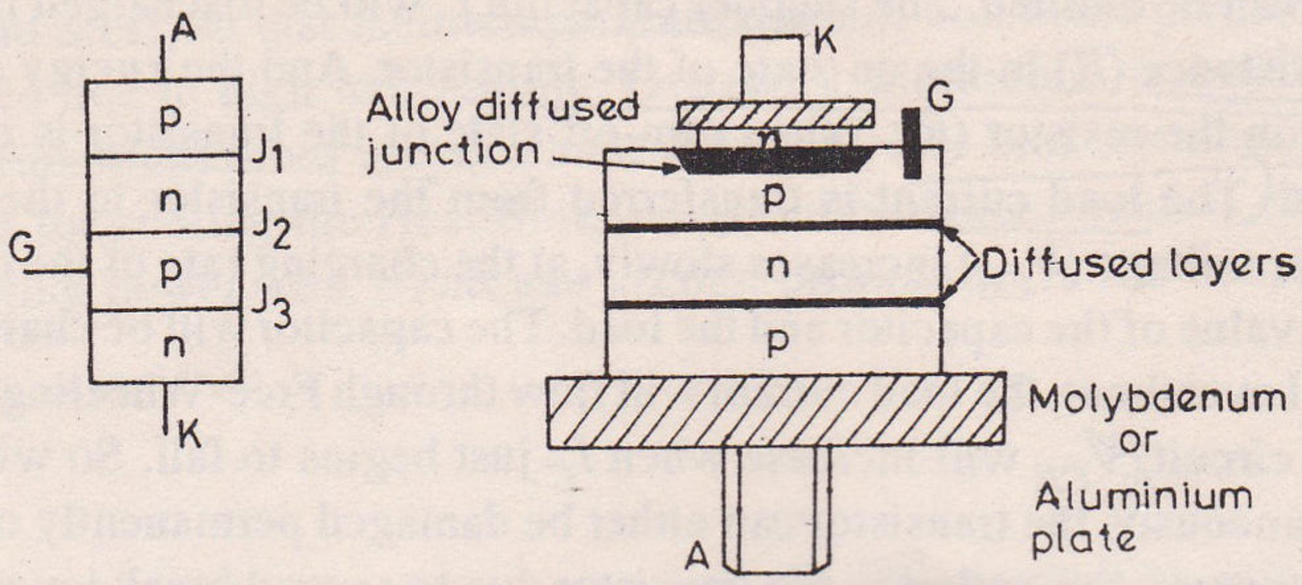
1. **Forward Biasing**: When Anode is positive with respect to cathode then it is called forward biasing.
2. **Forward blocking**: In forward biasing, junction J_1 and J_3 are forward biased. However, junction J_2 is reverse biased and prevents the flow of forward current (I_a). Only a small leakage current (I_{aFL}), of the order of several milliamps flows. The leakage current increases with an increase in Gate current (I_g) for same Anode to Cathode voltage.
3. **Forward ON-State**: The state of a forward biased thyristor can be changed from forward blocking state to conduction state by any one of the five methods given below :
   (i) Exceeding forward breakover voltage ($V_{ak} > V_{BO}$)
   (ii) High Rate of change of anode voltage (dV_{ak}/dt)
   (iii) By heating gate-cathode junction (J_3)
   (iv) Irradiation of gate-cathode junction
   (v) Gate triggering turn-ON method.

Commonly used method of turning-ON of a thyristor is Gate-triggering method. And generally, thyristorised circuits are protected as follows, so that the thyristor is not switched on due to first four methods.

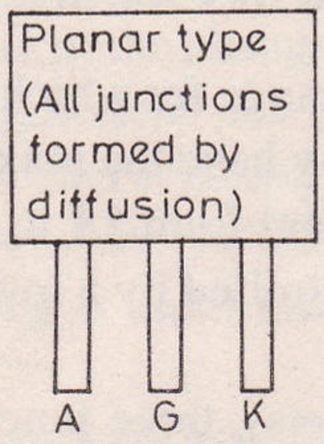
(i) Applied voltage across the thyristor (Anode to Cathode) must be less than forward breakover voltage.

(ii) Heat-Sinks are used for removing the heat produced by the power losses in the thyristor, so as to limit the temperature of thyristor junctions within the permissible limit.

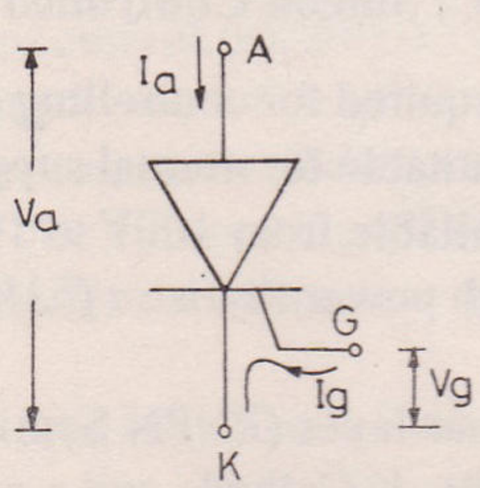
(iii) Snubber circuit is connected between the Anode and Cathode terminals of the thyristor for avoiding *dV/dt* turn-on of thyristor.



(a) BASIC STRUCTURE (b) MESA TYPE THYRISTOR



(Terminals are specified by manufacturer)



(c) PLANAR TYPE THYRISTOR (d) CIRCUIT SYMBOL OF THYRISTOR

FIG. 2·5: STRUCTURE CONSTRUCTIONS AND CIRCUIT SYMBOL OF A THYRISTOR

2.1.2.1 *Gate-Triggering Methods of Thyristor*

Three conditions should be met for turning-ON a thyristor by gate-triggering method :

(i) $V_{amin} \leq V_a < V_{BO}$

Thyristor must be forward biased and anode to cathode voltage must be greater or equal than V_{amin} (minimum anode to cathode voltage, specified by Data-Sheet) and less than forward breakover voltage.

(ii) $V_{gmin} \leq V_g < V_{gmax}$ (positive bias)

Gate-cathode junction must be forward biased and Gate to cathode voltage (V_g) must be higher than V_{gmin} and less than V_{gmax}, which are specified in Data-Sheet.

(iii) $I_{gmin} \leq I_g < I_{gmax}$

If Gate Voltage (V_g) is higher than V_{gmax} and/or Gate-current (I_g) is higher than I_{gmax}, then Gate-Cathode junction (J_3) may be damaged.

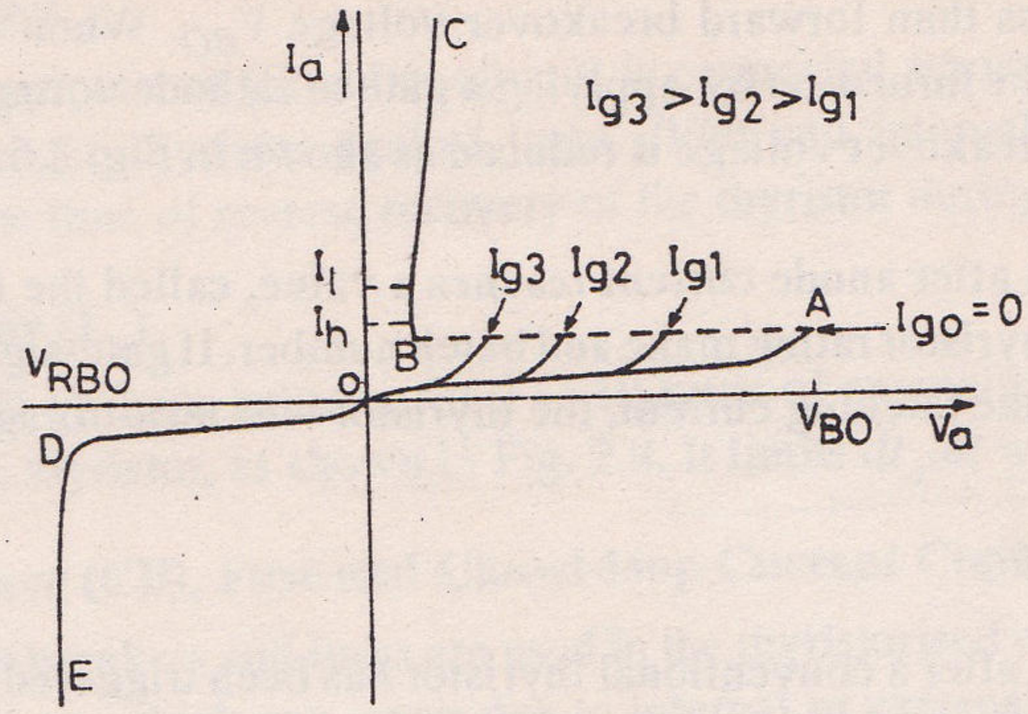


FIG. 2·6: THYRISTOR'S V-I CHARACTERISTICS

Where:

Curve OA → Forward blocking leakage anode current (I_{aFL}) When Ig=0

Curve OD → Reverse blocking leakage annode current

V_{BO} → Forward breakover voltage

V_{RBO} → Reverse breakover voltage

I_h → Holding current of the device

I_l → Latching current of the device

Ig → Gate current

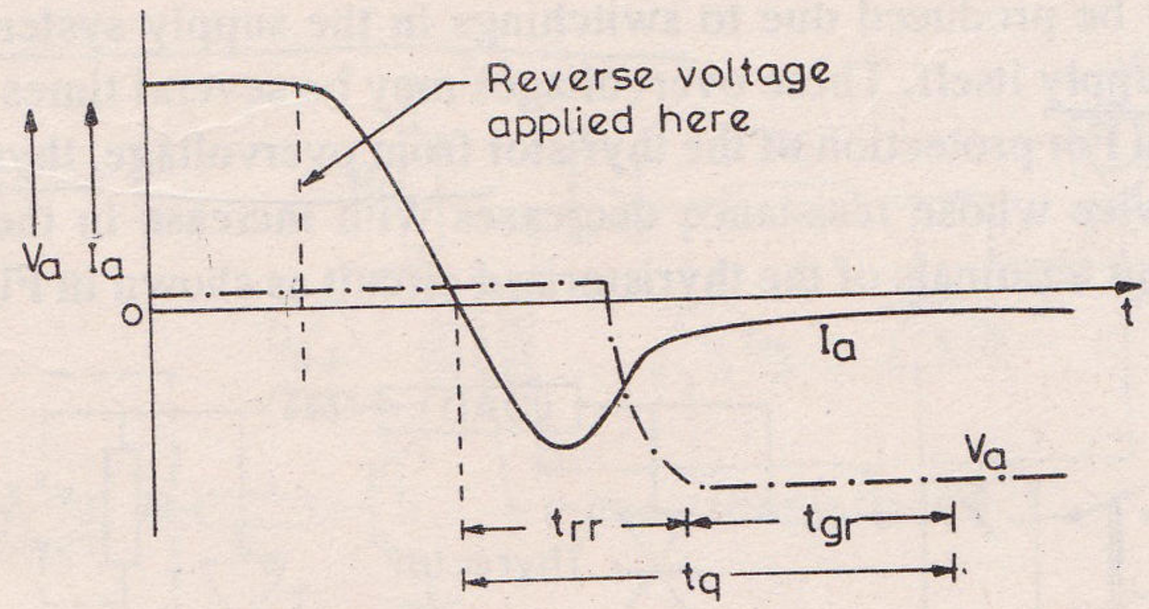


FIG. 2·7: THYRISTOR TURN-OFF CHARACTERISTICS

Where:

t_{rr} → Reverse recovery time

tgr → Gate recovery time

tq → Turn of time

In the absence of the gate-current I_g, the thyristor remains in the forward blocking state if applied voltage across it is less than forward breakover voltage V_{BO}. When the thyristor is in the forward blocking mode, it can be turned-on by applying a gate to cathode voltage (V_g). By increasing the gate-current, the forward breakover voltage is reduced as shown in Fig. 2.6. (V-I characteristic of the thyristor).

Gate looses the control after anode current reaches a value, called the Latching Current (I_l), which varies according to the thyristor rating make and batch number. If gate-signal is removed before the anode current (I_a) reaches the latching current, the thyristor will turn-off again.

2.1.2.2 *Turn-off Characteristics*

The gate has no control after a conventional thyristor has been triggered into conduction. The device can be brought back to the blocking mode either by reducing the forward anode current (I_a) below its *Holding Current* (I_h) level or by applying a reverse voltage across it for the period which is not less than the turn-off-time of the thyristor (t_q, specified in data sheet of thyristor). Note that when the thyristor is reverse-biased, no positive gate signal should be applied. The turn-off process of a thyristor is also called commutation. Thyristor turn-off characteristics is shown in Fig. 2.7.

2.1.2.3 *Thyristor Protection Methods*

Higher than rated anode voltage and anode current, dV_a/dt, dI_a/dt, surge current, gate voltage, negative gate bias and inadequate heat sink can destroy the device permanently. Protection techniques against these abnormal conditions are discussed here.

(i) **Thyrector for Overvoltage Protection**

In the thyristorised circuits overvoltage can be developed due to external and/or internal reasons. Overvoltage generated from short circuits, improper load, and wrong commutation, come under internally generated overvoltages. And externally generated voltage many be produced due to switchings in the supply system, lightning surges and variation in supply itself. These overvoltages may be several times the thyristor breakover voltage (V_{BO}). For protection of the thyristor from overvoltage, thyrector diode (non-linear resistance device whose resistance decreases with increase in the voltage) is connected across the input terminals of the thyristorised circuit as shown in Fig. 2.8.

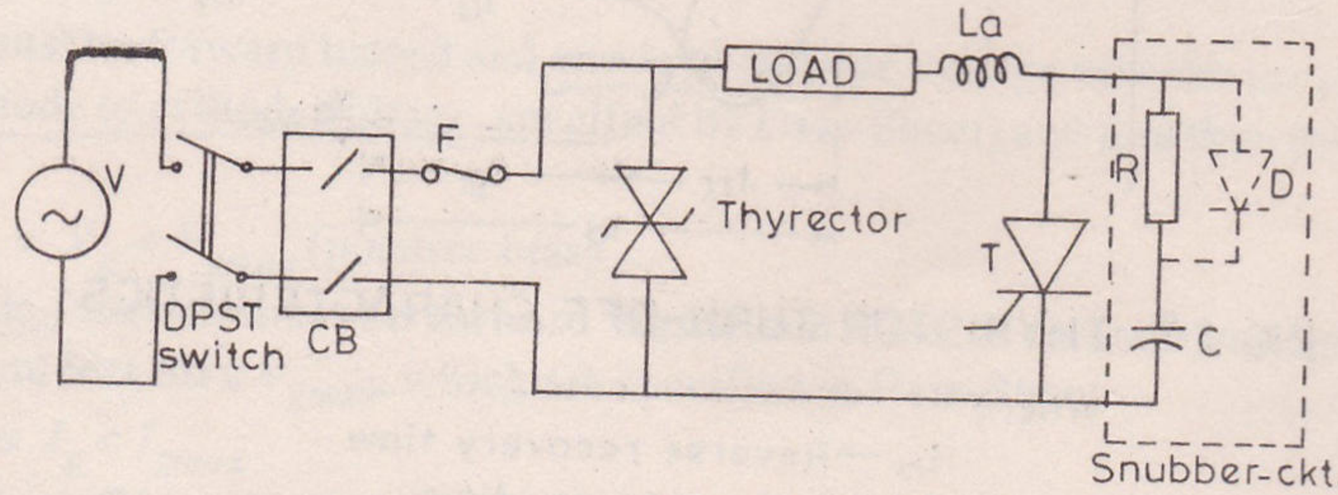


FIG. 2·8: THYRISTOR PROTECTIONS

(ii) Snubber Circuit

R-C series circuit (Snubber circuit) is connected across the thyristor as shown in Fig. 2.8. It protects the thyristor against large *dV/dt* and internal voltage transients which are generated at the time of reverse recovery of the thyristor during commutation.

(iii) Small Inductor (L_a)

A small air core inductor, of 2 to 10 turns of enamelled copper wire, is connected in series with the thyristor, as shown in Fig. 2.8. It limits dI_a/dt within thyristor rating.

(iv) Circuit Breaker (CB), Fuse and Closed-loop Current Control (CLCC)

Circuit breakers and fuses are used in the thyristorised circuits for protecting the device from overcurrents which can occur due to internal or external short circuit. Circuit Breakers have longer tripping time, therefore, they are used against surge currents of long duration and/or continuous overloads. The thyristor is protected against surge currents of very short duration (subcycle surge currents) by using the fast-acting fuses.

A thyristor may withstand a surge of around 50 ms duration with the magnitude upto around 10 times the rated rms current. So thyristors also can be protected against overload by the fast acting (controlled within 40 ms) closed-loop current control circuits.

(v) Gate Networks

Pulse transformers or optical isolators are used for providing isolation between firing circuit and the gate. The use of pulse train of frequency 5 to 10 KHz, instead of a single pulse, allows a reduction in the size of pulse transformer and reduces the gate power loss. Diode D_1 in series with secondary of pulse transformer and gate, prevents the flow of a reverse current (from cathode to gate). And a diode D_2 is connected across the secondary of the transformer or across the gate and cathode for protecting the gate from large reverse voltage. Gate driving circuit is shown in Fig. 2.9.

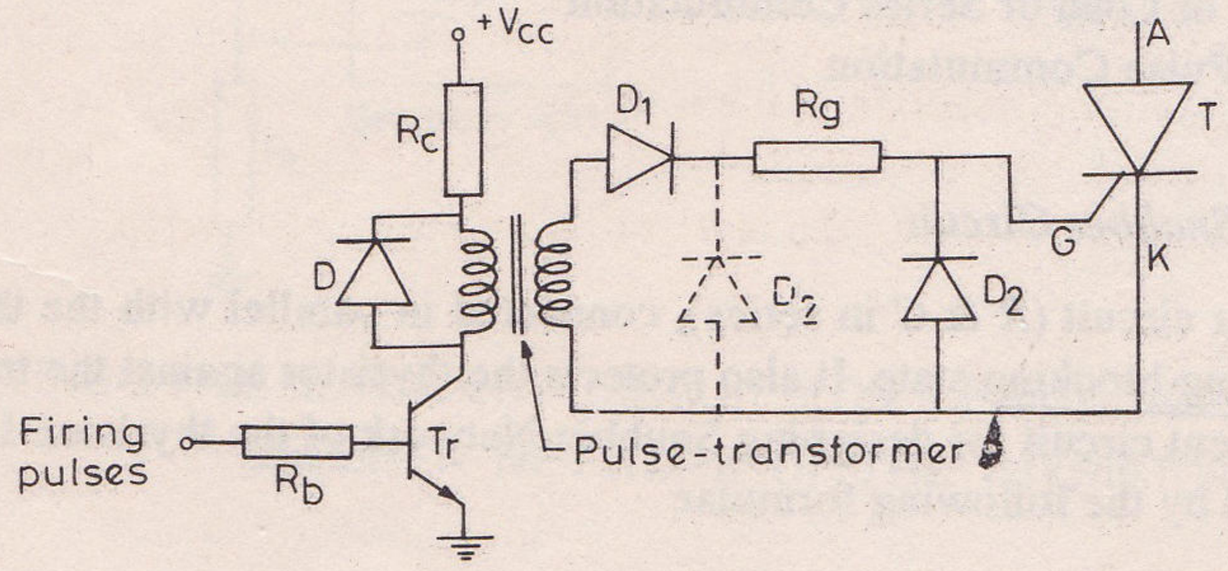


FIG. 2·9 : THYRISTOR'S GATE DRIVING CIRCUIT

(vi) **Heat-Sink**

Thyristors are available upto 2500*V* and 2000*A* (average). The thyristor body alone can- not dissipate sufficient heat, which is produced during the coduction period of the device. The power dissipated in the thyristor increases with the increase in the power rating. If the junction temperature exceeds $125^{\circ}C$, the thyristor can be damaged permanently. Therefore, thyristors are mounted on heat-sinks for dissipating the generated heat, so that the junction temperature can be limited to a satisfactory level. The size of the heat-sink is chosen according to the amount of heat to be dissipated. Fig. 2.10 shows thyristor with heat-sink.

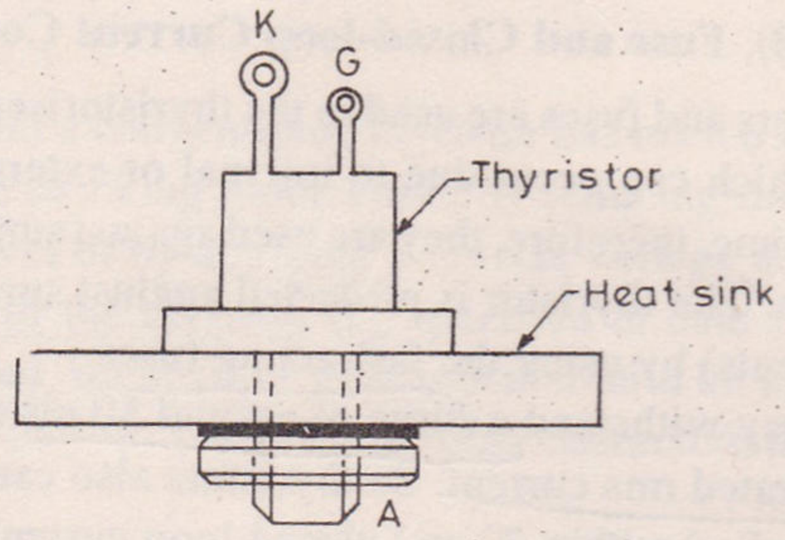


FIG. 2·10 : THYRISTOR WITH HEAT SINK

2.1.2.4 *Thyristor Commutation*

The turn-off process of a thyristor is called commutation. The conventional thyristor can be brought back to the blocking mode from conduction mode by reducing the forward current below the holding current (I_h) level by applying a reverse voltage across the thyristor for a period higher than thyristor turn-off time (t_q). Thyristor commutation schemes are classified in the following groups :

1. Line or Natural Commutation
2. Forced Commutation
3. Self Commutation
4. Resonant or Load or Series Commutation
5. External Pulse Commutation

2.1.2.5 *Design of Snubber Circuit*

The snubber circuit (*R* & *C* in series), connected in parallel with the thyristor, controls the *dv/dt* across it, during blocking state. It also protects the thyristor against the transient voltage. Fig. 2.11 shows equivalent circuit for designing Snubber Network of the thyristor. In DC circuits, *R* and *C* can be calculated by the following formulae

$$\frac{dv}{dt} = VR/L \tag{2.2}$$

$$R + R_L = 2\sqrt{(L/C)} \tag{2.3}$$

where *dv/dt* value must be less than the rated value.

When circuit is excited by an ac source, the following formulae are used :

(a) Equations (2.2) and (2.3) can be used after *V* is replaced by peak amplitude of input voltage (V_p).

(b) The following formulae can also be used

$$C = 600\ \frac{V_L I_L}{V^2 f} \tag{2.4}$$

$$R = 1.3\sqrt{(L/C)} \tag{2.5}$$

where C = minimum capacitance in microfarads
$V_L I_L$ = full-load volt-ampere rating of the circuit
V = r.m.s. value of the applied voltage.
f = frequency of supply

If maximum dv/dt is known, then eqn. (2.6) is used in place of eqn. (2.4).

$$C \approx \frac{0.16}{L}\ \left[\frac{V_p}{dv/dt}\right]^2 \tag{2.6}$$

The formula (2.7) must be satisfied when the power is energised by ac or dc power supply.

$$I_{pr} > (V_p/R) \tag{2.7}$$

where; I_{pr} = Peak repititive current rating of the device.
and V_p = Peak value of the energised voltage.

Sometimes a diode D is connected across R in the snubber circuit as shown by the dotted lines in Fig. 2.11, to make the snubber action more effective.

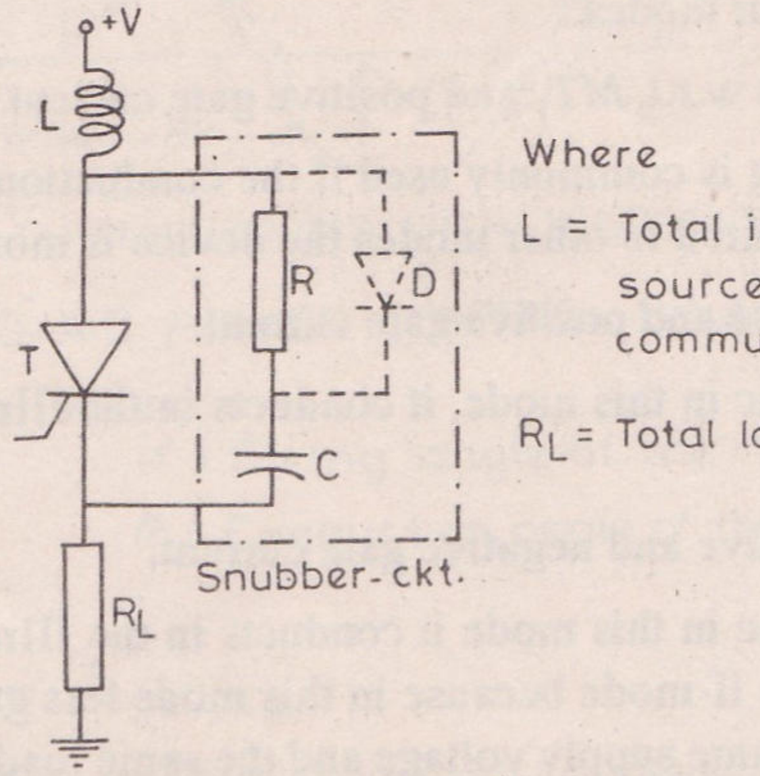


FIG. 2.11: EQUIVALENT CIRCUIT FOR DESIGNING SNUBBER NETWORK OF THE THYRISTOR

2.1.3 Triac

Triac symbol and characteristics are shown in Fig. 2.12 (a) and 2.12(b). A triac has three terminals MT_2, MT_1 and G (Gate). The triac can be turned-on with positive or negative gate current ($\pm I_g$) by keeping the MT_2 terminal at positive or negative voltage with respect to MT_1. It is a bilateral device and equivalent to two thyristors connected in anti-parallel.

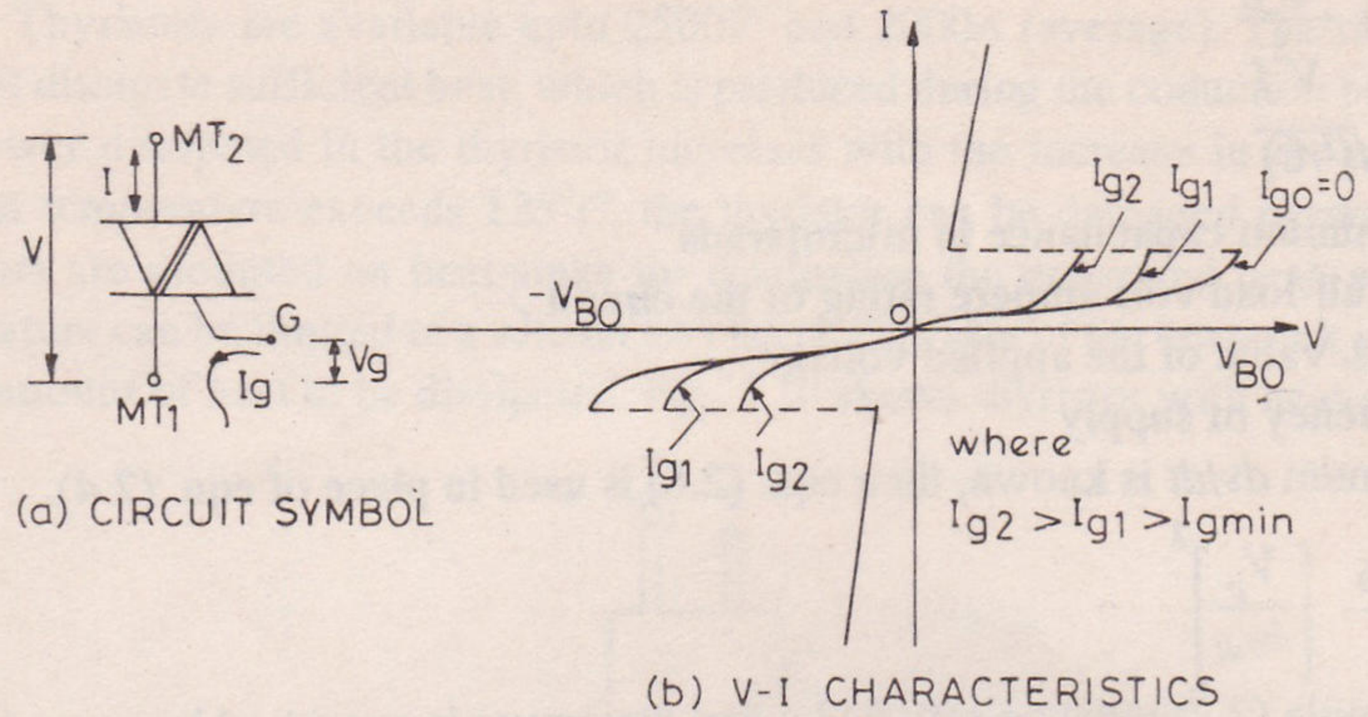


FIG. 2·12: CIRCUIT SYMBOL AND V-I CHARACTERISTICS OF A TRIAC

2.1.3.1 *Modes of Triggering a Triac*

A triac can be triggered in four modes :

(1) **I-Mode** : MT_2 terminal positive w.r.t. MT_1 and positive gate current.

This mode of triggering is commonly used if the conduction of the triac is required in the 1st quadrant because compared to other modes the device is more sensitive in this mode.

(2) **II-Mode** : MT_2 terminal negative and positive gate current.

After triggering the triac in this mode, it conducts in the IIIrd quadrant. The device is less sensitive in this mode.

(3) **III-Mode** : Terminal MT_2 negative and negative gate current.

After triggering the triac in this mode it conducts in the IIIrd quadrant. The device is more sensitive compared to the II-mode because in this mode less gate current is required for triggering the device with the same supply voltage and the same load compared to the positive gate current as shown in II-mode.

(4) **IV-Mode** : terminal MT_2 positive and negative gate current.

After triggering in this mode, the device operates in the Ist quadrant. The device is less sensitive in this mode compared to the I-mode of operation because the device requires more gate current (I_g) in this mode.

I (MT_2 positive with $+I_g$) and III (MT_2 negative with $-Ig$) modes are commonly used as they are more sensitive. Generally, the triac is used for controlling ac power as shown in Fig. 2.13. The circuit can control maximum upto 50% ac power because the firing angle of the triac can be controlled from 0° to 90° in each half-cycle.

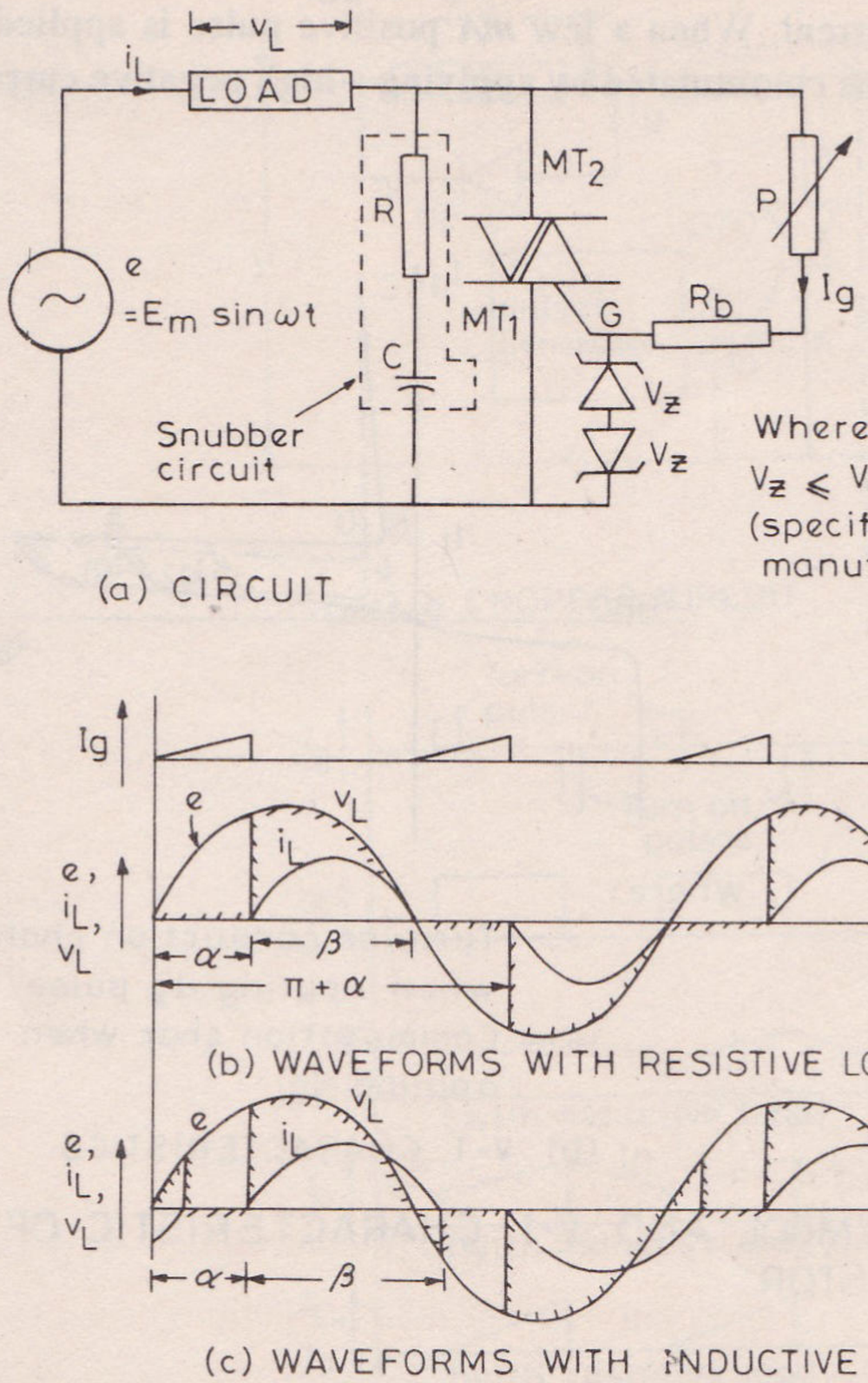


FIG.2-13: A C POWER CONTROL BY A TRIAC

where:

α = Firing angle of the thyristor

β = Conduction angle of the "

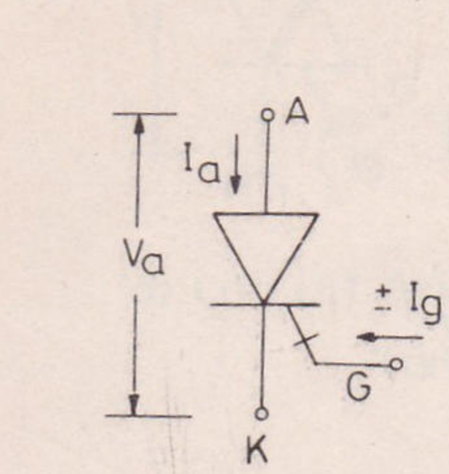
2.1.3.2 *Protection of Triacs*

Triacs are protected the same way as thyristors. Further more care is required for designing the Snubber circuit because the triac has lower *dv/dt* rating.

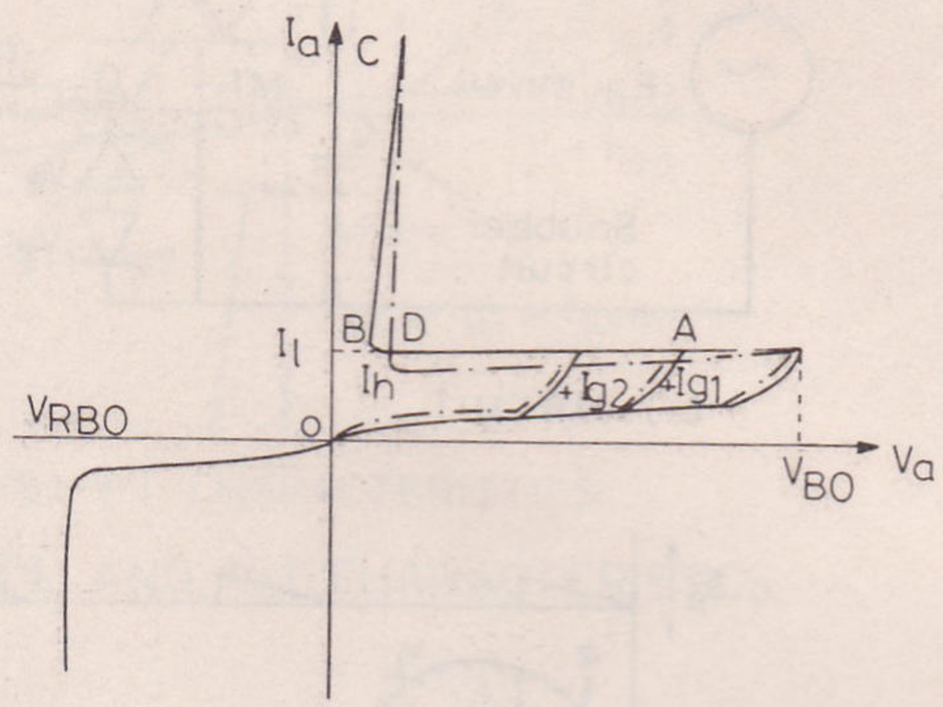
2.1.4 Gate-turn-off Thyristor (GTO-Thyristor)

A GTO-thyristor is a special type of thyristor which has the same turn-on characteristics but different turn-off (commutation) characteristics than a conventional thyristor. The GTO is commutated by applying a negative gate current (I_g) pulse of few microseconds with the magnitude upto 1/3 to 1/5 times the anode current, i.e., for commutating a GTO rated 100*A*, the negative gate current pulse amplitude may be about 25*A*. GTOs are commercially available upto 2000*A* (*av.*) and 2500*V* (*av.*). The circuit symbol and characteristic of a GTO are shown in Fig. 2.14. If forward

potential across GTO is less than forward breakover voltage (V_{BO}), a leakage current flows through GTO in the absence of the gate current. When a few *mA* positive pulse is applied to the gate, the device is turned-on. The GTO can be commutated by applying a high negative current pulse to gate.



(a) CIRCUIT SYMBOL



Where:

—— Turn-on conduction char. when appling +Ig pulse

—·— Commutation char. when appling -Ig

(b) V-I CHARACTERISTICS

FIG. 2.14 CIRCUIT SYMBOL AND V-I CHARACTERISTIC OF A GTO-THYRISTOR

The GTO circuits have less volume and higher frequency of operation than thyristor circuits, because the bulky commutation circuits are not required to commutate the GTO. Due to the above advantages, the GTO converters (choppers, inverters, cyclo-converters, etc.), are replacing thyristor converters.

2.1.4.1 *Firing Circuit and Polarised Snubber Circuit for GTO*

Two sets of pulses are required to control the GTO thyristor. One pulse set of low positive amplitude for turn-on and other pulse set of high negative amplitude for turn-off. The GTO firing circuit generates turn-on and turn-off pulses alternatively.

The Snubber of GTO has three functions as following :

(i) Protects the device against dv/dt during its off-state.

(ii) Protects the device against dv/dt during commutation period and after the commutation.

(iii) Reduces its power dissipation during turn-off period.

To fulfil the above requirement, a polarised snubber is used and the snubber capacitor size is several times higher than that of the thyristor. A GTO chopper circuit is shown in Fig. 2.15.

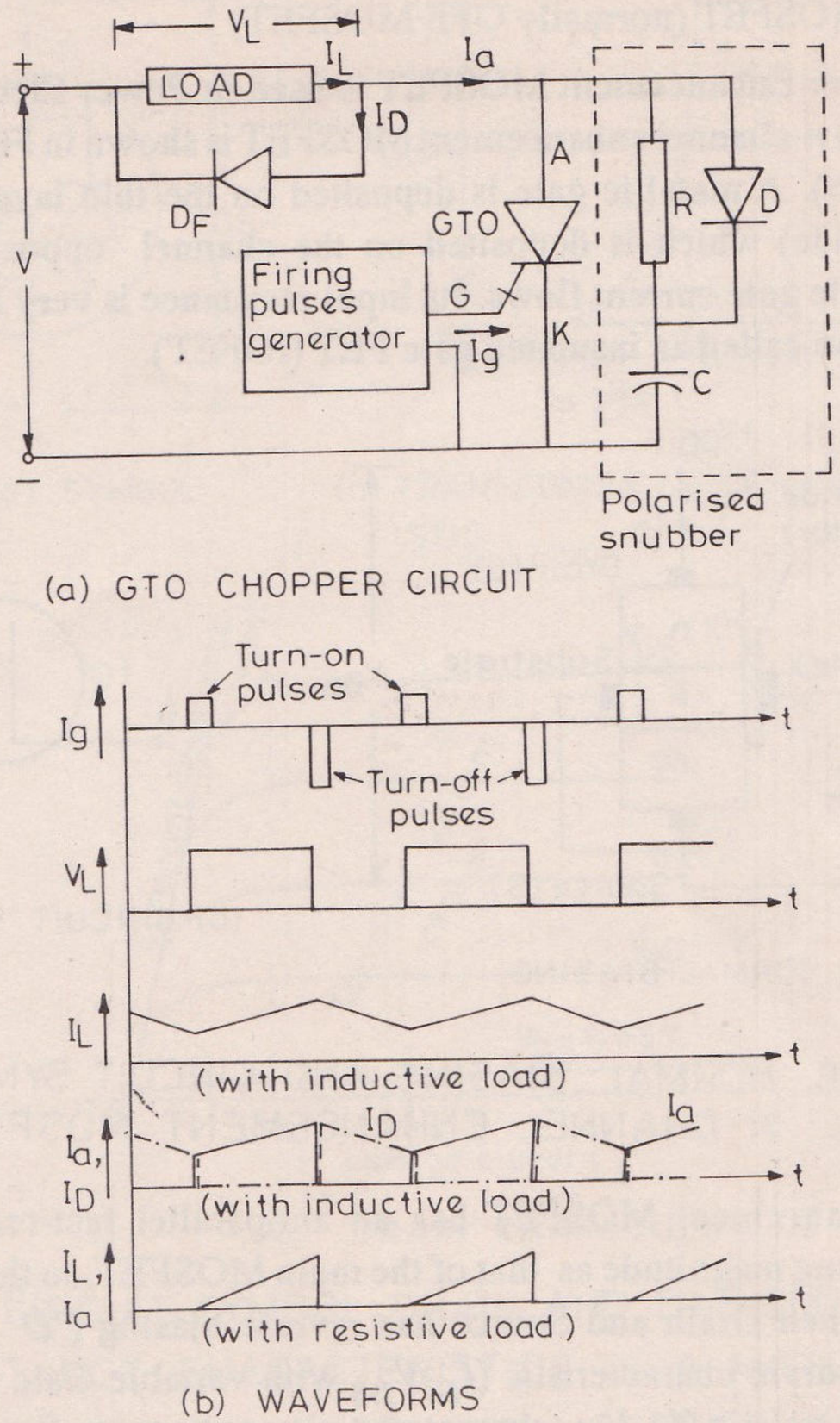


FIG. 2·15: GTO CHOPPER AND ITS WAVEFORMS

2.1.5 Power MOSFETs

Power MOSFETs (metal-oxide semiconductor field-effected transistors) can be used in low power converters (chopper, inverter, etc.) due to their superior characteristics. The ratings upto 100V, 72 *A* and 500 *V*, 26 *A* are available.

It is a unipolar device. It needs only majority carriers to work. The FET is a voltage controlled device while transistor is a current controlled device. MOSFET has four terminals known as Drain, Source, Gate and Substrate, but generally, the manufacturer internally connects the substrate to the source, so three terminals come outside the device, i.e., Drain, Source and Gate. MOSFETs are classified according to the used extrinsic semiconductor in the channel of a MOSFET, such as :

P-channel MOSFET

N-channel MOSFET

P-channel and *N*-channel MOSFETs are further classified according to the characteristics of the device :

Depletion-enhancement MOSFETs (normally ON MOSFET)
enhancement MOSFET (normally OFF MOSFET)

Generally, Power Enhancement MOSFET is used in Power Electronic Circuits. Its structure with normal biasing of a *n*-channel enhancement MOSFET is shown in Fig. 2.16(a) and circuit symbol is shown in Fig. 2.16(b). A metallic gate is deposited on the thin layer of metal oxide (insulator, generally, silicon dioxide) which is deposited on the channel opposite to the substrate. Due to insulated gate, negligible gate current flows. Its input resistance is very high, i.e., from 15 *K*Ω. to 10 *M* Ω. A MOSFET is also called as insulated gate FET (IGFET).

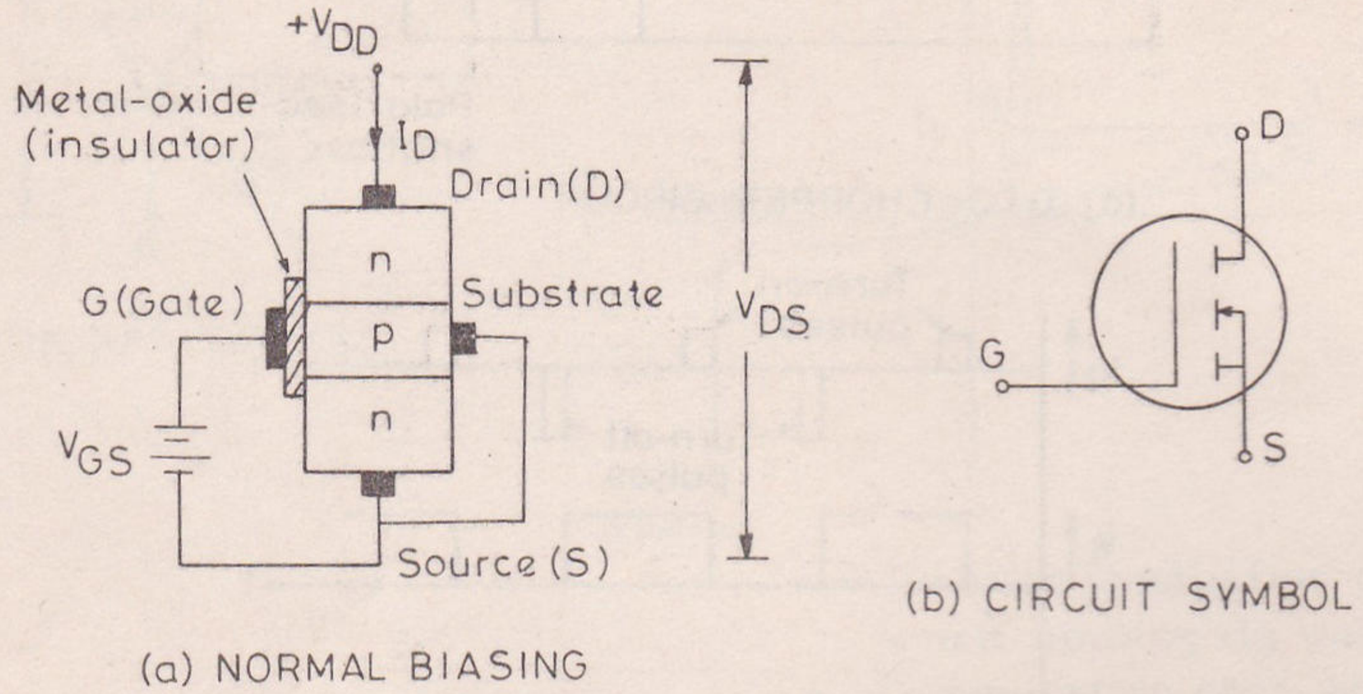


FIG. 2.16 NORMAL BIASING AND CIRCUIT SYMBOL OF A N-CHANNEL ENHANCEMENT MOSFET

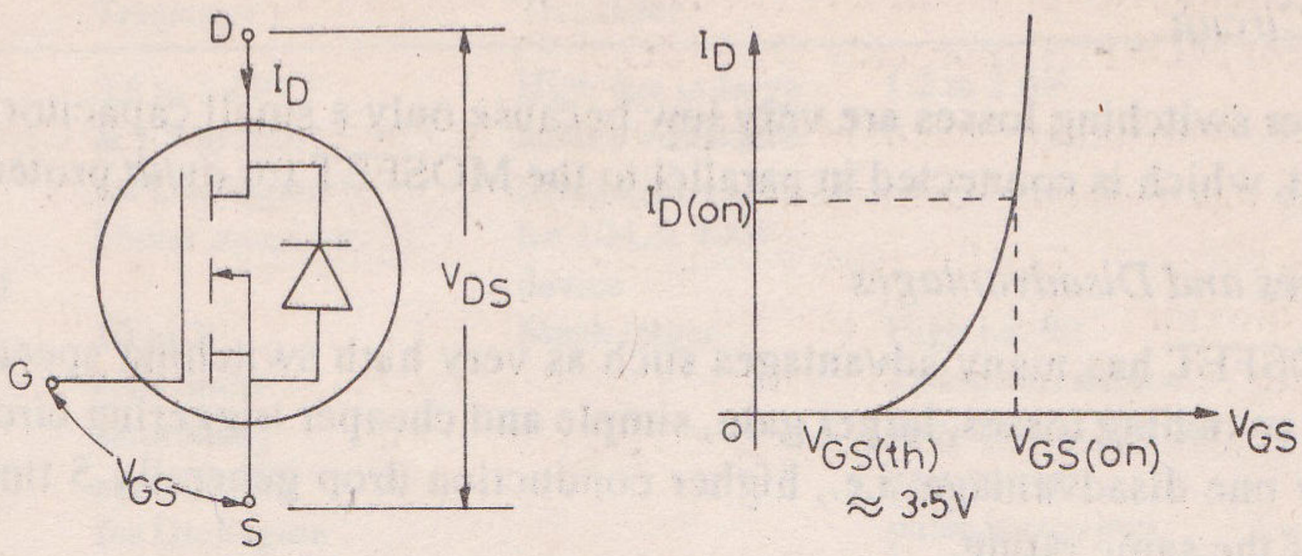
The power enhancement MOSFET has an antiparallel fast-turn-on diode which permits reverse current of the same magnitude as that of the main MOSFET, so that, Drain-Substrate junction will not be damaged when Drain and Source has reverse biasing (*'D'* terminal negative *w.r.t. 'S'* terminal). The symbol, drain characteristic (I_D-V_{DS} with variable Gate voltage characteristic), and transconductance characteristic (I_D-V_{GS} characteristic) are shown in Fig. 2.17 (a,b,c).

2.1.5.1 *Threshold Voltage [$V_{GS(th)}$]*

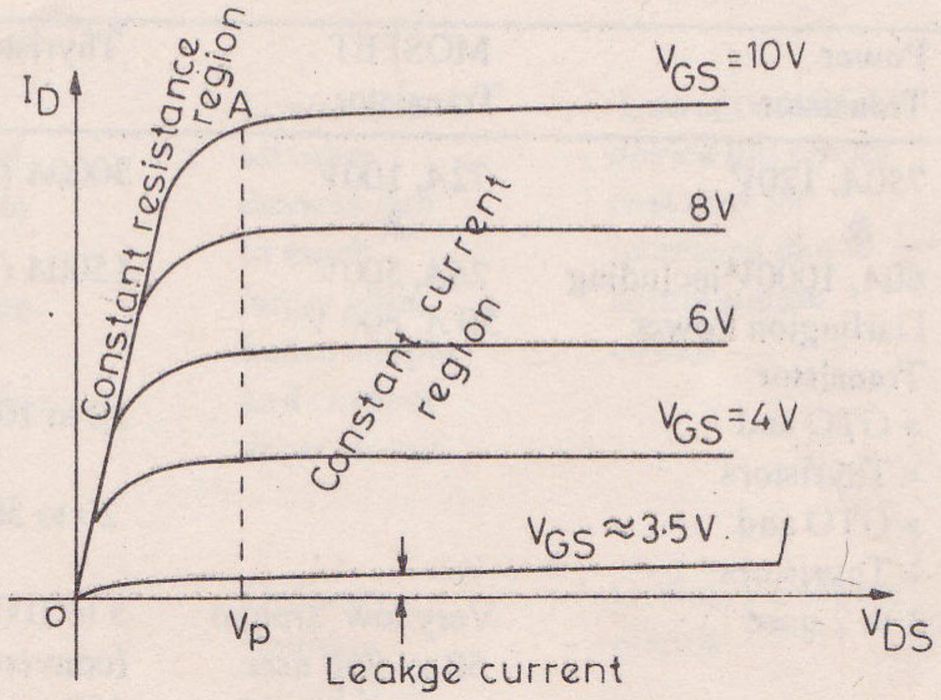
The minimum Gate-Source Voltage ($V_{GS(min)}$) which is required for conduction to start in the enhancement MOSFET, is called Threshold Voltage. If V_{GS} is less than $V_{GS(th)}$, only very small leakage current flows from Drain (*D*) to Source (*S*). And if V_{GS} is greater than ($V_{GS(th)}$), Drain to Source current (I_D) flows the magnitude of which depends upon the magnitude of the Gate Voltage as shown in Fig. 2.17(b). Threshold voltage $V_{GS(th)}$ varies from 2 to 5V.

2 *Pinch-off Voltage (V_p)*

For a particular Gate Voltage (V_{GS}), there is a pinch-off voltage (V_P) between Drain and Source as shown in Fig. 2.17(c) by point A on the Drain characteristic Curve for V_{GS} = 10*V*. If V_{DS} is lower below than V_p, the device works in the constant resistance region, and Drain-Current (I_D) is directly proportional to the V_{DS}. But when V_{DS} is more than V_p, constant Drain-Current (I_D) flows from the device and this operating region is called constant current region.



(a) CIRCUIT SYMBOL (b) TRANSCONDUCTANCE CHARACTERISTIC



(c) DRAIN CHARACTERISTICS

FIG. 2·17 : CIRCUIT SYMBOL, DRAIN AND TRANSCONDUCTANCE CHARACTERISTICS OF A N-CHANNEL POWER ENHANCEMENT MOSFET

2.1.5.3 *Transconductance Characteristic*

As shown in Fig. 2.17(b), the transconductance curve of an enhancement MOSFET follows the parabolic or square-law, so the equation of Drain-Current (I_D) is

$$I_D = KV_G^2$$

where V_G = difference between actual gate voltage (V_{DS}) and threshold voltage.

K = proportionality constant which depends upon the device to device.

2.1.5.4 *Applications*

The enhancement -MOSFET is used as a switch in Power-Electronic by keeping sufficient Gate Voltage (V_{GS}) so that it conducts in the constant resistance region. The conduction loss of the MOSFET is high due to large value of device resistance in the ON-state. The MOSFET can be triggered directly from the CMOS or other gates due to high input impedance. Switching times (turn-on and turn-off) are very low around 200 ns for a 500*V*, 26*A* device. Its switching loss is almost nil. The gate drive power is also negligible.

2.1.5.5 *Snubber Circuit*

The snubber switching losses are very low because only a small capacitor is required in the RC snubber circuit, which is connected in parallel to the MOSFET for *dv/dt* protection.

2.1.5.6 *Advantages and Disadvantages*

Power MOSFET has many advantages such as very high switching speed, very high input impedance, lower switching losses, larger gain, simple and cheaper triggering circuit, etc.

It has only one disadvantage, i.e., higher conduction drop generally 5 times more than the power transistor of the same rating.

2.1.6 Comparison Between Different Power Semiconductor Devices

	Features	Power Transistor	MOSFET Transistor	Thyristor	GTO
1.	Available upto the ratings	750*A*, 120*V* & 60*A*, 1000*V* including Darlington Power Transistor	72*A*, 100*V* & 26*A*, 500*V* 50 *A*, 800 *V*	3000*A* (*av*), 1200*V* & 1500*A* (*av*), 4000*V*	2000*A*, 2500*V*
2.	*dV/dt* rating	> GTO and < Thyristors		20 to 1000*V*/usec	
3.	*dI/dt* rating	> GTO and < Thyristors		20 to 500 *A*/usec	
4.	Turn-off time (t_{off})	1 to 2 usec	Very low around 50 to 250 nsec.	5 to 100 usec (converter Grade 50 to 100 usec & Inverter Grade 5 to 25 usec)	About 5 usec
5.	Turn-on time (t_{on})	1 to 2 usec. Much higher than thyristor and GTO but lower than MOSFET	50 to 250 nanosec.	1 to 2 usec	1 to 2 usec
6	Frequency	Very high		Low	Higher than Thyristor
7	Gate or base pulse magnitude and width during turn-on	Large and continuous base drive upto turn-on period of the device (t_{on})	Upto turn-on period of the device (t_{on})	After the turn-on of the device, gate losses its control. It is triggered by a small current pulse of duration greater than the turn-on time of the device.	Same as Thyristor
8.	Turn-off process (commutation)	Positive base drive is removed and negative base drive is applied if fast turn-off is required	By making gate voltage (V_{GS}) zero	Negative bias is required at main terminals (Anode must be negative *w.r.t.* cathode) and gate pulse is removed	Negative gate current pulse of much higher magnitude is required for few msec and it can be commutated in the presence of forward biasing of the device
9.	Commutation circuit is required	No	No	Yes but Not required when line commutation is used	No

Features	Power Transistor	MOSFET Transistor	Thyristor	GTO
10. Voltage drop across device in ON-period (conduction drop)	0.6 to 1.1*V* & 1.7 to 2.2*V* for Darlington Power transistor	High due to large device resistance ($R_{DS(on)}$), i.e., ≈ 4.5*V* for 10*A* & 400*V* device	1.2 to 2.6*V*	1.2. to 2.6*V*
11. Current gain of device = (Max. load current/ Max. gate current)	10 to 20 (just under saturation) and 100-300 for Darlington Power transistor	Much larger	High i.e. for 250*A* rated device only around 500 m*A* gate current pulse is required for turn-on	Same as thyristor
12. Isolator between Triggering circuit & main power circuit	Optical-isolator	Not required	Pulse transformer or Optical isolator	Optical-isolator
13. Circuit cost in converters requiring forced commutation	Lower than thyristorised circuit due to absence of commutation circuit (cheaper drive upto 230*V* and less)	Lower than all other devices due to much larger gain, hence simple and cheaper drive circuit	Lower cost of the device but circuit cost may be increased due to commutation circuit	Higher cost of the device compared with the thyristor but total circuit cost is reduced because com-mutation circuit is not required
14. Snubber circuit required	Polarised Snubber circuit	Ordinary Snubber circuit with a small capacitor	Ordinary Snubber circuit	Polarised Snubber circuit with higher capacitor
15. Device circuit power losses	Lower than thyristor due to absence of commutation circuit but higher than GTO	Very low compared to all other devices	Moderate	Moderate
16. Converter efficiency	Low	Very High	High but less than GTO due to the commutation circuit losses	High
17. Volume of Total Circuit	Less than thyristor due to the absence of commutation circuit	Least	Large	Small compared with thyristor circuit due to the absence of commutation circuit
18. Available Power rating	Upto 200 *KW*	Few *KW*	Upto few Megawatts	Somewhat lower than thyristor
19. Reserve voltage capability	No	No	Good	Absent in shorted emitter structure
20. Can provide current limit protection	Yes (by controlling base current)	Yes (by controlling gate voltage)	Yes (by firing angle control)	Yes (by controlling t_{on} and t_{off} period of device)

Features	Power Transistor	MOSFET Transistor	Thyristor	GTO
21. Ratio of Max. surge Current to continuous current of device	Low		High	High
22. Parallel operation of devices	Difficult because of negative resistance coefficient	Easy because of positive resistance coefficient	Easy	Easy
23. Input impedance	Low	Very high (because the gate is electrically isolated from the channel by a metal-oxide layer)	Medium	Medium
24. Nature of device	Current controlled	Voltage controlled	Drive pulse of the small duration is required only for turn-on	Positive and negative drive pulses of the small duration are required for turn-on and turn-off respectively
25. Gate/base circuit power losses	Very high	Very low	Low	Low

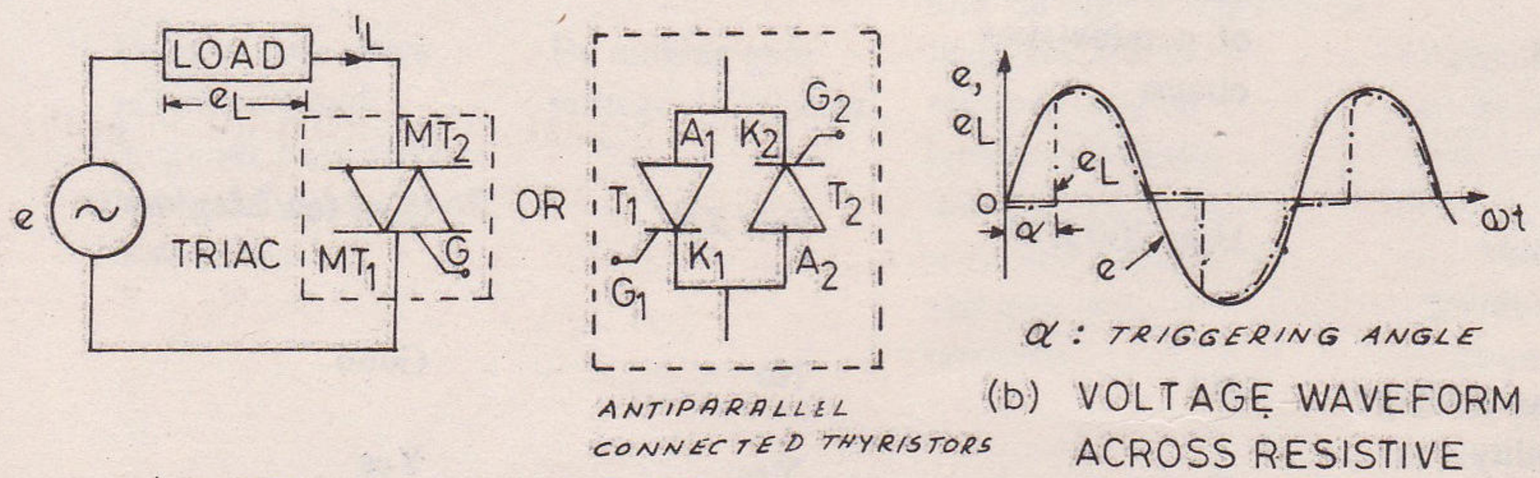
2.2 POWER CONVERTERS

The power semiconductor converters are described in detail in chapter 4. A brief description of commonly used converters is given below :

1. AC Regulators

The ac regulators convert a fixed ac voltage to a variable ac voltage at the same frequency. The ac regulator circuit and load voltage waveforms are shown in Fig. 2.18.

USES : Illumination control, temperature control and speed control of ac drives (fans and pumps).



(a) AC REGULATOR CIRCUITS (b) VOLTAGE WAVEFORM ACROSS RESISTIVE LOAD

FIG. 2.18 : AC REGULATOR CIRCUITS AND WAVEFORM FOR A RESISTIVE LOAD

2. **Rectifiers (Converters)**

(a) Uncontrolled Converters :

The power diodes are used in the uncontrolled converter circuits. These circuits change a fixed ac voltage to a fixed dc voltage. The uncontrolled converter circuits are shown in Fig. 2.19 (a & b).

(b) Controlled Converters :

These circuits change a fixed ac voltage to a variable dc voltage. The controlled converters are shown in Fig. 2.19 (c & d).

USES : Dc drives, dc power supply and HVDC systems.

3. **Choppers (or dc to dc converters)**

These circuits change a fixed dc voltage to a variable dc voltage. A dc chopper circuit is shown in Fig. 2.20. For simplicity, the commutation circuit is not shown in the figure.

4. **Inverters**

The inverters change a fixed dc voltage into a fixed or variable ac voltage of fixed or variable frequency. The inverter circuit is shown in Fig. 2.21.

USES : Fluorescent tubes, speed control of induction and synchronous motors, induction heating.

5. **Cycloconverters**

The cycloconverters change a fixed frequency ac voltage into a variable frequency ac voltage. The cycloconverter circuit is shown in Fig. 2.22.

USES : Rolling mills, Cement Kilns and traction motor speed control.

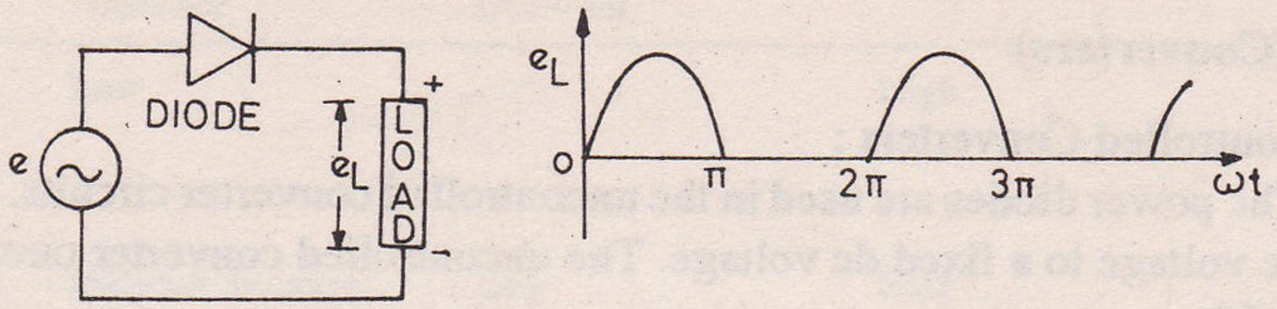
6. **Circuit Breakers**

The semiconductor devices are also used in ac and dc circuit breakers. The ac circuit breaker is shown in Fig. 2.23.

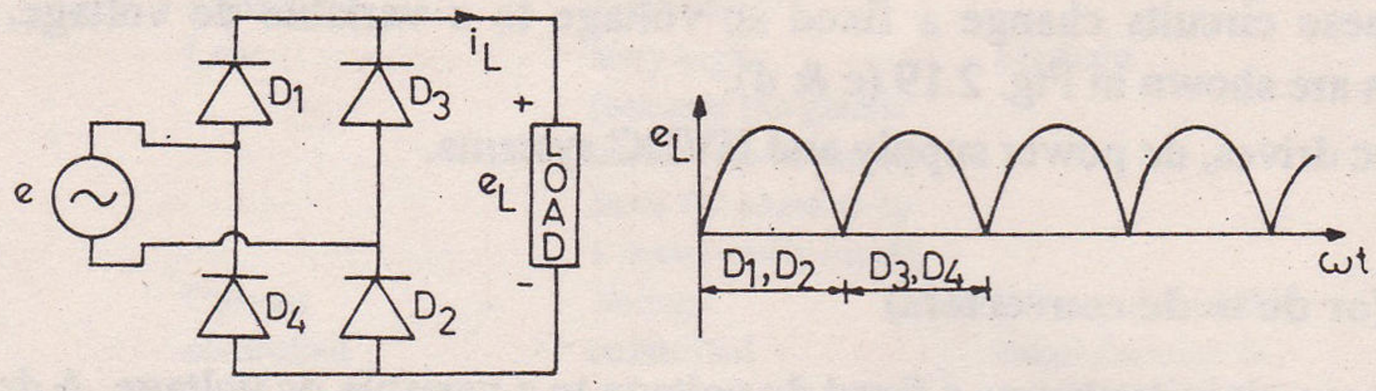
7. **VAR (Reactive Volt Ampere) Compensators**

Now-a-days, semiconductor VAR compensators are used for improving power factor (*pf*) of supply and load. One type VAR compensator is shown in Fig. 2.24.

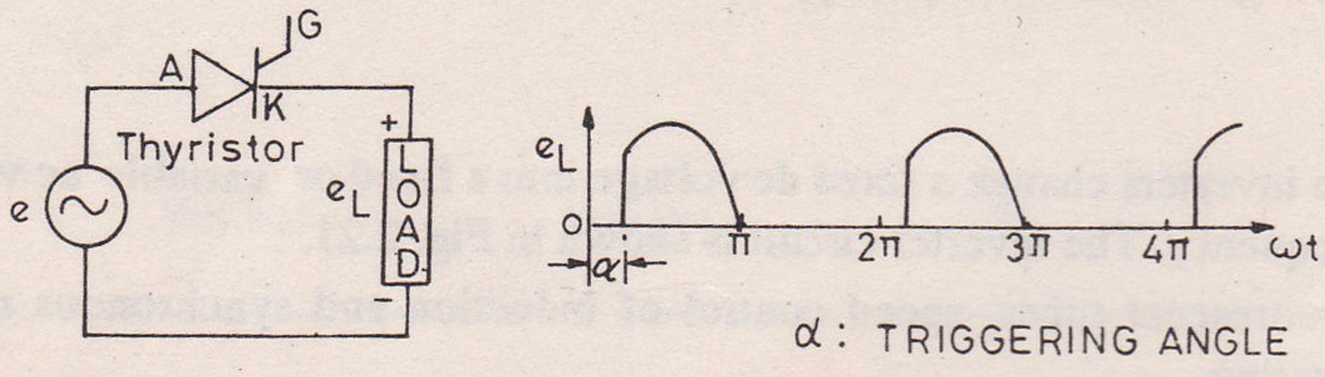
For proper functioning, the solid-state devices are mounted on the Heat-Sinks for radiating excess heat of the devices. The Heat-Sinks are cooled by natural air cooling, forced air cooling, oil cooling or water cooling.



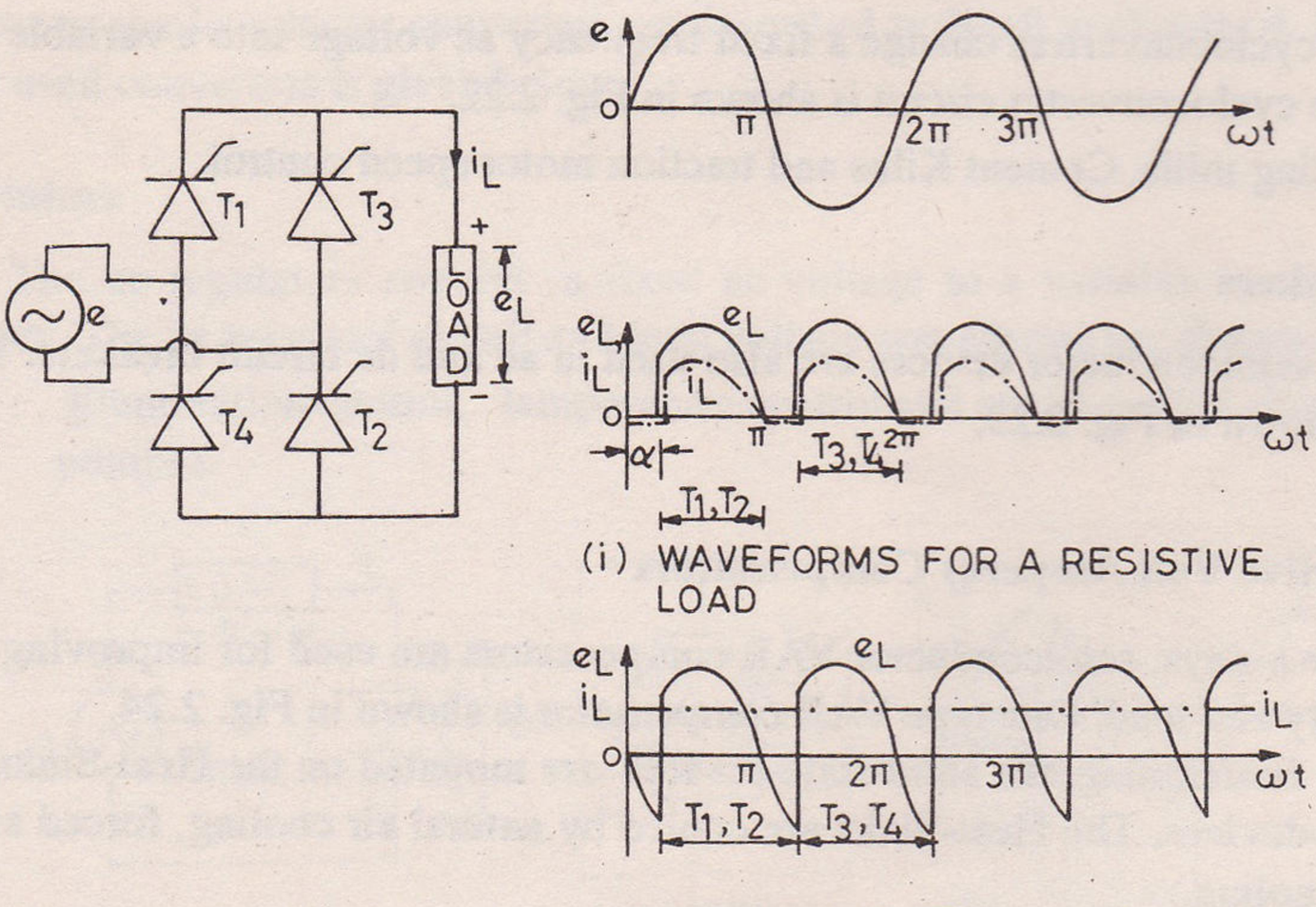
(a) HALF-WAVE UNCONTROLLED RECTIFIER



(b) FULL-WAVE UNCONTROLLED RECTIFIER



(c) HALF-WAVE CONTROLLED RECTIFIER AND VOLTAGE WAVEFORM FOR A RESISTIVE LOAD

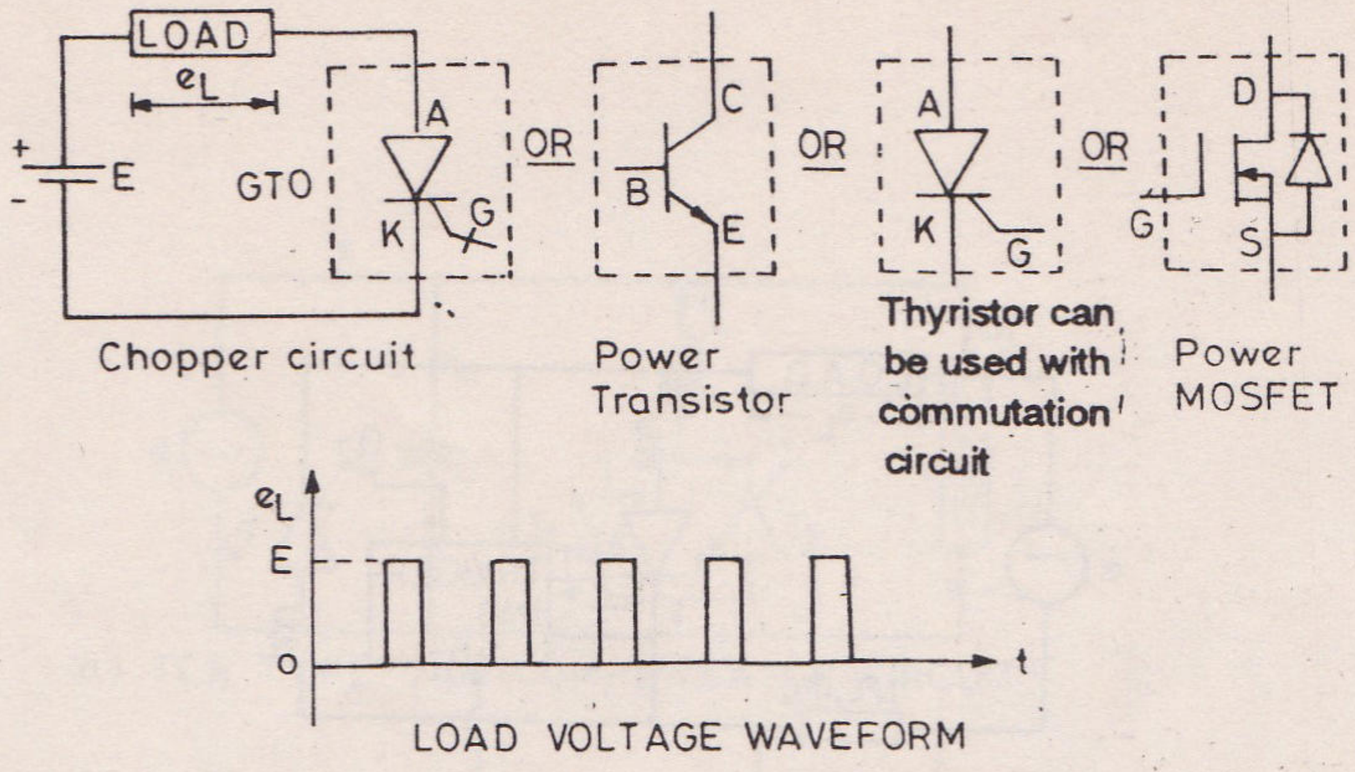


(i) WAVEFORMS FOR A RESISTIVE LOAD

(ii) WAVEFORMS FOR A HIGHLY INDUCTIVE LOAD

(d) FULL-WAVE CONTROLLED RECTIFIER CIRCUIT WITH VOLTAGE AND CURRENT WAVEFORMS FOR A RESISTIVE AND A INDUCTIVE LOAD

FIG. 2·19 DIFFERENT TYPES OF SINGLE PHASE BASIC CONVERTER CIRCUITS AND WAVEFORMS ACROSS THE LOAD



FIG·2·20: CHOPPER CIRCUIT WITH LOAD VOLTAGE WAVEFORM

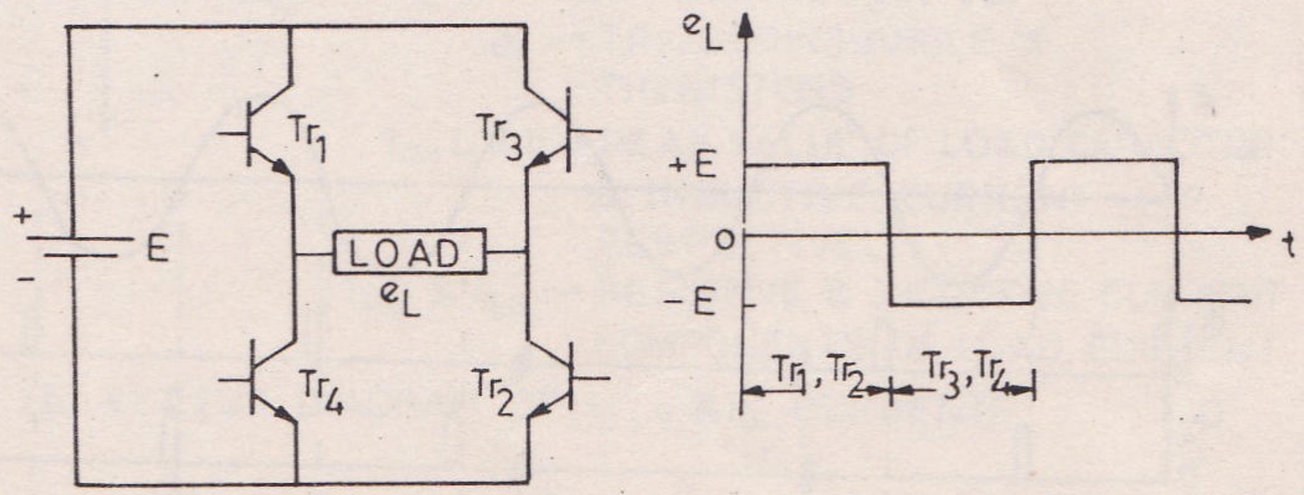


FIG.2·21: TRANSISTORISED INVERTER CIRCUIT WITH LOAD VOLTAGE WAVEFORM

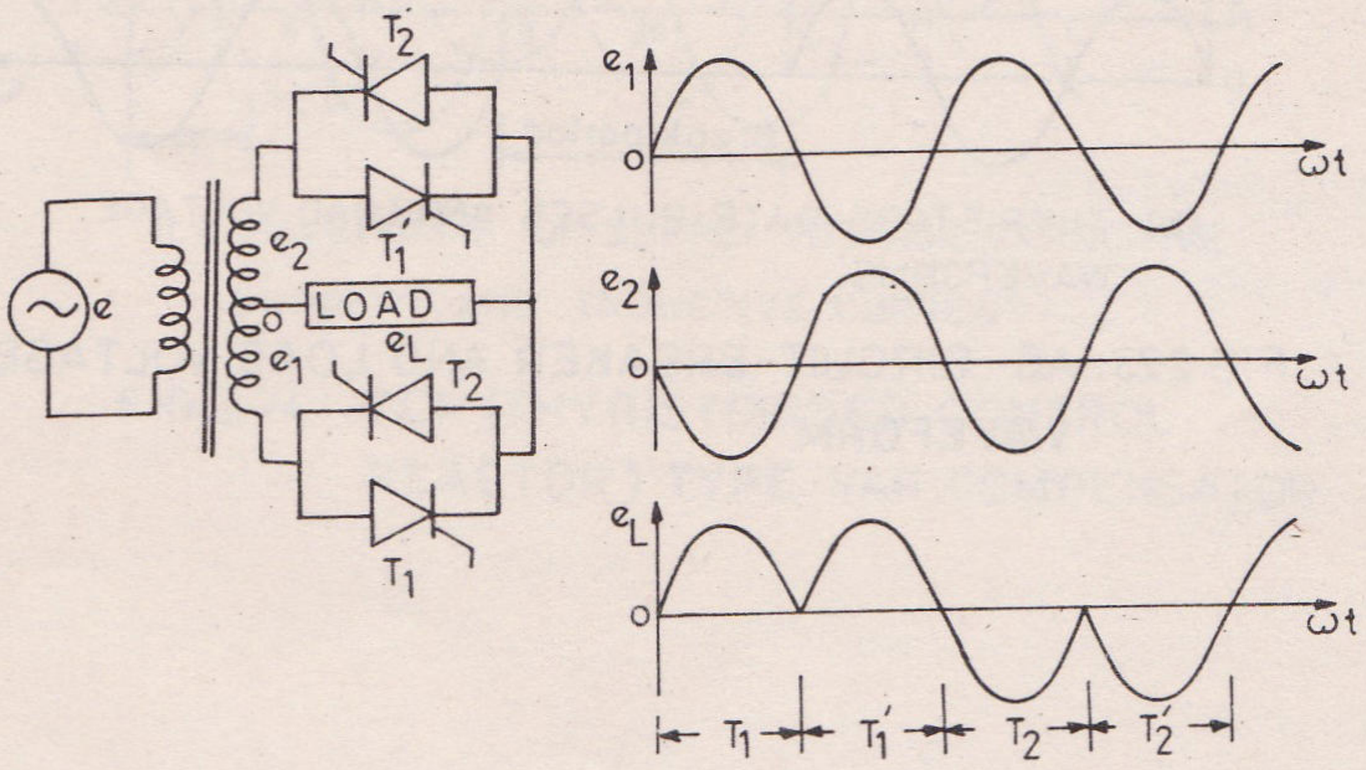
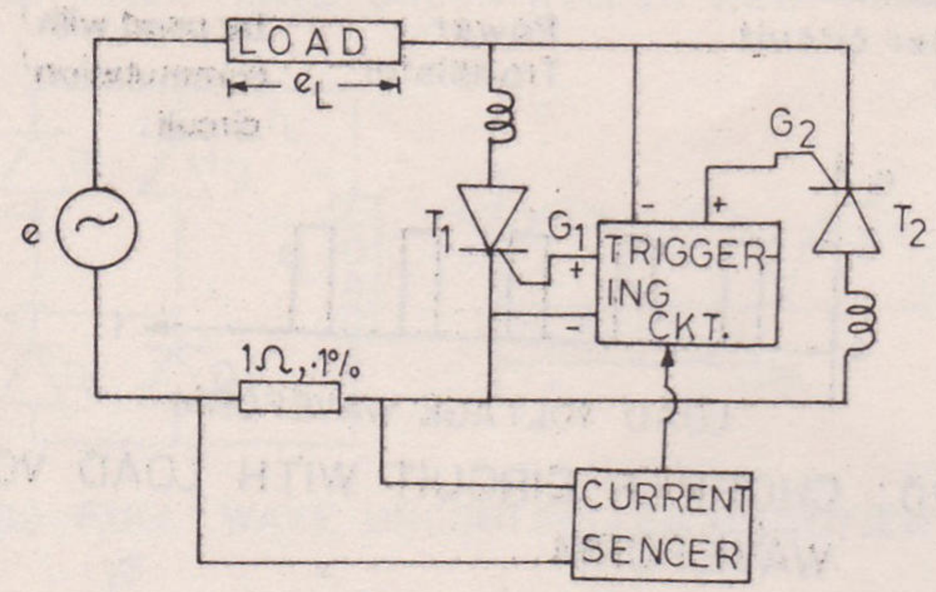
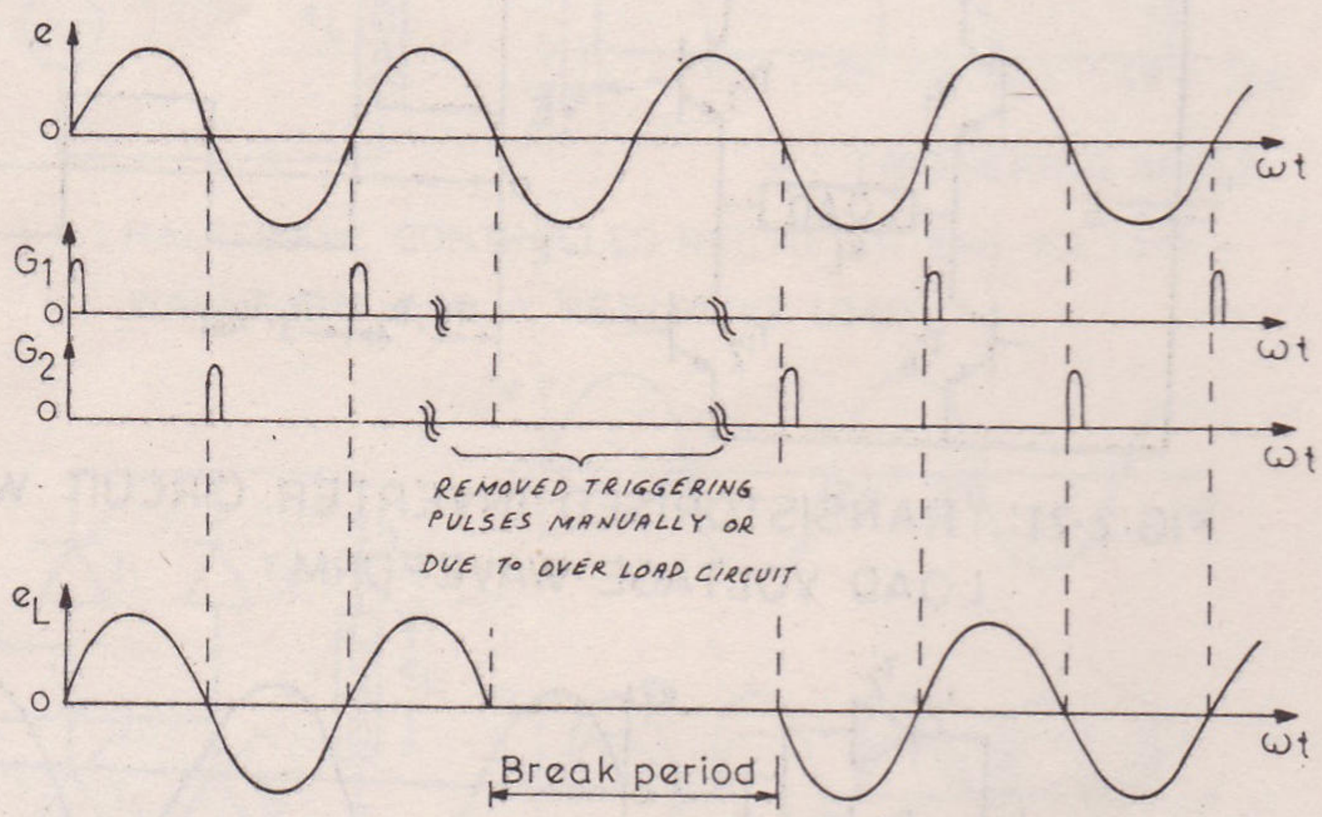


FIG.2·22: CYCLOCONVERTER CIRCUIT WITH RESISTIVE LOAD VOLTAGE WAVEFORM

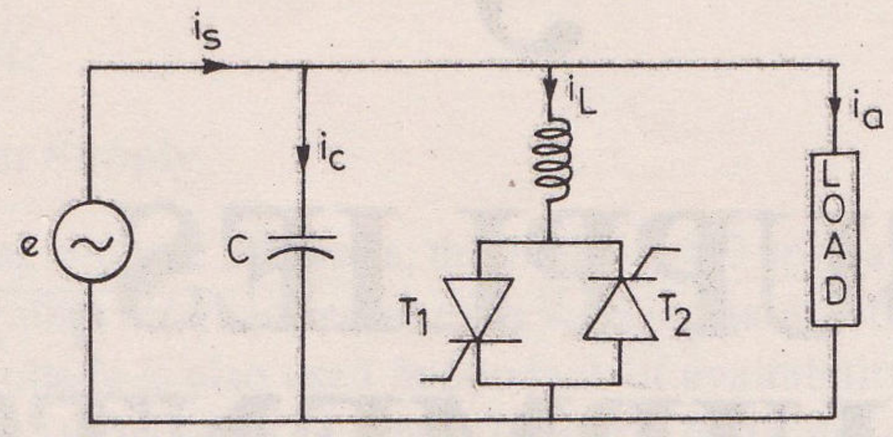


(a) A.C. CIRCUIT-BREAKER'S CIRCUIT

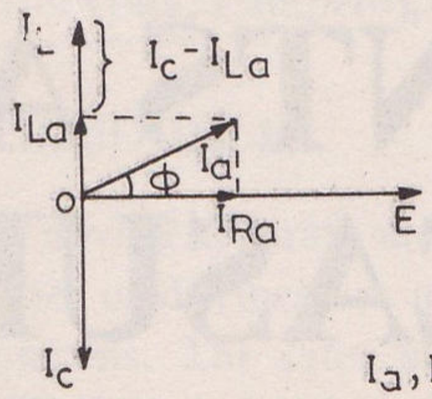


(b) THYRISTORS GATE PULSES AND LOAD VOLTAGE WAVEFORMS

FIG.2·23: A.C. CIRCUIT-BREAKER AND LOAD VOLTAGE WAVEFORM



(a) TCR TYPE VAR COMPENSATOR CIRCUIT



$I_L = I_c$ (AT NO LOAD) & $\alpha = 90^\circ$

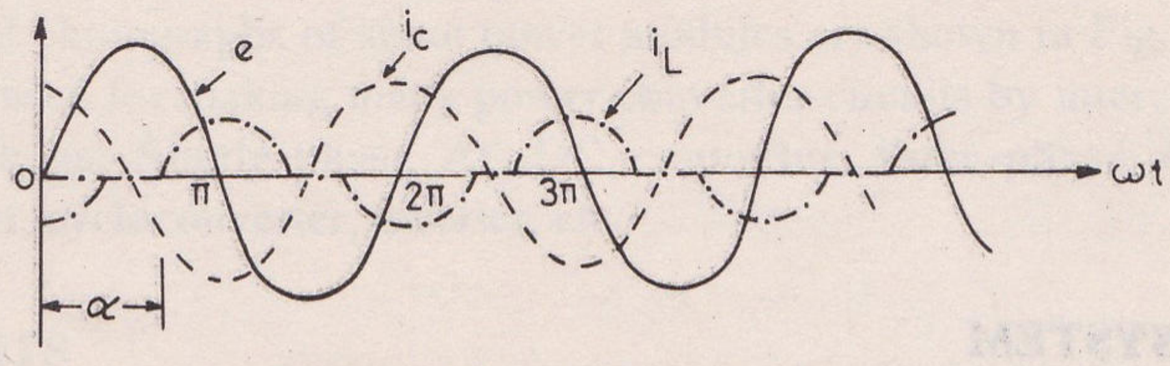
$I_L = I_c - I_{La}$ (AT i_a LOAD) & $\alpha > 90^\circ$

α → TRIGGERING ANGLE OF THYRISTORS

I_a, I_c & I_L → PEAK VALUE OF LOAD, CAPACITOR & INDUCTIVE CURRENT RESPECTIVELY

I_{Ra} & I_{La} → RESISTIVE & INDUCTIVE CURRENT COMPONENTS OF LOAD CURRENT

(b) VECTOR DIAGRAM OF i_c, i_L & i_a CURRENTS



(c) WAVEFORMS OF SUPPLY VOLTAGE, CAPACITIVE CURRENT AND INDUCTIVE CURRENT

FIG. 2·24: TCR (THYRISTORISED CONTROL REACTOR) TYPE VAR COMPENSATOR

3

SUPPLIES, EQUIPMENTS, INSTRUMENTS AND SAFETY MEASURES FOR A POWER ELECTRONICS LAB

3.1 SUPPLY SYSTEM

The power supplies are required in the lab for apparatus, converter modules and control modules.

3.1.1 Power Supply for Control Circuits

Mainly three types of low voltage and power levels supplies are required for supplying power to the control units which consist of digital integrated circuits, discrete circuits and/or microprocessor, etc. These supplies are as follows :

1. *Regulated +5 Volts Power Supply*

The regulated +5*V*, about one ampere power supply is required for TTL-ICs and other discrete circuit components.

2. *Regulated ± 12 Volts and + 24 Volts Power Supplies*

Regulated power supply of ± 12*V*, about one ampere is used for CMOS, HTL and Operation-amplifier integrated circuits. The + 24 Volts power supply is used to supply the power to the pulse amplifier unit.

3.1.2 Converter Power Supply

Generally, the single-phase 220 volts, three-phase 440 volts and 220 volts DC isolated power supplies of high power rating are required in each working-table of the lab. Sometime less voltage than the above written voltage is also used due to lack of availability of the semiconductor devices of the high voltage rating. The variable dc supply from 0 to 600 volts of about 100 *mA* is also required in lab for finding the forward and reverse breakover voltages of small voltage rating thyristors such as thyristor SN-100 (100 volts, 1 ampere), etc.

3.2 CONVERTER MODULES

Either one can have a separate module for each converter circuit or one can have module where a suitable number of devices are mounted and then these can be interconnected to realize different converter circuits. The later alternative is economical. Such modules are termed as generalised modules. The generalised modules may consist of the following :

1. Transistors and Diodes Power Module
2. Thyristors, Triac and Diodes Power Module
3. MOSFETs and Diodes Power Module
4. GTOs (Gate Turn-off Thyristors) and Diodes Power Module.

The connection terminals on the front panel of some of the above mentioned modules are shown in Fig. 3.1. And photographs of some power modules are shown in Fig. 3.2. A generalised power module can be used for making many power converter circuits by interconnecting the front panel terminals, such as: Single-phase AC-DC converter, three-phase AC-DC converter, AC-Regulator, chopper, cycloconverter, inverter, etc.

3.3 INSTRUMENTS

The oscilloscope is used to display voltage waveforms of converter and control circuits. Any current waveform can also be displayed on the oscilloscope by connecting shunt resistor (1 miΩ to 1Ω) in series.

The multi-beam (at least two beams) oscilloscopes are required so that the waveforms at different points of the power converters and control firing circuits can be compared. It is better to use differential oscilloscopes. If differential oscilloscopes are not available, they can be electrically isolated from the converter and its control circuit with the help of 1 : 1 isolation transformer. This isolation or differential feature allows the observation of waveform between any two points of the power circuit. In the absence of any of these features waveforms of any point with respect to earth can only be observed.

The r.m.s. values of the continuous and discontinuous sine waves can be measured directly by electronic multimeter which is now available in the market.

3.4 LOADING ARRANGEMENTS

For study of converters for *R*, *R-L*, and *R-L* and back emf loads one should have
(i) Rheostates of suitable ratings (5*A*, 220*V*)
(ii) Inductances (10 to 100 *mH* and 5*A*)
(iii) Small dc and ac motors (around 0.25 *kW*)

3.5 SAFETY MEASURES

For the safety of the students and control circuit, the control circuit should be isolated from the power converter circuit. Rubber mats on the floor may also be used to avoid shocks.

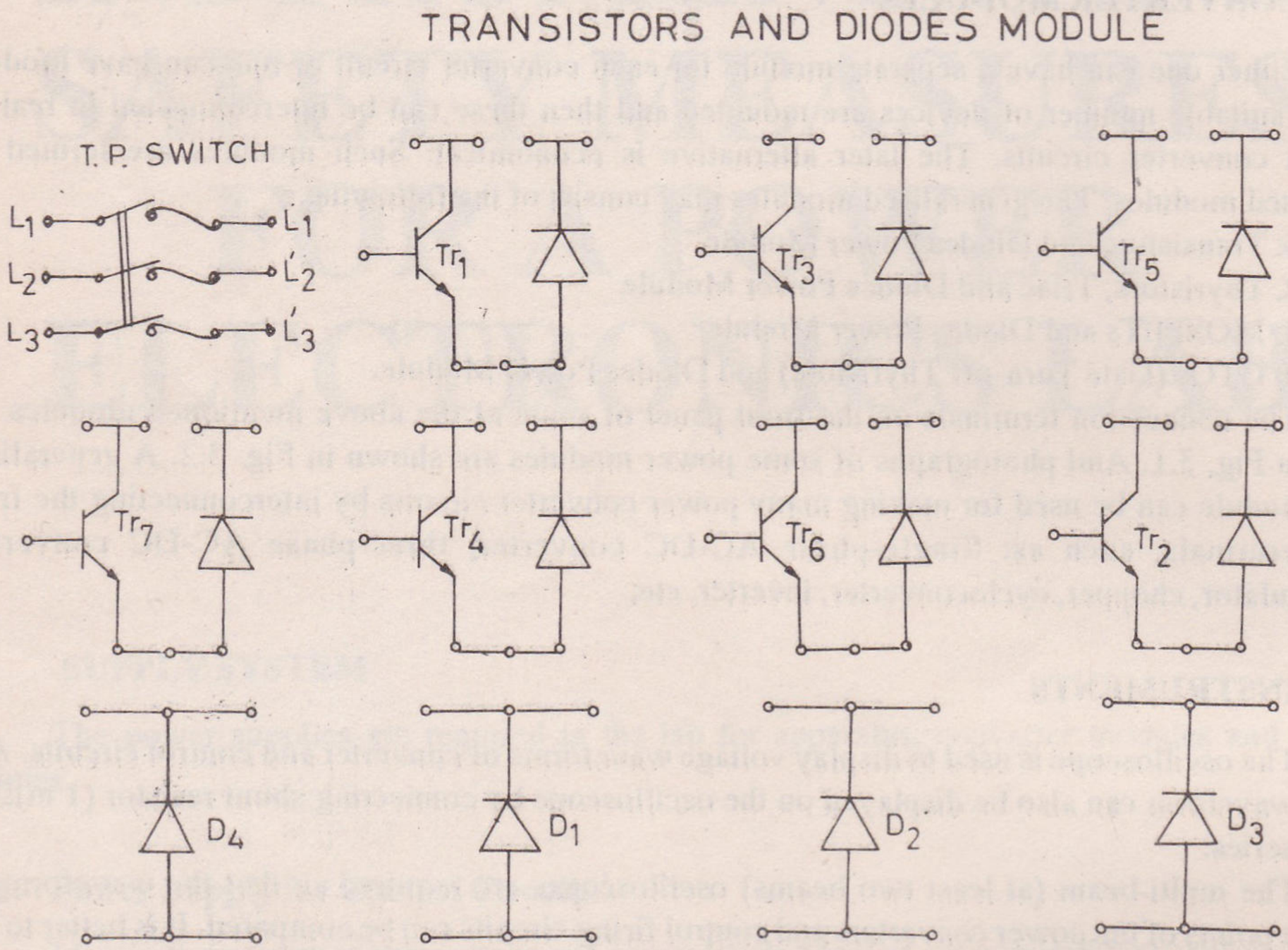


FIG. 3·1(a): FRONT PANEL OF THE POWER TRANSISTORS AND DIODES LAB MODULE (Polarised-snubber is also connected across each transistor)

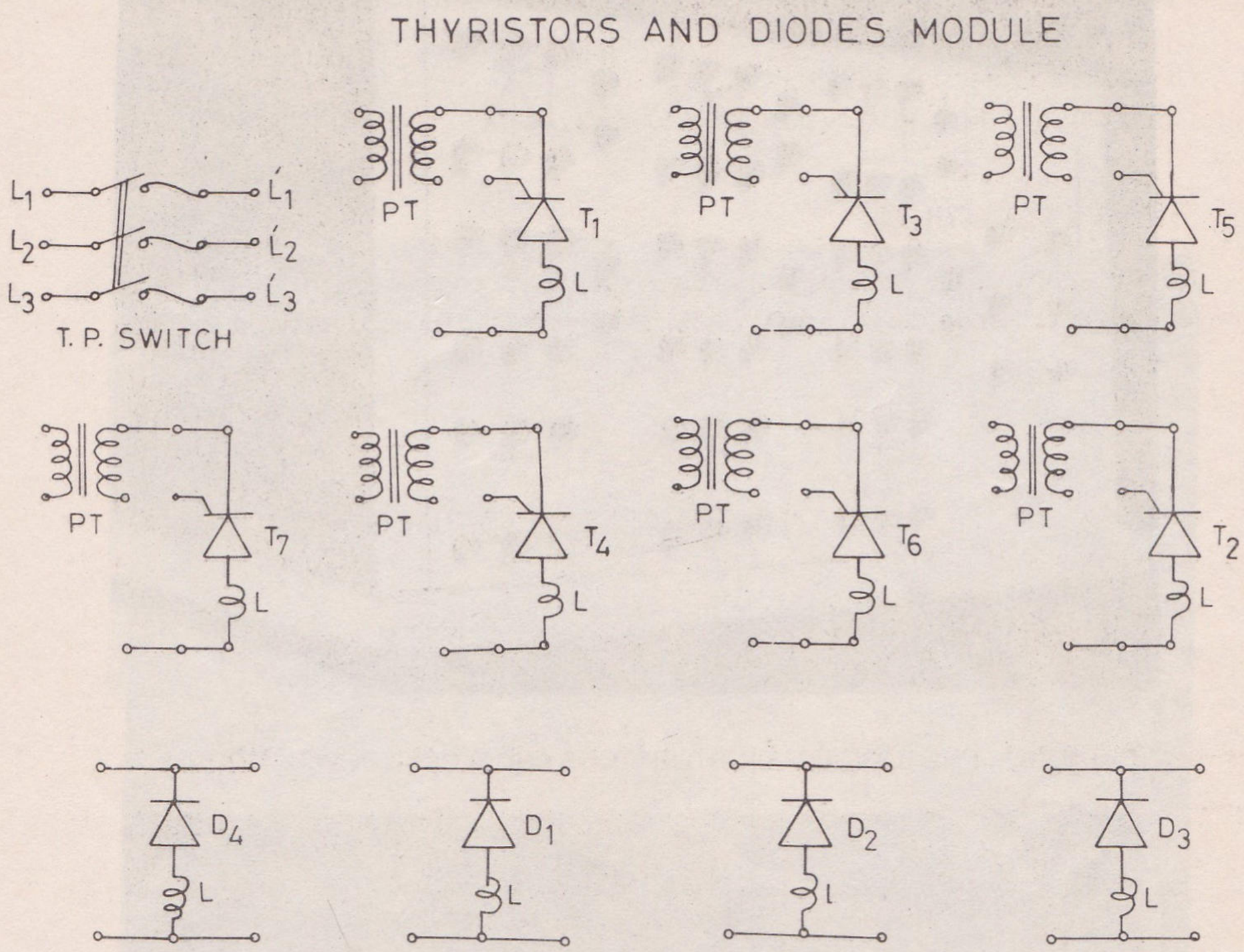


FIG. 3.1(b): FRONT PANEL OF THE POWER THYRISTORS AND DIODES LAB MODULE (Snubber circuits are also connected across thyristors)

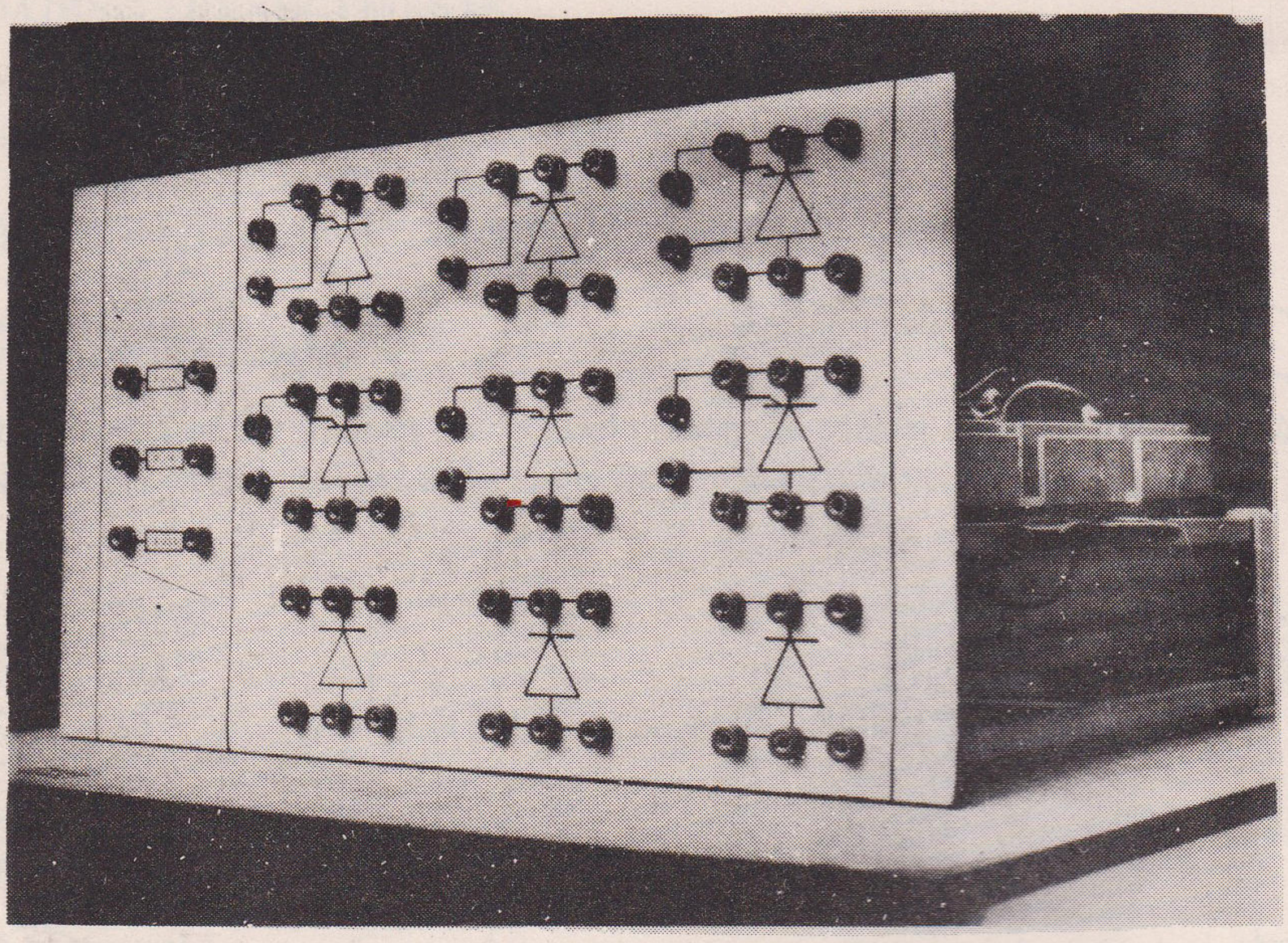


FIG. 3.2(a) : PHOTOGRAPH OF THYRISTORS AND DIODES POWER MODULE

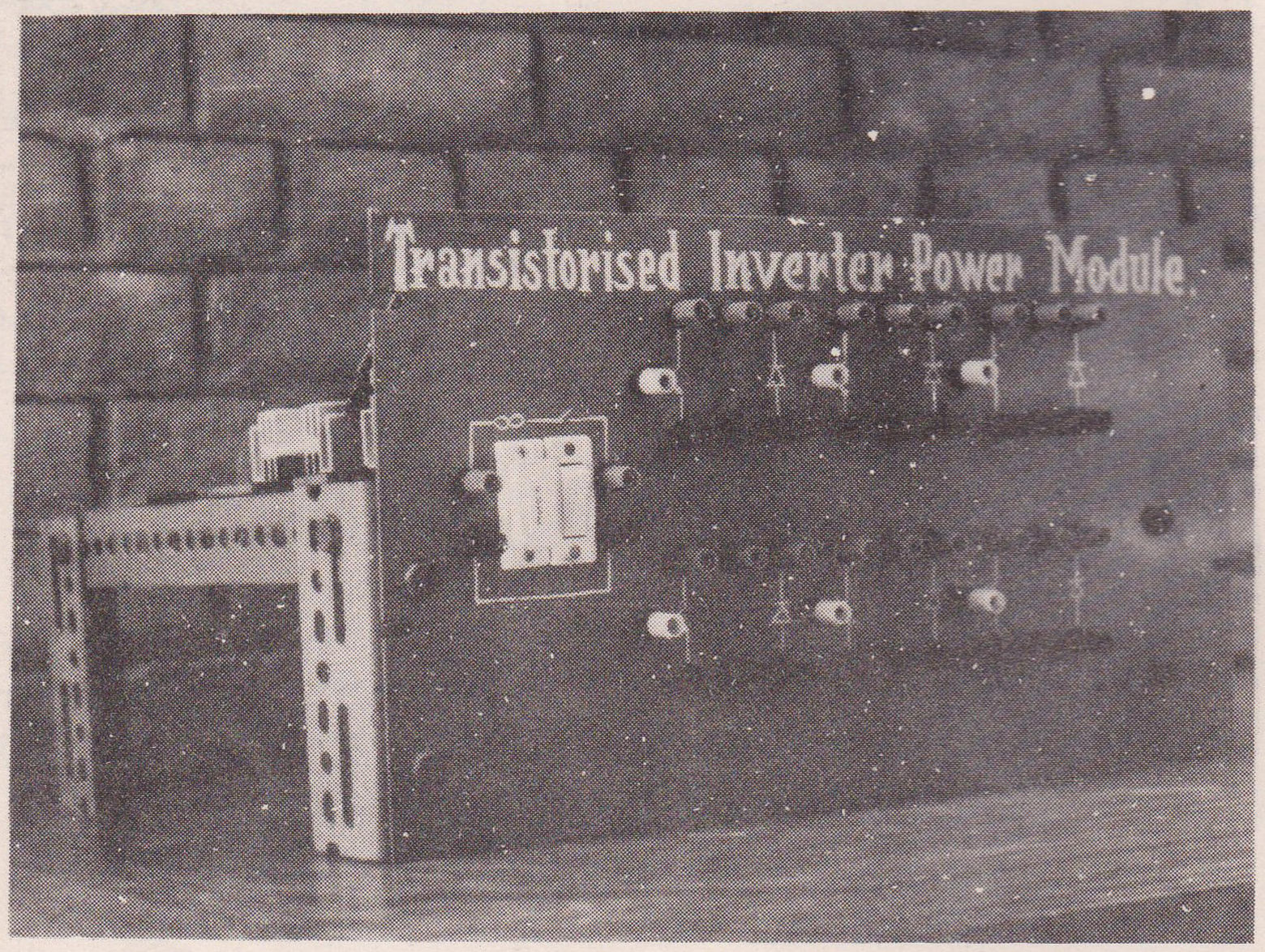


FIG. 3.2(b) : PHOTOGRAPH OF TRANSISTORS AND DIODES POWER MODULE (NEW)

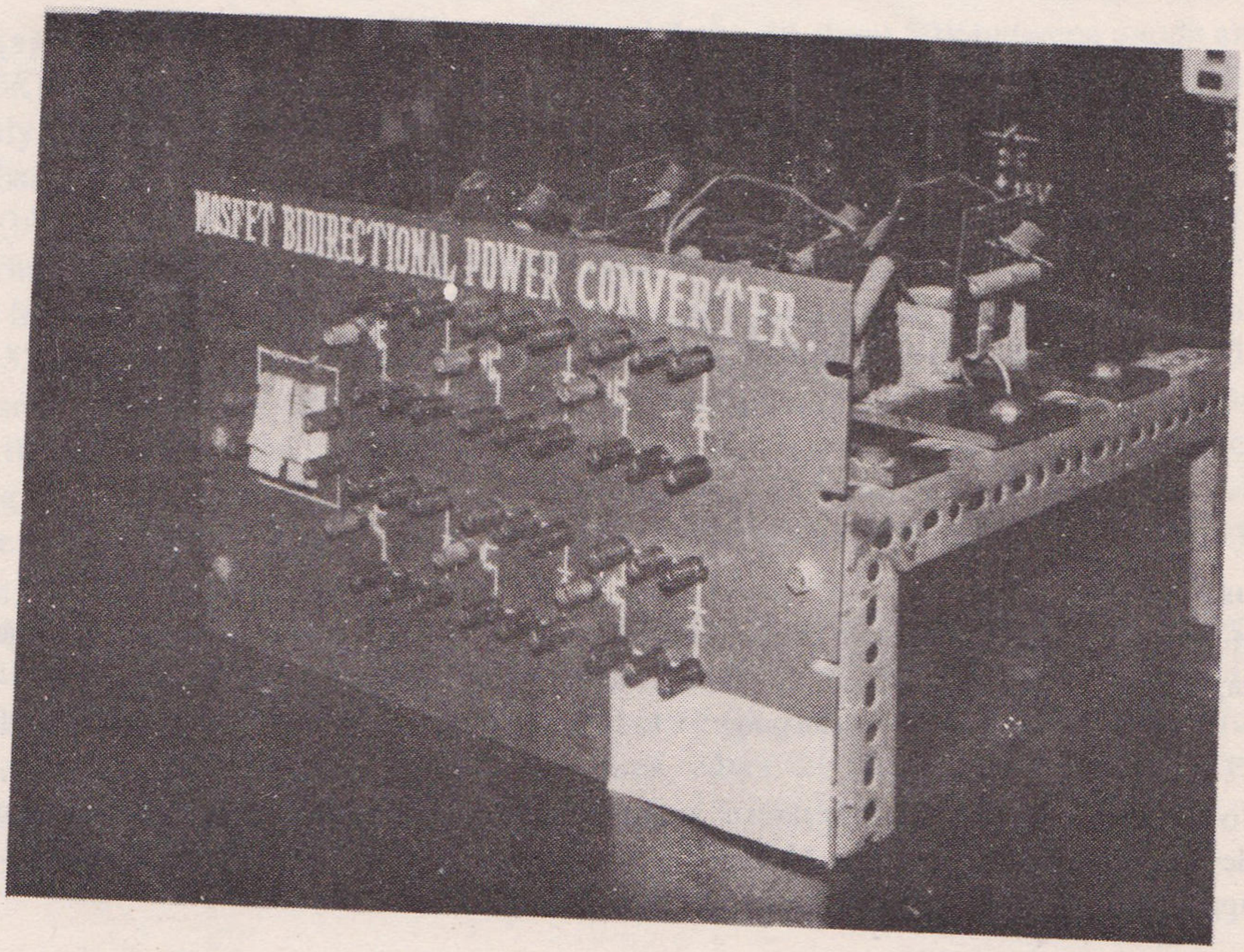


FIG. 3.2(c) : PHOTOGRAPH OF MOSFETs AND DIODES POWER MODULE

4

LAB EXPERIMENTS

Experiment No. 1

Objective : To study the characteristics of a Thyristor and a Triac

Apparatus Required

Multi-beam (at least dual beam) Oscilloscope, Probe 10:1 (if applied voltage is greater than the maximum input voltage range of the oscilloscope), Variable voltage (0-500*V*, 100m*A*) dc power supply, Milliammeter (0-25-50--100 *mA*), Low voltage (between range 5*V* to 15*V*) dc power supply, Transformer (230*V* : 6.3*V*-0-6.3*V*, 500 *mA)*, Thyrsitors and Triac.

[**Note** : You can select the range of instrument according to the rating of the available power semiconductor devices (Thyristors, Diodes, MOSFETs, Transistors, GTO Thyristors, Triacs, etc.). Also see appendix 1 for selecting the range of apparatus.]

Description and Procedure

1.1 Observe the terminal configuration of a thyristor

1.2 To measure the breakdown voltage of a thyristor

1.3 To measure latching and holding current of a thyristor

1.4 To observe V-I characteristics of a thyristor on oscilloscope

1.5 To observe V-I characteristics of a triac on oscilloscope

1.1 OBSERVE THE TERMINAL CONFIGURATION OF A THYRISTOR

Thyristor's body is generally connected with Anode (*A*) terminal by the manufacturers, hence, the anode terminal can be identified with the help of a multimeter. Now, measure the resistance between other two terminals (Gate and Cathode) of the thyristor. The forward-biased p-n junction of a diode shows a low resistance than the reverse-biased junction. When the analog multimeter shows a low resistance then the Gate (*G*) terminal is the one which is connected with positive terminal of the multimeter battery.

1.2 TO MEASURE THE BREAKDOWN VOLTAGE OF A THYRISTOR

Connect the circuit as shown in Fig. 4.1. Use oscilloscope or voltmeter across the thyristor's main terminals (*A* and *K*) for determining the forward and reverse breakover voltages with the gate circuit open. Increase the power supply voltage gradually. As soon as the thyristor breaks, oscilloscope shows nearly zero voltage drop across the thyristor. Reduce the voltage immediately.

1.3 TO MEASURE LATCHING AND HOLDING CURRENT

(a) Assemble the circuit as shown in Fig. 4.2. Apply about 50*V* between anode and cathode. Keep 33*K* pot at the minimum resistance position. The device must be in the off state with open gate. Gradually increase the gate supply voltage by varying the position of 10*K* pot. Do not go beyond 10V. Observe the minimum gate current (I_{gmin}) required to turn on the device.

(b) Adjust the gate voltage to a slightly higher value than what is found in (a). Set 33*K* pot at the maximum resistance position. The device must be in the off state, otherwise decrease the supply voltage from 50*V* gradually. The gate voltage should be kept constant in this experiment. With the help of 33*K* pot, gradually increase the anode current (I_a) in steps, each step may be of 1 *mA*. Open and close the gate switch after each step. If anode current is greater than the latching current of the device, then the device stays on even after the gate switch is opened. Otherwise the device goes into blocking mode as soon as the gate switch is opened. Note the value of latching current. Obtain more accurate value of the latching current (I_l) by taking 0.25 *mA* steps of the anode current (I_a) near the latching current value already obtained.

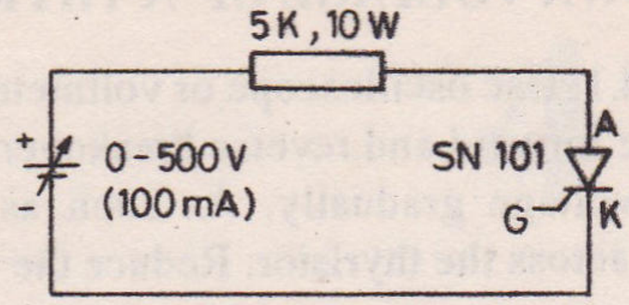
(c) Increase the anode current from the latching current level with 33*K* pot or by increasing slightly the supply voltage. Open the gate switch permanently. The thyristor must be fully on. Now start reducing the anode current gradually by adjusting the 33*K* pot. If thyristor does not turn off even after the pot is at the highest resistance value, then reduce the anode supply voltage. Observe when the device goes into blocking mode. The anode current through the device at this instant, is the holding current (I_h) of the device.

1.4 V-I CHARACTERISTICS OF A THYRISTOR

Connect the circuit as shown in Fig. 4.3. Use the oscilloscope in the *X-Y* input mode by disconnecting the internal time base and *X*- plate and *Y*-plate are connected with external signals. The point *A* is connected to Horizontal Input terminal (*X*-plate), *B* to Vertical Input terminal (*Y*-plate) and *C* to common terminal of *X-Y* plate (T_{X-Y}; generally connected with the body of the oscilloscope). Set the pot in gate circuit to a suitable value. Use the 12.6*V* ac supply provided on the board. Observe the trace on the oscilloscope screen. This is the *V-I* characteristic of the thyristor. The forward break-over voltage can be adjusted by changing the setting of the pot in the gate circuit.

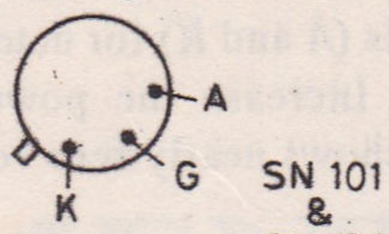
1.5 V-I CHARACTERISTIC OF A TRIAC

Assemble the circuit shown in Fig. 4.4. Connect the oscilloscope in *X-Y* input mode as shown. Observe *V-I* characteristic of the triac on the oscilloscope. Change the gate current by adjusting the 10*K* pot and observe the effect on triggering.



Thyristor SN 101 has voltage rating of 100V and current rating of 1A

Low power Thyristor terminal configuration



Top View

FIG.4.1: CIRCUIT FOR MEASURING FORWARD BREAKOVER VOLTAGE WITH GATE OPEN

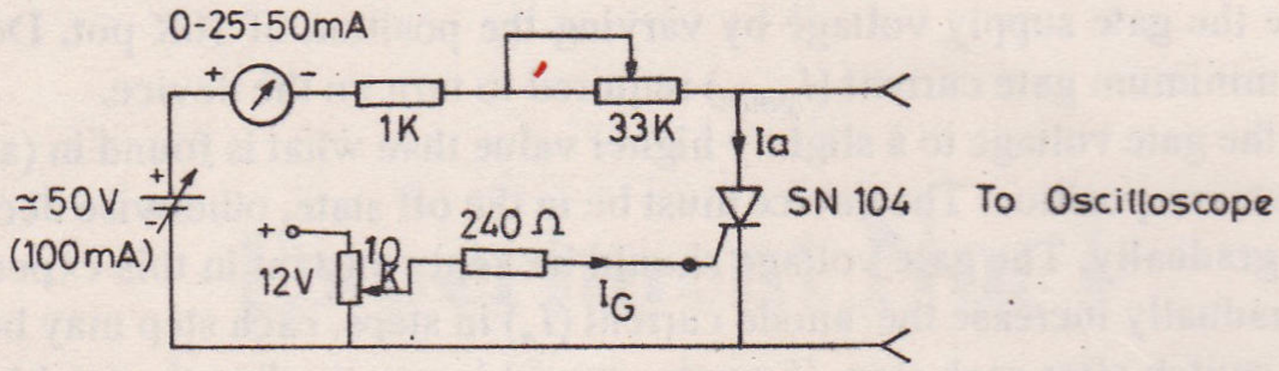
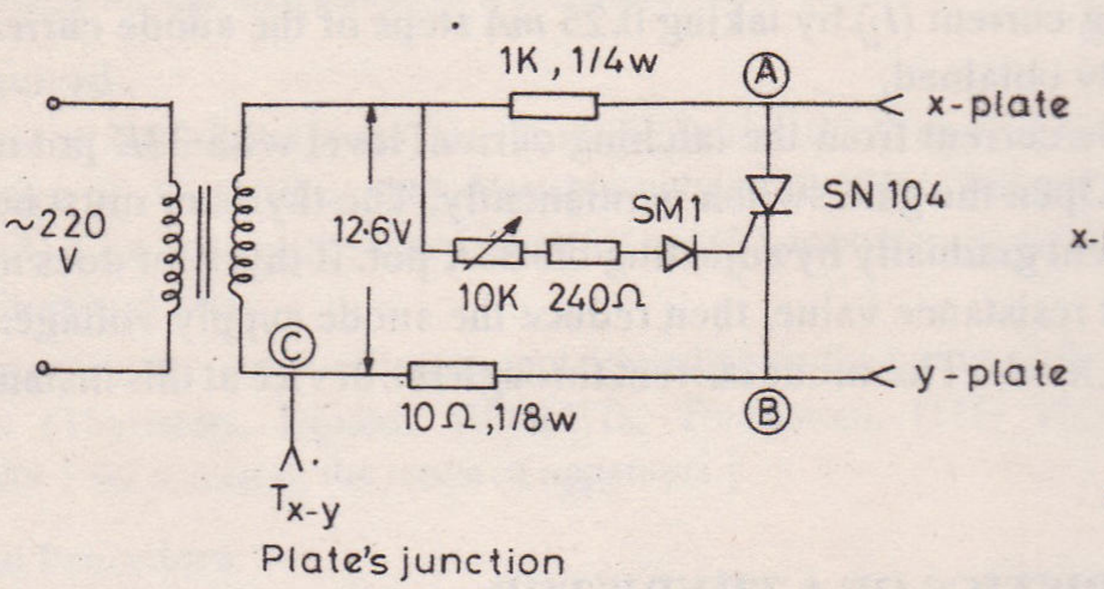


FIG.4.2: CIRCUIT FOR MEASURING LATCHING AND HOLDING CURRENT



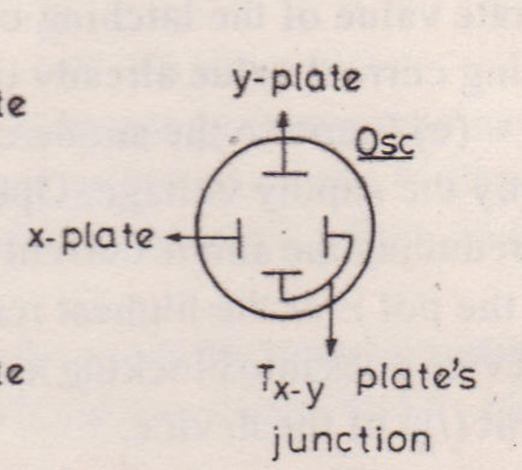
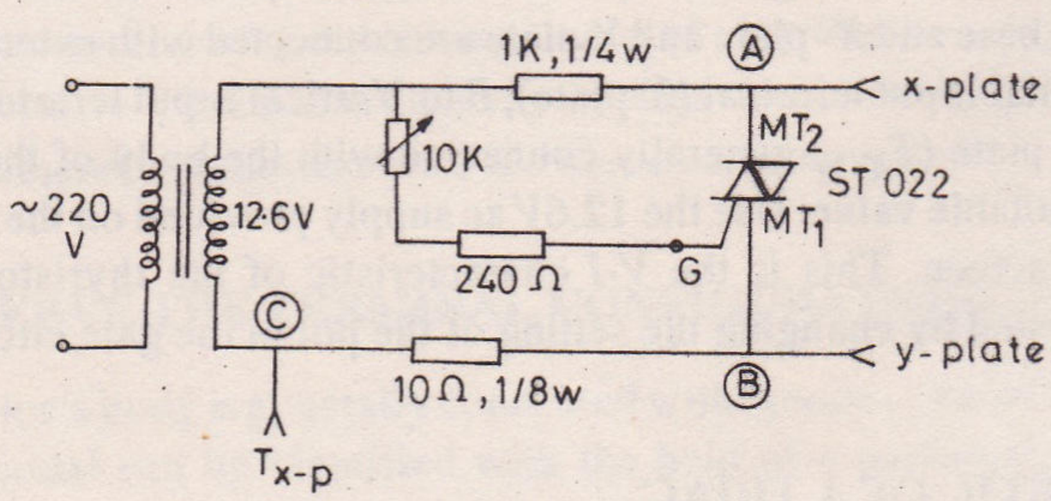
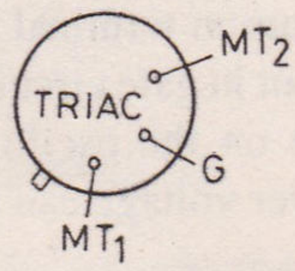


FIG.4.3: MEASUREMENT OF THE V-I CHARACTERISTICS OF A THYRISTOR



Low power triac terminal configuration



TOP VIEW

FIG.4.4: MEASUREMENT OF THE V-I CHARACTERISTIC OF A TRIAC

QUESTIONS

1.1 Fill in the blanks :

(i) Thyristor is a_____ layers and_____ junctions device.

(ii) The other name of the thyristor is_____.

(iii) Thyristor is a_____ terminals device and the name of the terminals are_____, _____, _____.

(iv) Generally,_____ terminal is connected with the body of the thyristor.

(v) The resistance between Anode and Cathode and between Anode and Gate is _____.

(vi) The resistance between Cathode and Gate is _____than the resistance between Anode and Cathode.

(vii) The ohm meter (or multimeter) shows_____ resistance when *p-n* junction between Gate and Cathode of a thyristor in reverse-biased than the resistance when the same *p-n* junction in forward-bias.

(viii) The voltage across the thyristor becomes_____ as soon as it turned ON.

(ix) Generally, the reverse breakdown voltage of a thyristor is_____ than the forward breakover voltage.

(x) For the normal operation of a thyristor, the supply voltage must be _____ than breakover voltages (forward and reverse breakover voltage.).

(xi) Generally, the holding current of a thyristor is_____ than its latching current.

(xii) A thyristor is a_____ device while triac is a _____device (unidirectional/bidirectional).

(xiii) A thyristor is turned off when the anode current reduces to_____ value.

(xiv) The forward breakover voltage_____ with increase in the gate current.

(xv) The thyristor is mounted on the_____ for radiating excess heat of the device.

1.2 What are the conditions for operating a thyristor in the normal operation?

1.3 Explain the holding current and latching current of a thyristor.

1.4 What is the difference between a diode and a thyristor?

1.5 What are the typical voltages drops across conducting thyristor, triac and diac ?

1.6 What is the relation between gate current and anode current of a thyristor in conduction period?

1.7 What are the differences between an ordinary switch and a semiconductor switch (such as thyristor, triac, bipolar transistor, MOSFET or GTO thyristor, etc.)?

Experiment No. 2

Objective : To study the differènt Triggering Circuits for Thyristors

2.1 : Resistor (R) Triggering Circuit

2.2 : Resistor-Capacitor (R-C) Triggering Circuit

2.3 : Uni-junction Transistor (UJT) Triggering Circuit (UJT Relaxation Oscillator)

2.4 : Half-wave Controlled Rectifier

2.5 : Full-wave Controlled Rectifier

Apparatus Required

Dual beam oscilloscope, fabricated R-triggering circuit, R-C triggering circuit and UJT-triggering circuit, thyristor and diode lab module, pulse transformer, potential transformers; See appendix 1 for selecting the range of apparatus.

Description and Procedure

2.1 R-TRIGGERING CIRCUIT

The circuit is shown in Fig. 4.5. Connect the oscilloscope across the thyristor. The firing angle (α) of the thyristor can be varied by varying the gate current by 2.2K pot. Observe the variation in the load voltage as the 2.2K pot is varied. If thyristor's triggering-angle cannot be varied from about 0° to $\frac{\pi}{2}$ then replace 2.2K pot with 10K or 22K pot. In this circuit, the synchronized firing angle can be obtained easily and economically in the positive half-cycle of the supply. But there is a drawback that the firing angle can be controlled at the most at 90°, because the gate current is in phase with the applied voltage. A resistor R_g is connected in the gate circuit, so that the gate current does not cross the maximum permissible value I_{gmax}. The value of R_g can be calculated by the following equation

$$R_g \geq E_m / I_{gmax}$$

where E_m = Peak value of the supplied ac voltage.

2.2 R-C TRIGGERING CIRCUIT

The circuit is shown in Fig. 4.6. A capacitor (C) is connected in the thyristor's gate circuit for shifting the phase of the gate voltage. The capacitor is charged through diode D_2 upto the negative peak value of the applied voltage and it is discharged through pot R_c, resistor R_f and supply e. The value of R_c, R_f and C are chosen in such a way that the negatively charged capacitor can be discharged fully and charged in the positive direction upto V_{gmin} between 0° to $\frac{\pi}{2}$ of the positive half cycle. The discharging rate of the capacitor is controlled by the pot R_c.

The maximum firing angle delay is about $\frac{\pi}{2}$. Observe the voltage across thyristor and load. Also observe the variation in the capacitor voltage with respect to the thyristor voltage as the R_c pot is varied and note the minimum and maximum values of the firing angle.

2.3 UJT TRIGGERING CIRCUIT (UNIJUNCTION TRANSISTOR RELAXATION OSCILLATOR)

Make the connection as shown in Fig. 4.7(a). The charging rate of the capacitor (C) is varied as the R_c pot is varied. When capacitor voltage reaches the threshold voltage (ηV_{bb}) of the UJT, the UJT is turned on. The capacitor discharged quickly through the pulse transformer. And a pulse (V_g) is produced at the secondary of the pulse transformer in every discharging period of the capacitor. These output pulses of the relaxatien oscillator, as this UJT circuit is commonly known, are synchronised with respect to the applied ac voltage and are used for firing thyristors. The pulse transformer provides isolation between the power and firing circuits. The angle between the initial point of a half-cycle and the first pulse in a half-cycle, is the firing angle of the thyristor. Other pulses in the half-cycle have no effect because once a thyristor is turned on, it can be turned off only after the anode-current reaches below the holding current of the thyristor.

Observe the voltage waveforms at point B and D with respect to point A. Also observe the voltage waveform at point G with respect to point D. It can also be observed that the period t between the pulses in a half-cycle is approximately given by RC, where R is the total resistance $(R_c + R_f)$ of the charging circuit. Since

$$t = RC \log e^{[1/(1-\eta)]}$$

where $\eta \rightarrow$ intrinsic stand-off ratio of the UJT. It generally, varies from 0.65 to 0.8.

If $\eta = 0.65$ then $t \simeq RC$.

Two essential requirements are given below to ensure that the firing pulses of a UJT firing circuit, can fire the thyristor.

1) The stored capacitor energy (P_c) at the instant of the switching of the UJT, must be greater than the minimum energy required by the gate-cathode junction for firing the thyristor.

$$P_c = \frac{1}{2} C V_c^2 = \frac{1}{2} (\eta V_{bb})^2 C$$

2) And total charging resistance R $(= R_C + R_f)$ of the capacitor must satisfy the equation

$$\frac{V_{bb} - V_p}{I_p} \geq R \geq \frac{V_{bb} - V_v}{I_v}$$

where

V_p: Emitter voltage at peak point in the UJT characteristics

I_p : Emitter current at peak point in the UJT characteristics

V_v : Emitter voltage at valley point in the UJT characteristics

I_v : Emitter current at valley point in the UJT characteristics

V_{bb} : Applied dc voltage at base-2 (B_2) of the UJT.

The μJT–characteristics is also discussed in article 3 of appendix 3.

2.4 SINGLE-PHASE HALF-WAVE CONTROLLED RECTIFIER

Now connect the half-wave controlled rectifier circuit as shown in Fig. 4.8. Use the thyristor from the generalised thyristor-triac module of the lab. Keep the rheostat resistance at sufficiently large value. Switch on the ac power supply. Now apply the gate pulses from the output winding of the pulse-transformer of the UJT triggering circuit. Observe the thyristor and load voltage waveforms with respect to the input voltage for various firing angles.

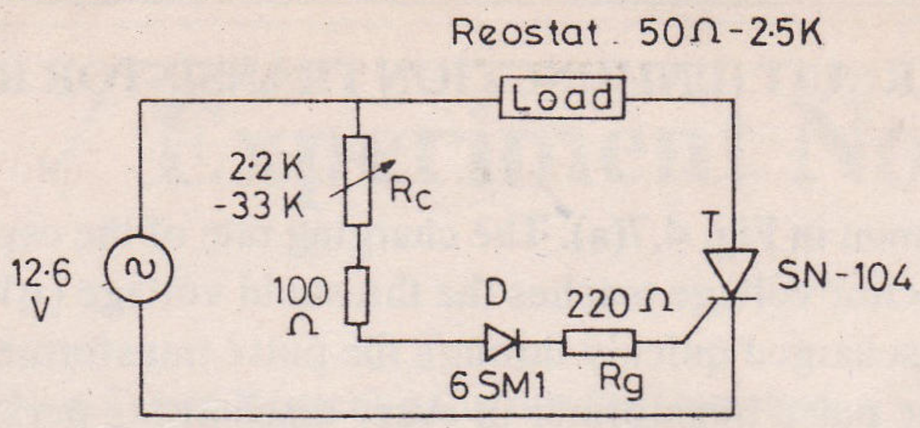


FIG.4·5: R-TRIGGERING CIRCUIT

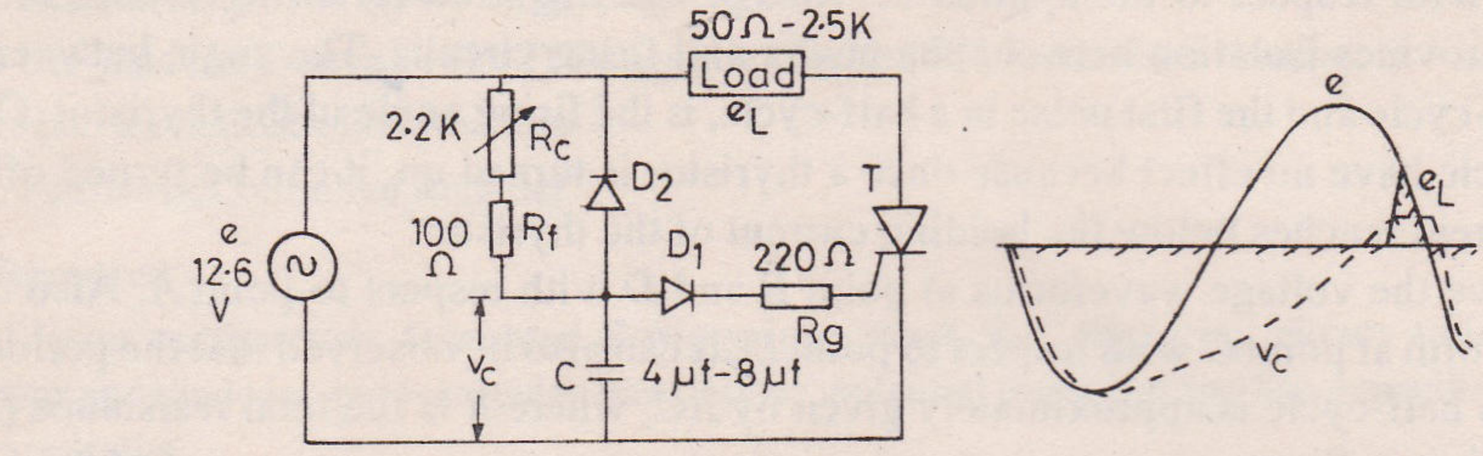
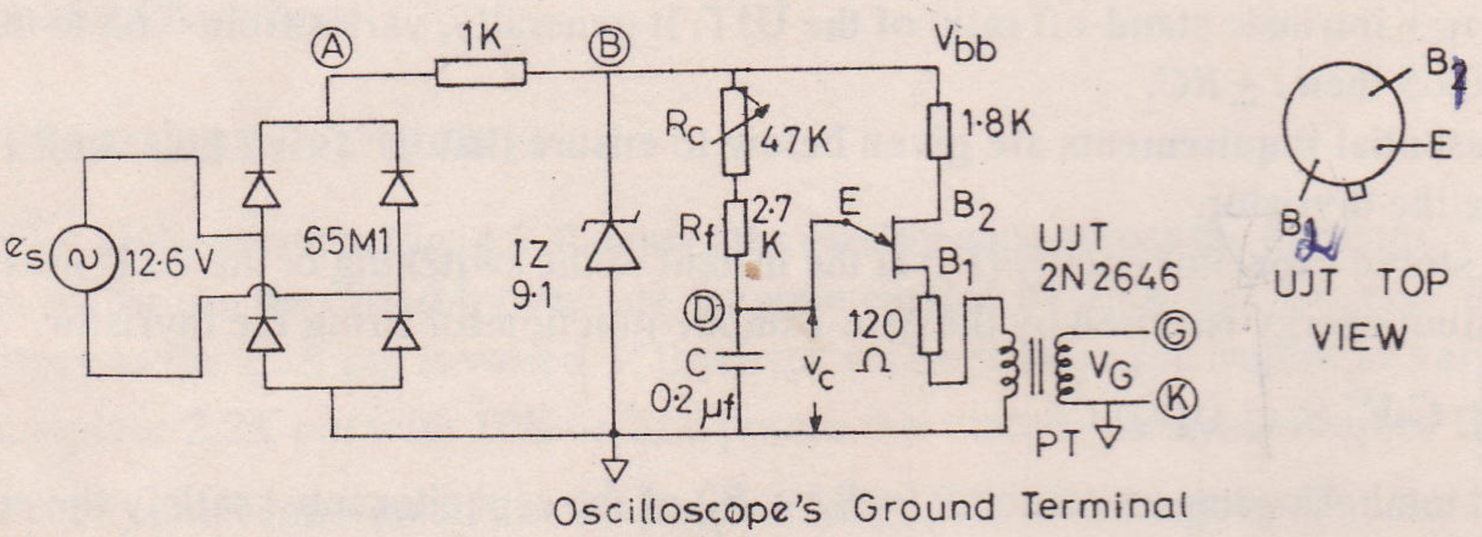
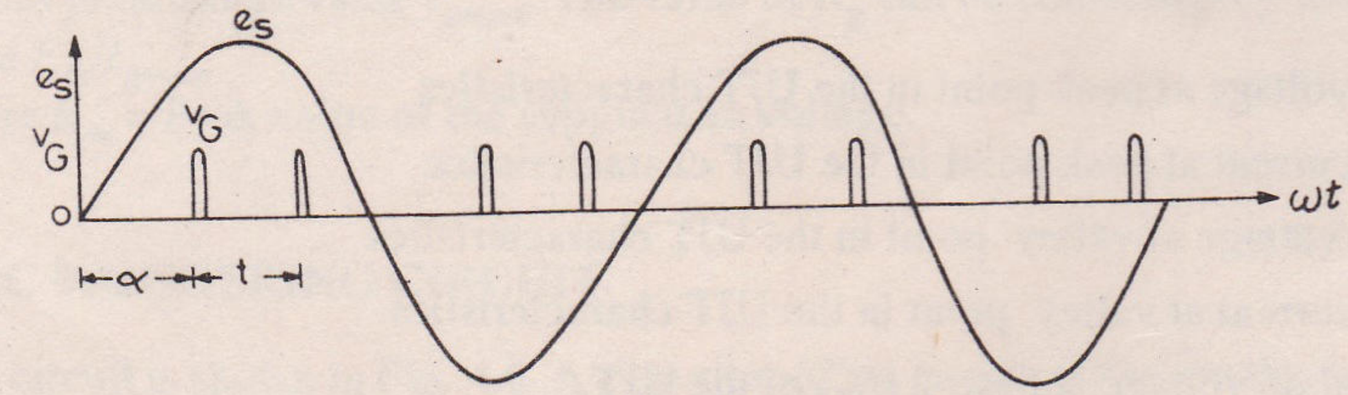


FIG.4·6: R-C TRIGGERING CIRCUIT



(a) UJT-FIRING CIRCUIT



(b) Waveforms at different points of UJT

Triggering circuit (a)

FIG.4·7: UJT TRIGGERING CIRCUIT WITH WAVEFORMS

2.5 SINGLE-PHASE FULL-WAVE CONTROLLED RECTIFIER

Next connect the full-wave controlled rectifier circuit of Fig. 4.9, employing one thyristor and four diodes. Repeat the steps of the previous paragraph.

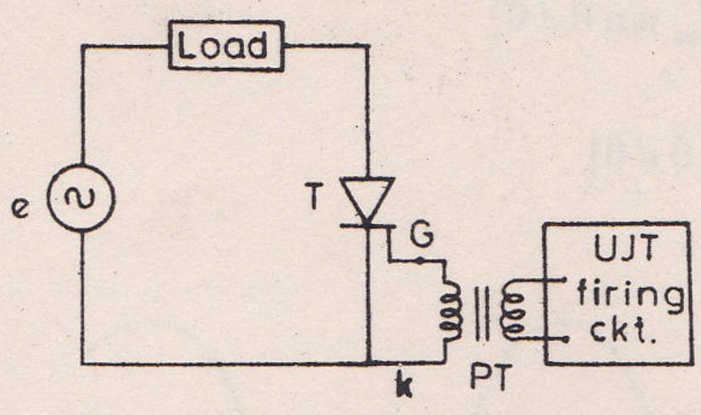


FIG.4-8 : HALF WAVE CONTROLLED RECTIFIER

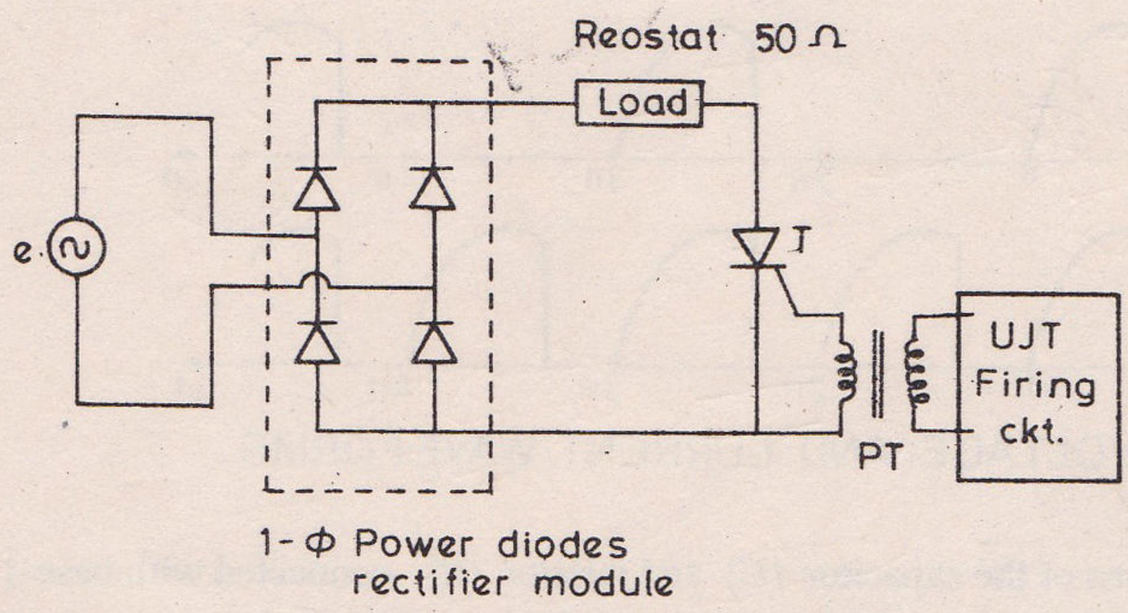


FIG.4-9 : FULL-WAVE CONTROLLED RECTIFIER

QUESTIONS

2.1 What is the meaning of triggering circuit (also called firing circuit or control circuit) of a thyristor or a triac?

2.2 Draw and explain the *V*-I characteristic of a UJT (Unijunction Transistor).

2.3 What is the "intrinsic ratio (h)" of a UJT and what is its typical value?

2.4 Draw and explain *V*-I characteristic of a triac. Why is a diac preferred to trigger a triac?

2.5 Find the equation of average voltage or current for the following waveforms shown in Fig. Q. 2.5.

[**Hint** : V_{av} (Half-wave) $= \frac{1}{2\pi}\int_{\alpha}^{\pi} V_m \sin\theta \, d\theta$]

and V_{av} (Full-wave) $= \frac{1}{\pi}\int_{\alpha}^{\pi} V_m \sin\theta \, d\theta$]

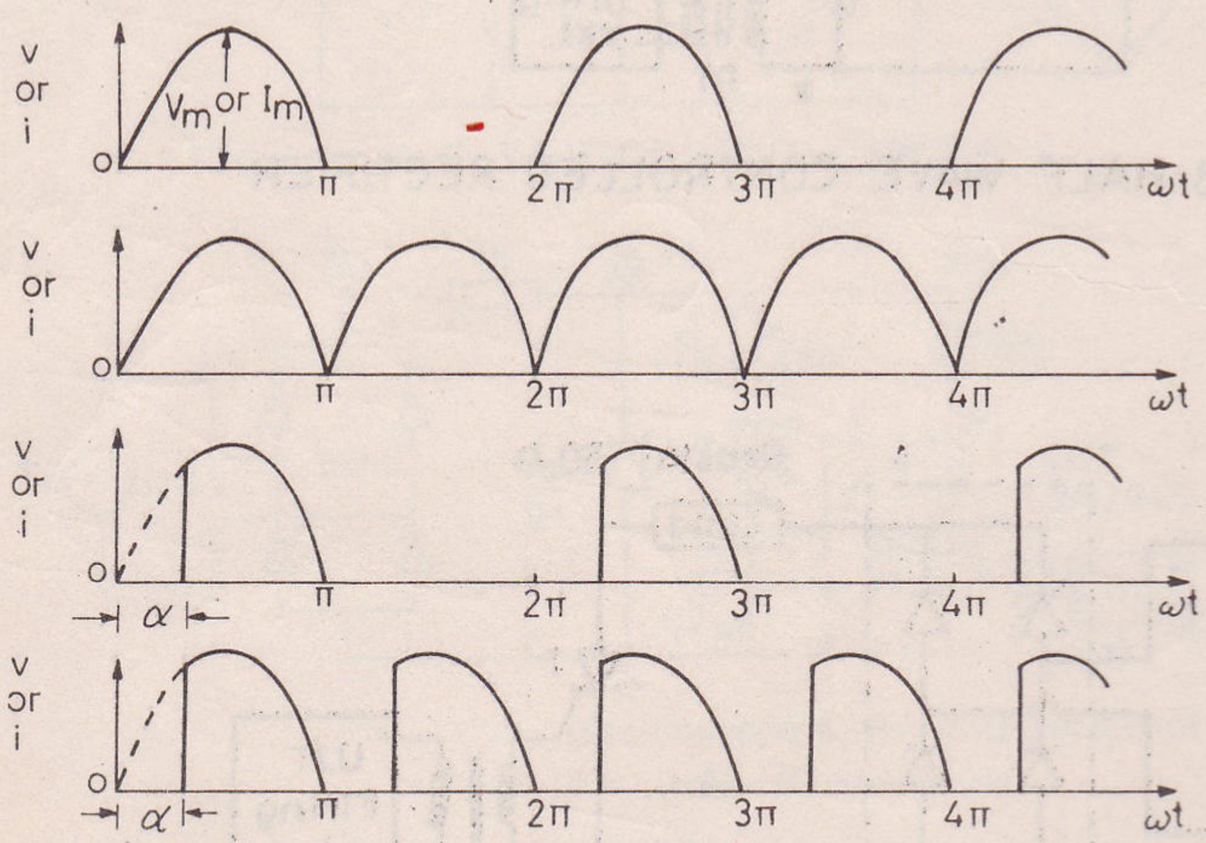


FIG.Q.2.5: VOLTAGE AND CURRENT WAVEFORMS

2.6 Draw the voltage waveforms of the capacitor (C) and resistor (R), connected with base-1 (B_1) and also calculate the amplitude and frequency of the oscillations of the capacitor voltage for relaxation oscillator circuit shown in Fig. Q.2.6 (let $R_1 = 0\Omega$ and η of UJT = 0.65).

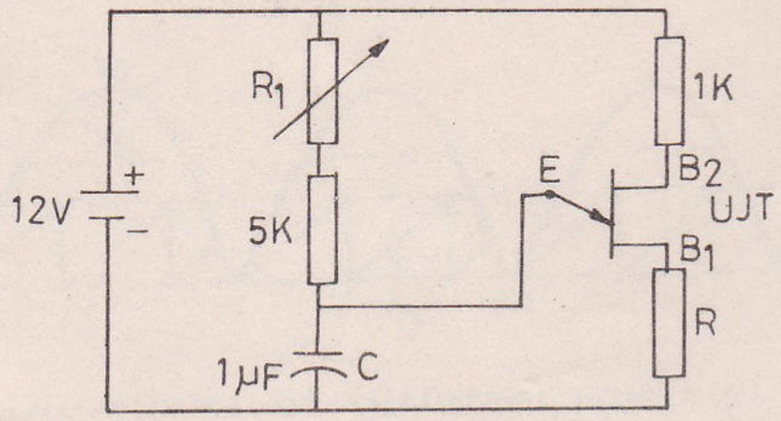


FIG.Q.2.6: RELAXATION OSCILLATOR CIRCUIT

2.7 Fill in the blanks :

(i) The triggering angle (α) can be controlled from _____ to _____ with *R*-triggering circuit.

(ii) The triggering angle (α) can be controlled from _____ to about _____ with *R-C* triggering circuit.

(iii) The UJT is turned-on when emitter voltage becomes equal to _____

(iv) The frequency of oscillation of the saw-tooth wave can be changed by varying the _____ in circuit of Fig. Q. 2.6.

Experiment No. 3

Objective : To study single-phase Firing Circuits suitable for Triggering Thyristors in a single-phase AC voltage Controller or Converter.

3.1 : Firing Circuit using ramp-comparator scheme

3.2 : Firing Circuit using cosine-wave scheme

3.3 : Firing Circuit using op-amps and gates

3.4 : Digital firing circuit

Apparatus Required

Dual beam oscilloscope, Fabricated firing circuits, Variable voltage (0 to ± 18*V*, 1*A*) or (fixed voltage between ± 10*V* to ± 15*V*, 1*A*) power supply for op-amps and CMOS *IC*s.

3.1 FIRING CIRCUIT USING RAMP-COMPARATOR SCHEME

Description

Make firing-circuit as shown in Fig. 4.10(a). The operation of the circuit is explained illustrating pertinent waveforms in Fig. 4.10(b). This circuit is very simple and requires less and easily available components. The zero-crossover-detector (ZCD) (Fig. 4.10(a)), which uses operational amplifier, transforms the synchronising signal (e) into a square wave signal (A) as shown in Fig. 4.10(b). The negative pulses are eliminated by using diodes at the output stage of each op-amp. The 1st Exclusive-OR gate (Pin Nos. 11, 12 & 13 of IC 74C86) is used as an inverter (one can also use NOT gates IC 74C901). The waveform $\bar{A}$ is obtained at the output of the inverter. The waveform $\bar{A}$ is given to the delay circuit (R-C integrator circuit) and the waveform B is obtained across the capacitor of the delay circuit.

The waveforms B and $\bar{A}$ are fed to the input terminals of EX.OR gate and the waveform C is obtained at the output of EX.OR gate. If EX.OR gate is not available then one can make EX.OR gate with the help of two NOT gates, two AND gates and a OR gate satisfy the following equation :

$$C = \bar{A} \oplus B = A\,\bar{B} + \bar{A}\,B$$

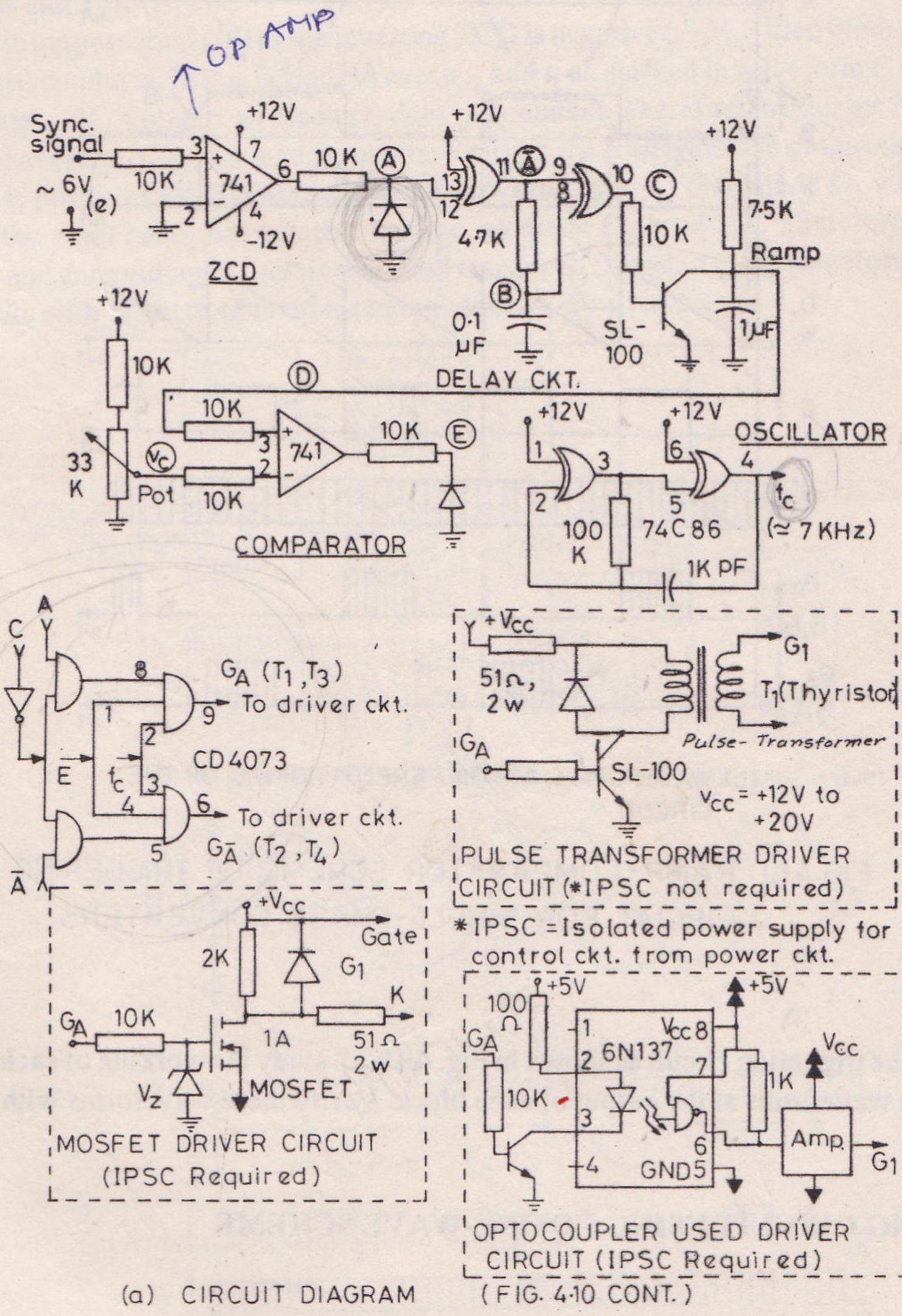
This C waveform is used for resetting the ramp-generator.

The comparator compares the ramp (D-waveform) with a dc voltage v_c which varies between 0 about +10*V* (when v_{cc} = +12*V*) and is controlled by the 33*K* Pot. The output of the comparator (waveform E), is used for triggering thyristors.

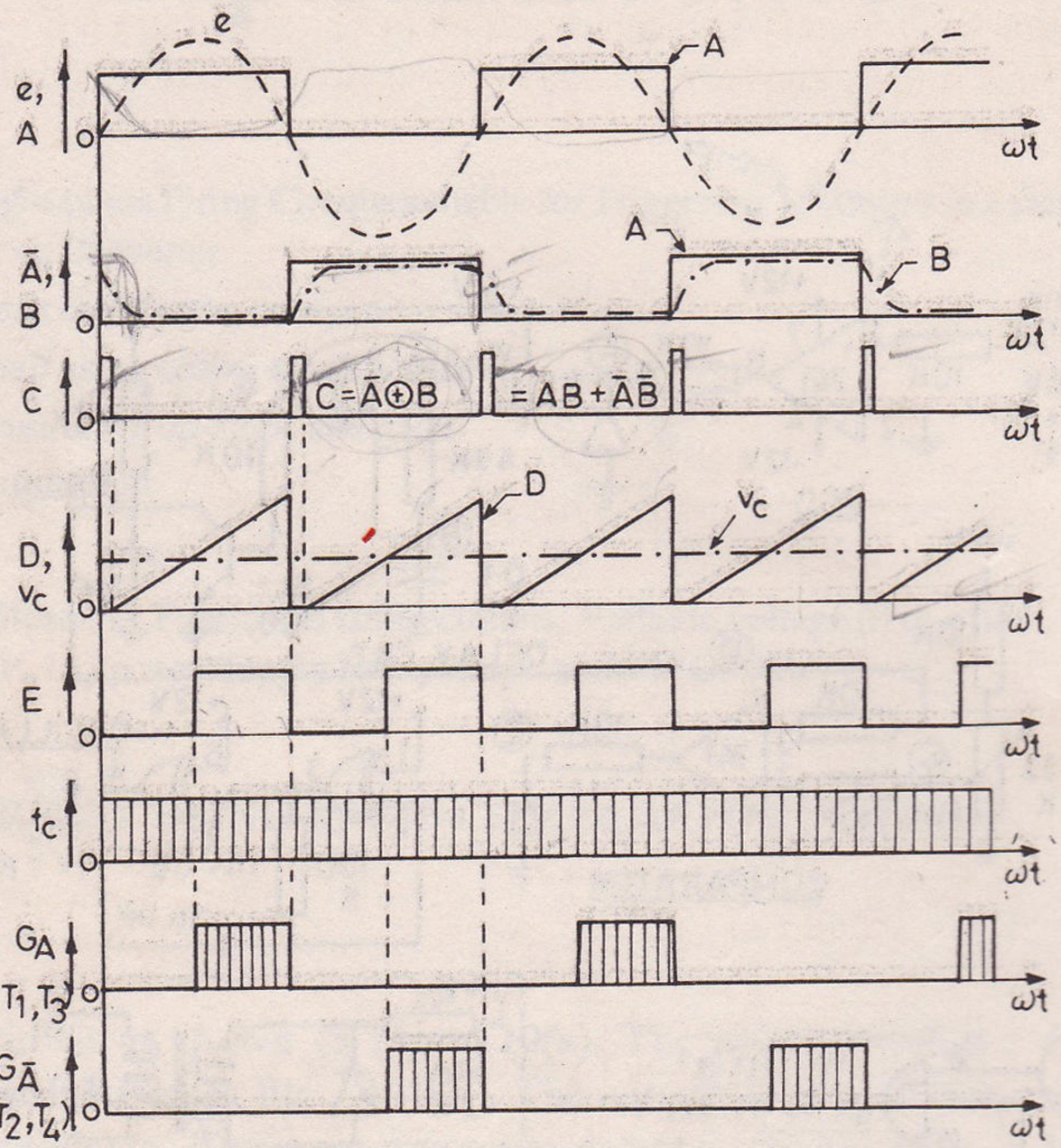
Generate carrier frequency f_c from an oscillator as shown in Fig. 4.10(a). Here EX.OR gates are used as ordinary NOT gates.

The waveform E is ANDed with A and $\bar{A}$ separately. These waveforms are also modulated by high frequency pulses f_c ($\simeq$ 7 *KHz*). The high frequency switching is essential to reduce thyristor's gate power dissipation and size of pulse transformer. Waveforms G_A and $G_{\bar{A}}$ are fed to the separate driver circuit which are also called pulse amplification and isolation stages. Three types of driver circuits (pulse-transformer and transistor driver circuit, MOSFET driver circuit and optocoupler

driver circuit) are given in Fig. 4.10(a), you can choose any one driver circuit. But pulse-transformer and transistor driver circuit can be handled easily and are more reliable.



(a) CIRCUIT DIAGRAM (FIG. 4.10 CONT.)



(b) WAVEFORMS AT DIFFERENT POINTS OF THE CIRCUIT

FIG.4.10: RAMP-COMPARATOR SCHEME OF TRIGGERING CIRCUIT FOR SINGLE-PHASE CONVERTERS

Procedure

Make the triggering circuit as shown in Fig. 4.10(a). study the working of each block. Observe and note down waveforms at the output of each block. Varify these waveforms with those shown in Fig. 4.10(b).

3.2 FIRING CIRCUIT USING COSINE-WAVE SCHEME

Description

Figs. 4.11(a), 4.11(b) and 4.11(c) show block diagram, waveforms at different stages of the block diagram and circuit diagram of the cosine-wave scheme for generating triggering pulses. The low voltage ($\simeq 6V$) synchronising signal is fed to non-inverting ZCD (Zero-Crossover Detector), inverting ZCD and a integrator (90^o phase-shifter). Each ZCD transforms the synchronising signal into a square wave signal, with $+V_{cc}$ and $-V_{cc}$ voltages, which is used for switching the transistor. Waveforms A and $\bar{A}$ are also obtained at the outputs of the ZCDs as shown in Fig. 4.11(c).

The two stage *R-C* phase-shifter is shown in the circuit. Adjust the 10*K* preset pot (*Pr*) in such a position that the output of the phase-shifter (waveform *B*) is shifted by 90°. This waveform *B* is also called cosine-wave with respect to the input voltage *e*. The op-amp inverter amplifier (Ist Amplifier) inverts and amplifies the waveform *B* into the waveform *B*. The waveform *B* is fed to another op-amp inverting amplifier (IInd Ampl.) and to the Ist transistor switch (Tr. SW_1) through series connected resistors of 4.7*K* and 10*K* (R_1).

When the output signal (*IZ*) of the inverting ZCD is negative ($-V_{cc}$) then diode D_1 (connected in Tr. SW_1 circuit) conducts. In this period (between t_2 and t_1 as marked in waveform *C* of Fig. 4.11(b), the Bas_1 point has $-V_{cc}$ voltage, so diode D_2 does not conduct. Therefore, transistor Tr_1 is off in this period and the waveform-*C* is obtained across the Resistor R_1. And when the output signal (*IZ*) of the inverting ZCD is positive ($+V_{cc}$) (duration period between t_3 and t_2) then diode D_1 will not conduct. In this period, the point $base_1$ has positive voltage, so diode D_2 conducts. Therefore, the transistor Tr_1 will be ON and zero voltage is obtained across resistor R_1. Similarly, the waveform *C* is obtained across resistor R_2 with the help of the transistor switch *Tr.* Sw_2.

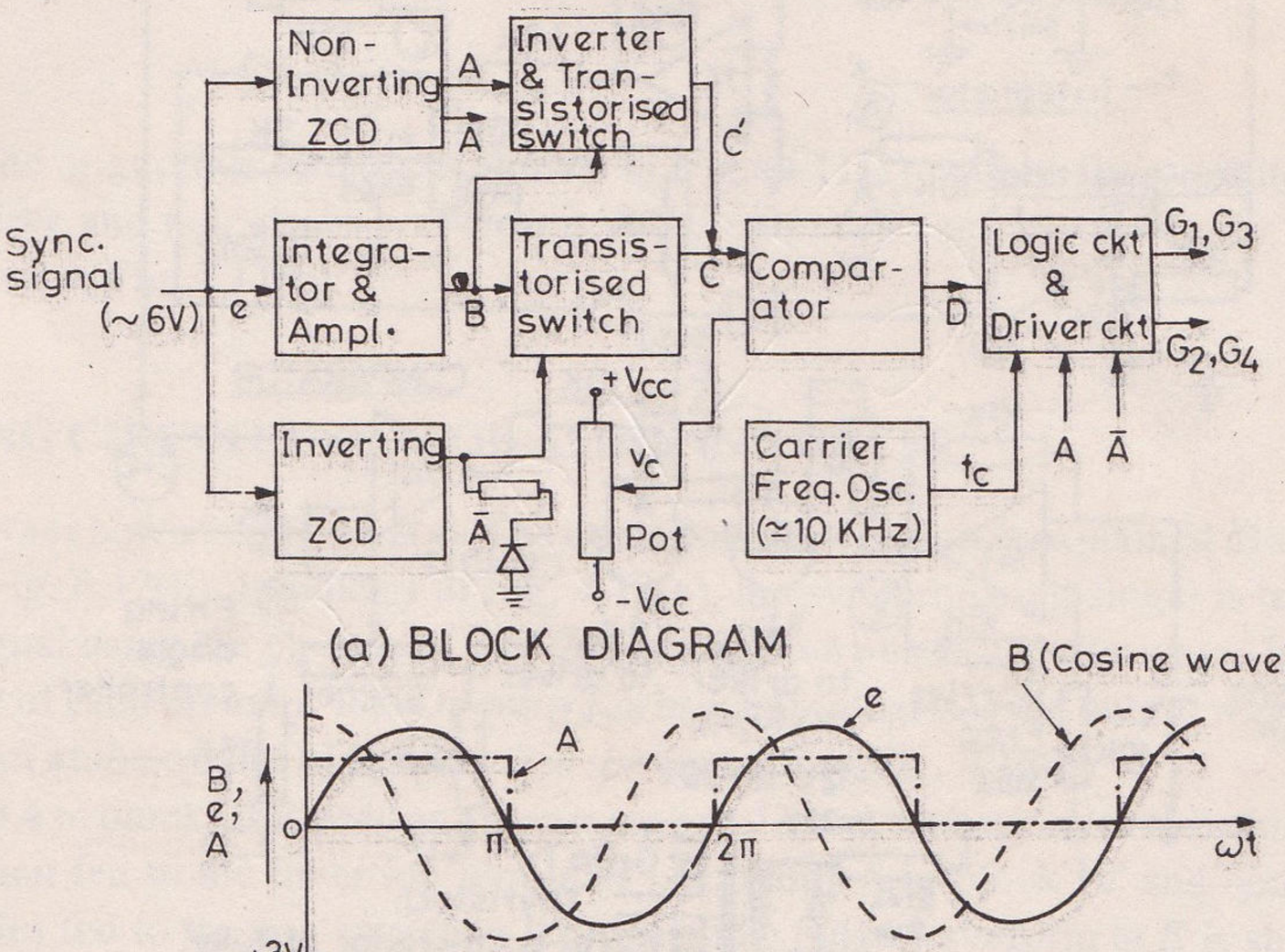
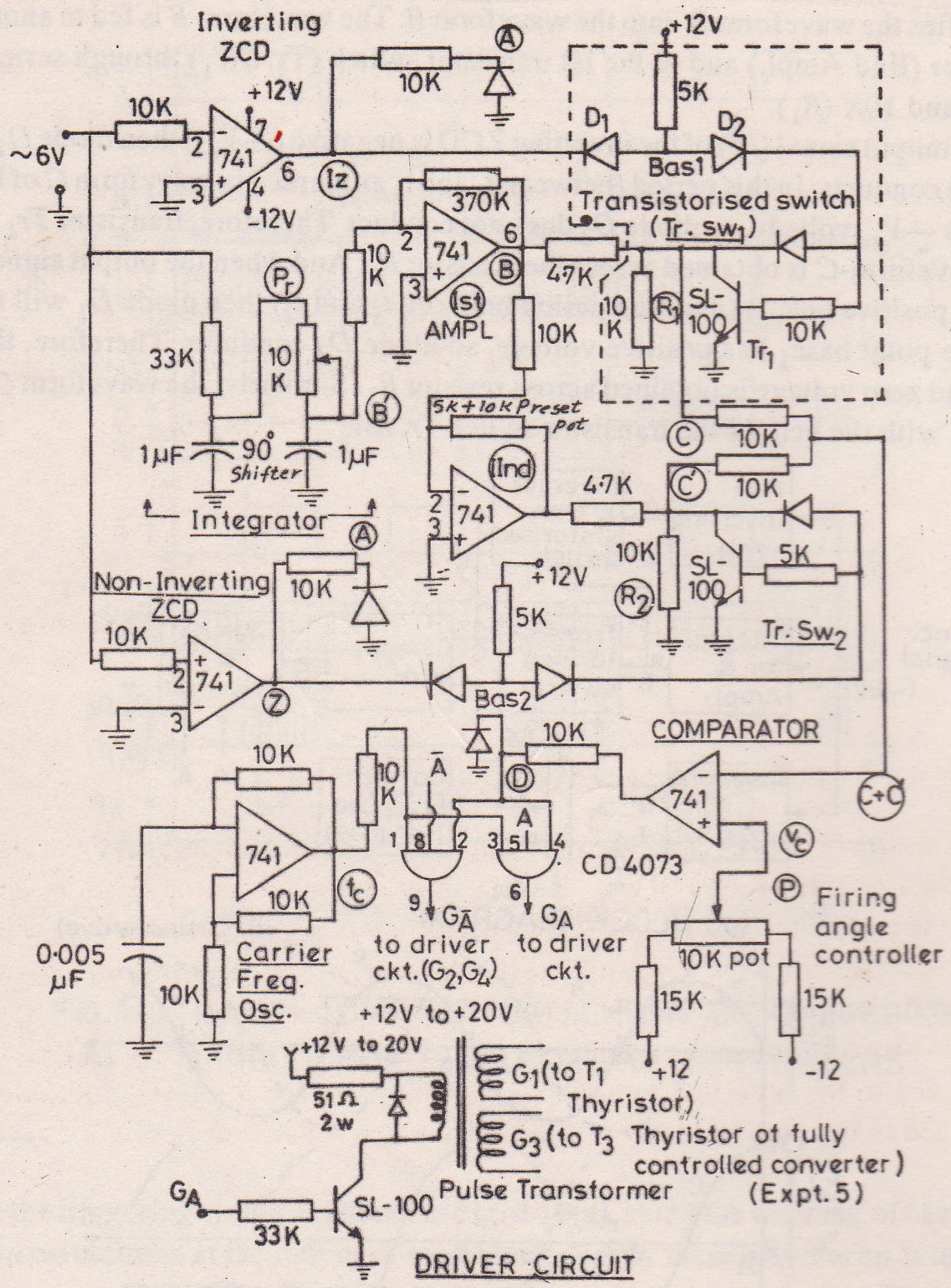


FIG. 4.11(b): WAVEFORMS AT DIFFERENT STAGES OF THE BLOCK DIAGRAM



(c) CIRCUIT DIAGRAM

FIG. 4·11 : COSINE-WAVE SCHEME OF GENERATING TRIGGERING PULSES FOR SINGLE-PHASE CONVERTERS

The waveform C and C' are added and are fed to the comparator. The comparator compares the waveform $(C+C')$ with a dc voltage which can vary between about $+3V$ and $-3V$ and is controlled by the $10K$ pot (P). The output of the comparator (waveform D) forms an input to the logic cicruit.

In logic circuit, a three inputs AND gate (or two AND gates of two inputs each) ANDs the waveforms D, A and carrier frequence f_c ($\simeq$ 10KHz). And the waveform G_A is obtained. Similarly, waveforms G_A^- is obtained at the output of the other AND gate. The high frequency switching is essential to reduce thyristor's gate power dissipation and size of the pulse transformer.

These modulated pulse signals G_A and G_A^- are applied to two separate but identical driver-circuits. The outputs of driver circuits G_1 and G_2 are applied to the positive group thyristor/thyristors and the negative group thyristor/thyristors respectively. The positive group thyristors control the positive half-cycle of controller's input line, while the negative group thyristors control the negative half-cycle.

Procedure

Make the triggering circuit as shown in Fig. 4.11(c). Study the working of each block carefully. Observe and note down waveforms at the output of each block. Verify these waveforms with those shown in Fig. 4.11(b).

3.3 FIRING CIRCUIT USING OP-AMPS AND GATES

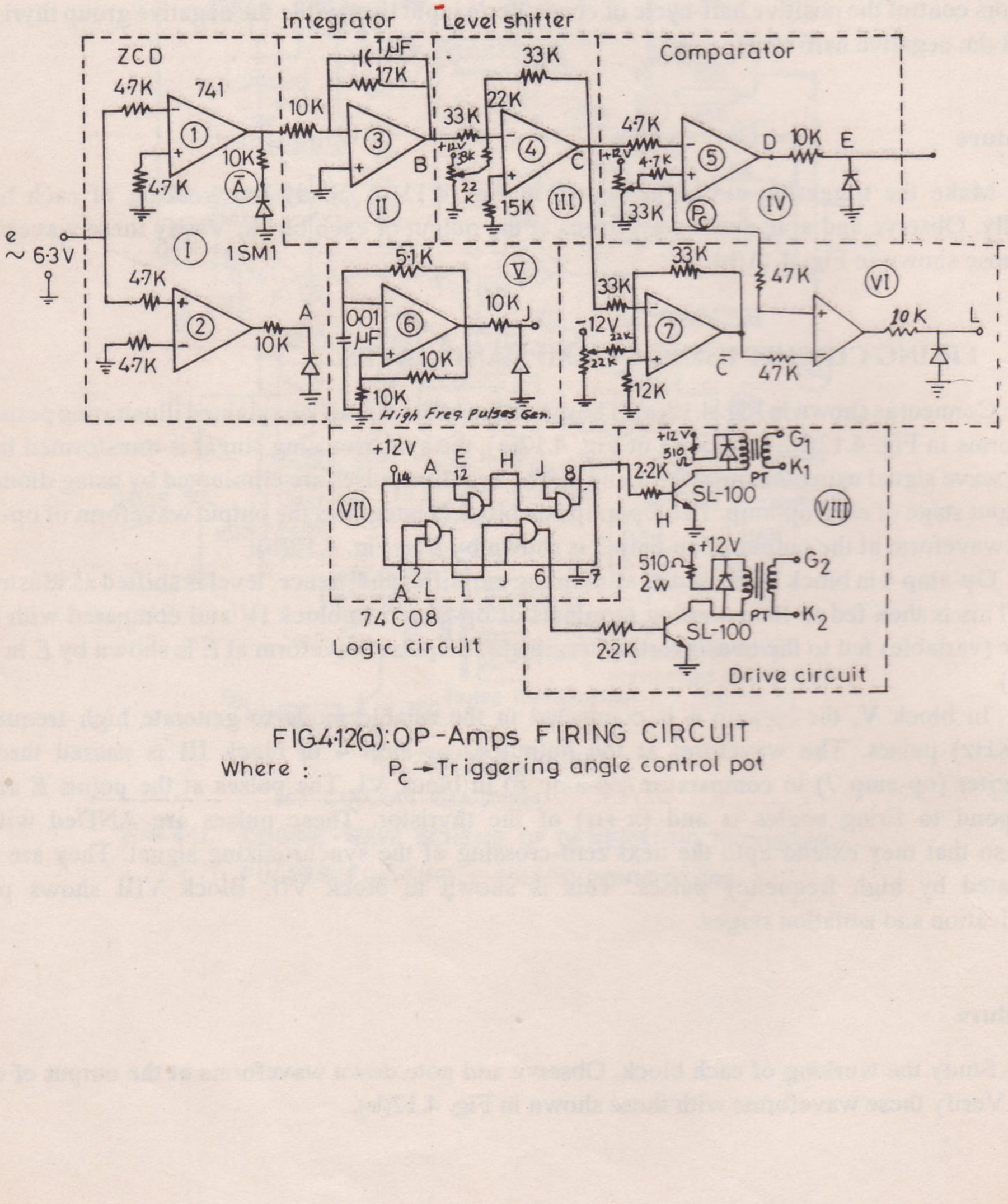
Connect as shown in Fig. 4.12(a). The operation of the circuit is explained illustrating pertinent waveforms in Fig. 4.12(b). In block I of Fig. 4.12(a), the synchronising singal is transformed into a square wave signal using the op-amps 1 and 2. The negative pulses are eliminated by using diodes at the output stage of each op-amp. The Op-amp 3 in block II integrates the output waveform of op-amp 1. The waveform at the output of op-amp 3 is shown by B in Fig. 4.12(b).

Op-amp 4 in block III is used as a summing amplifier and, hence, level is shifted as illustrated by C. This is then fed to the inverting terminals of op-amp 5 in block IV and compared with a dc voltage (variable) fed to the non-inverting terminal. The pulse waveform at E is shown by E in Fig. 4.12(b).

In block V, the op-amp 6 is connected in the astable mode to generate high frequency ($\simeq$ 10 KHz) pulses. The waveform at the output of op-amp 4 in block III is passed through an inverter (op-amp 7) to comparator (op-amp 8) in block VI. The pulses at the points E and L correspond to firing angles α and $(\pi+\alpha)$ of the thyristor. These pulses are ANDed with A and $\bar{A}$ so that they extend upto the next zero-crossing of the synchronizing signal. They are also modulated by high frequency pulses. This is shown in block VII. Block VIII shows pulse amplification and isolation stages.

Procedure

Study the working of each block. Observe and note down waveforms at the output of each block. Verify these waveforms with those shown in Fig. 4.12(b).



FIG·4·12(a): OP-Amps FIRING CIRCUIT

Where : P_c → Triggering angle control pot

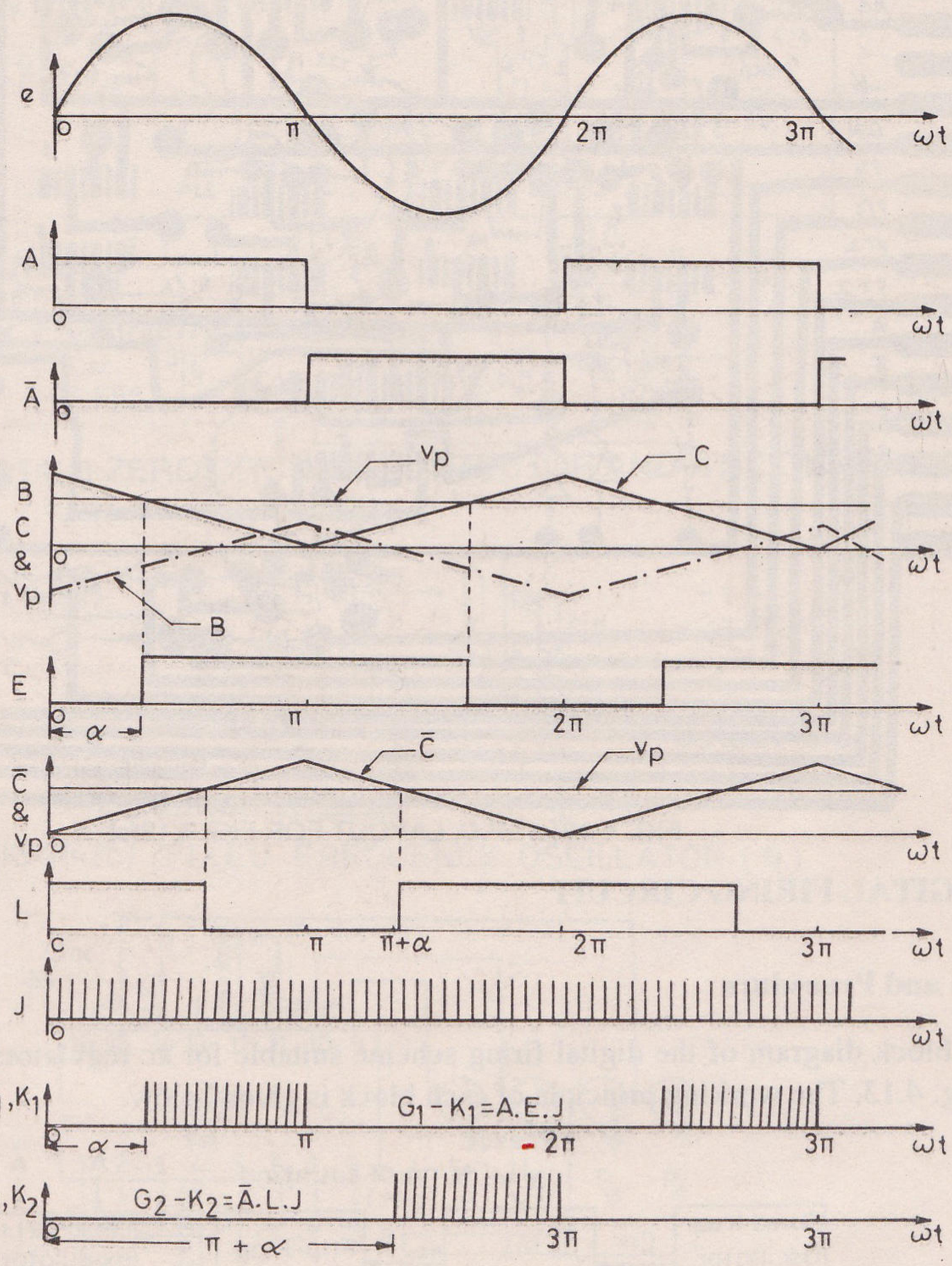


FIG.4.12 (b):WAVEFORMS AT DIFFERENT STAGES OF FIG.4.12(a)

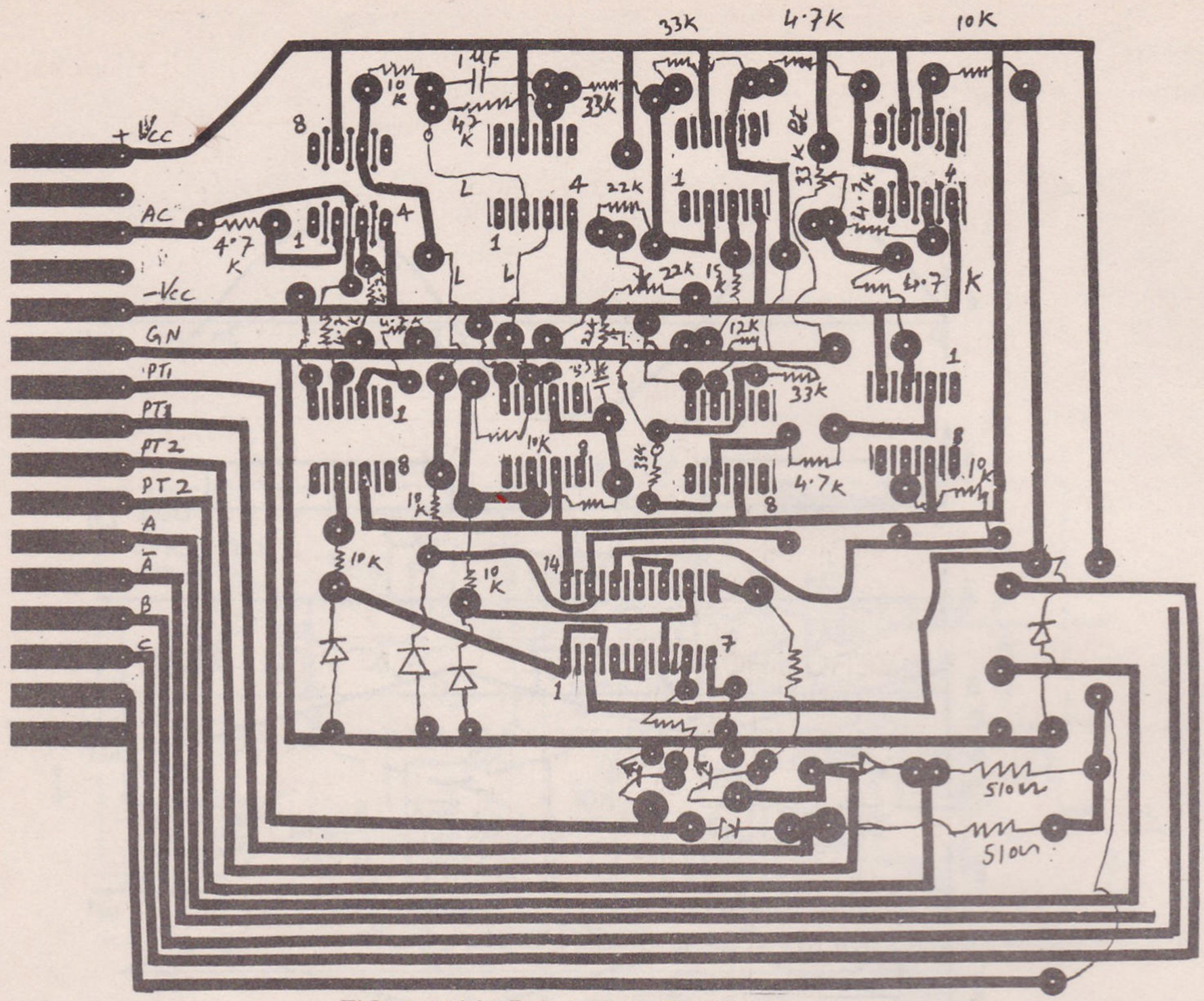


FIG. 4-12(c) : P.C. LAYOUT FOR FIG. 4.12(a)

3.4 DIGITAL FIRING CIRCUIT

Description and Procedure

The block diagram of the digital firing scheme suitable for ac regulators and converters is shown in Fig. 4.13. The working principle of each block is given below.

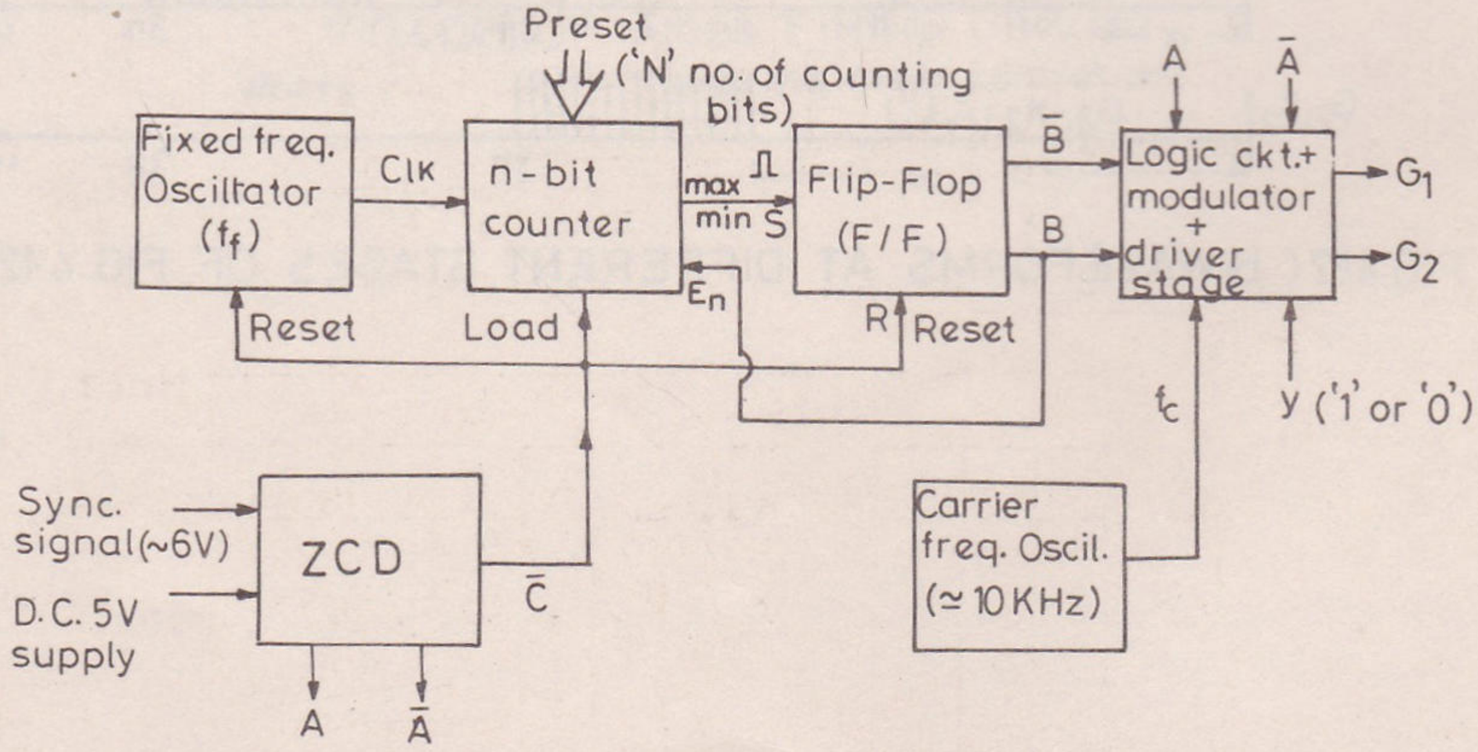


FIG.4·13 : BLOCK DIAGRAM OF THE DIGITAL FIRING CIRCUIT

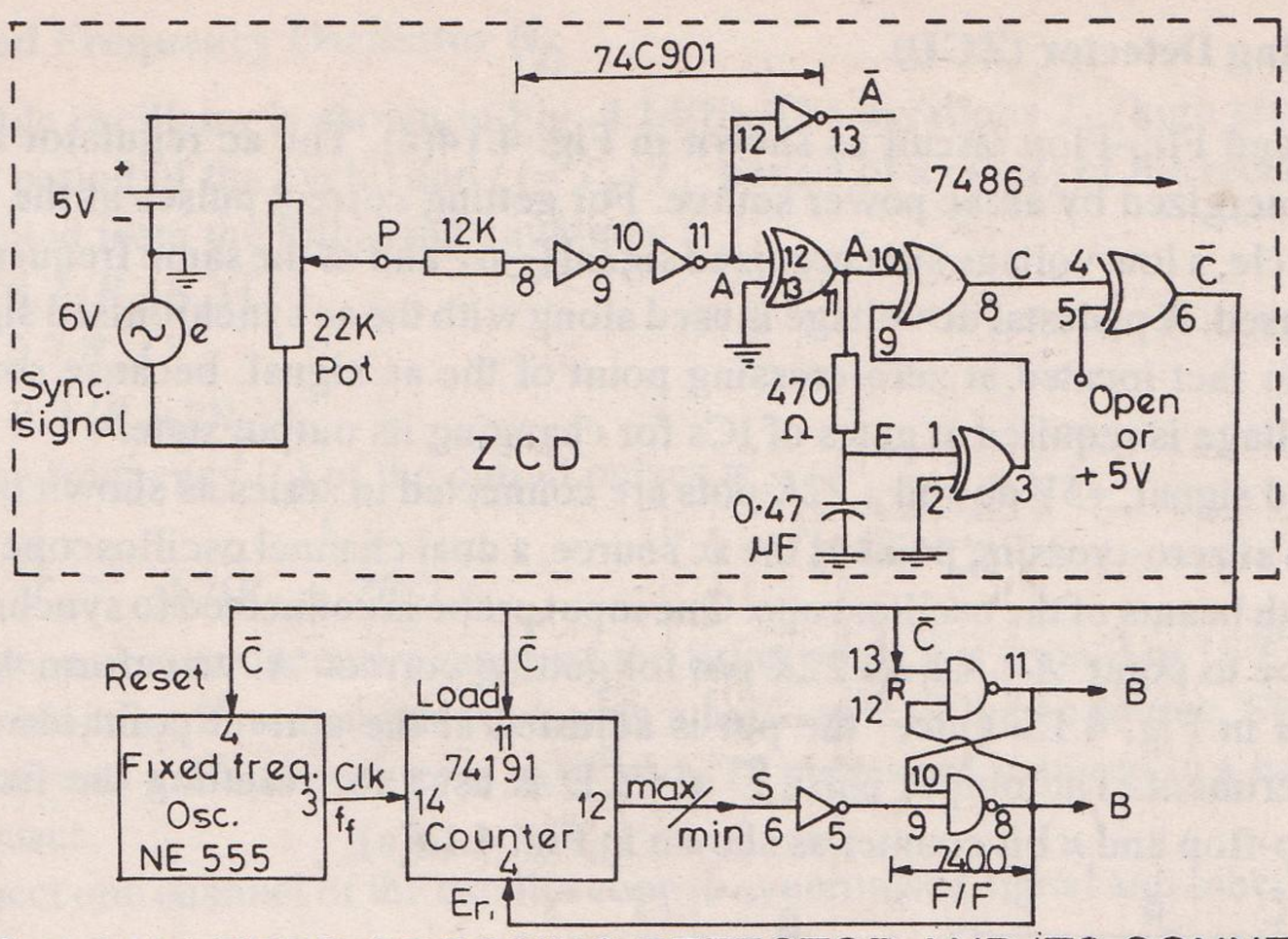


FIG. 4.14(a) ZERO CROSSING DETECTOR AND ITS CONNECTIONS

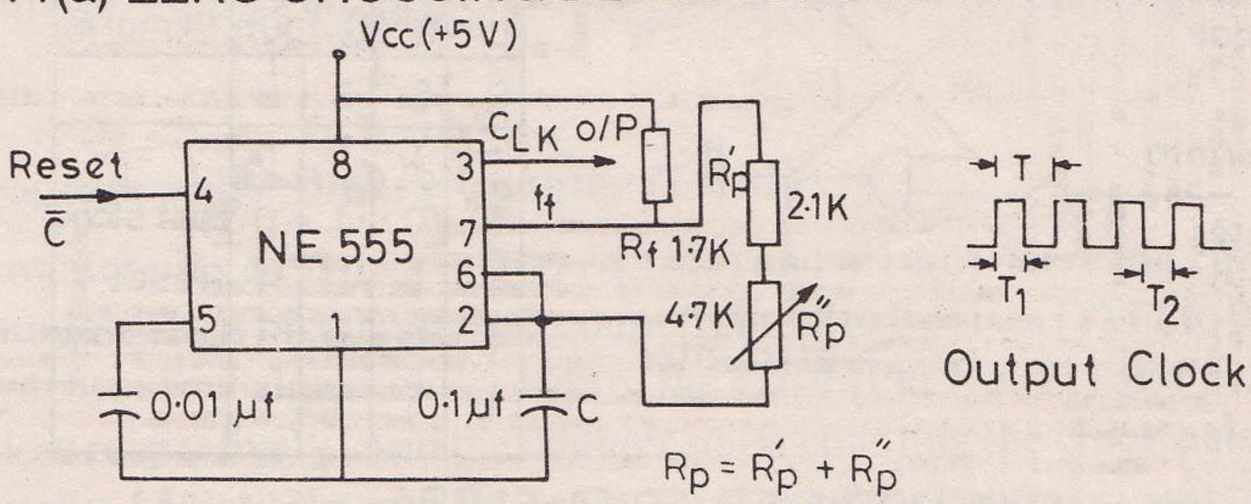
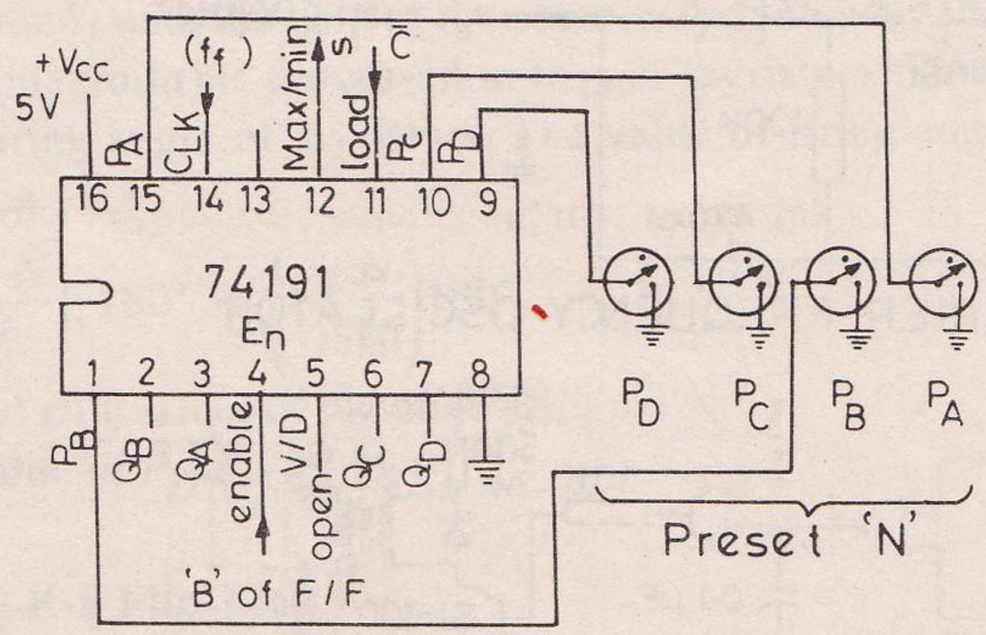


FIG.4·14(b): FIXED FREQUENCY OSCILLATOR (f_f)



Inputs								Outputs
E_N	V/D	Load	C_{LK}	P_A	P_B	P_C	P_D	Q_D Q_C Q_B Q_A
1	X	X	X	X	X	X	X	Stop count
0	X	0	X	P_A	P_B	P_C	P_D	P_D P_C P_B P_A
0	0	1	↑	X	X	X	X	Up count
0	1	1	↑	X	X	X	X	Down count

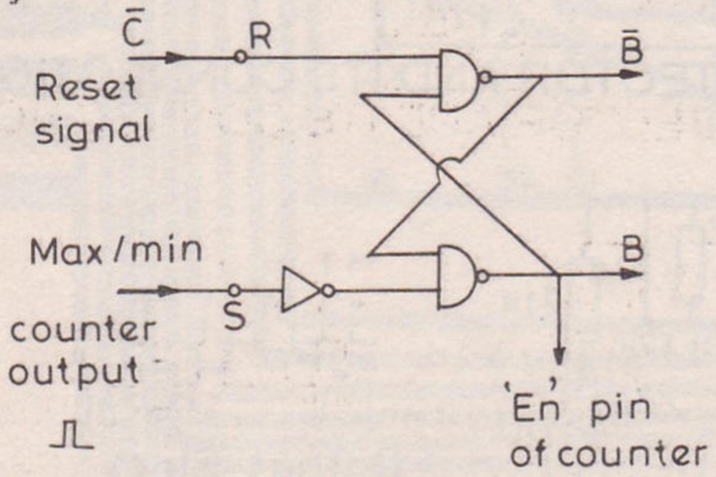
Note:
1 → Open or +5V
0 → Ground
x → No care 1 or 0

FIG. 4-14(c) : PROGRAMMABLE 4-BIT COUNTER

(1) Zero-Crossing Detector (ZCD)

make ZCD and Flip-Flop circuit as shown in Fig. 4.14(a). The ac regulator and converter power circuits are energized by an ac power source. For getting correct pulses at the zero crossing point in each half-cycle, a low voltage synchronized signal ($\simeq 6V$ and of the same frequency and phase as the ac source), is used. A pedestal dc voltage is used along with the ac synchronised signal to ensure that the pulses are in fact located at zero-crossing point of the ac signal, because some minimum (threshold) input voltage is required at gates of ICs for changing its output state.

Synchronised signal, $+5V$ dc and a $22K$ pots are connected in series as shown in Fig. 4.14(a). For obtaining pulses at zero-crossing point of the ac source, a dual channel oscilloscope is used. Keep the same base for both beams of the oscilloscope. One input probe is connected to synchronized signal and other input probe to point '*A*'. Adjust $22K$ pot for getting correct '*A*' waveform with respect to source '*e*' as shown in Fig. 4.15. Once the pot is adjusted at the correct point, do not disturb it throughout the experiment. The output pulse $\overline{C}$ of ZCD is used for resetting the fixed frequency oscilloscope (f_f), flip-flop and *n* bit counter as shown in Fig. 4.14(a).



Inputs		Outputs		Remarks
R	S	B	B̄	
1	1	1	0	
1	0	1	0	Last stage
0	0	0	1	Reset
1	0	0	1	Last stage
1	1	1	0	

FIG·4·14(d): MODIFIED FLIP-FLOP

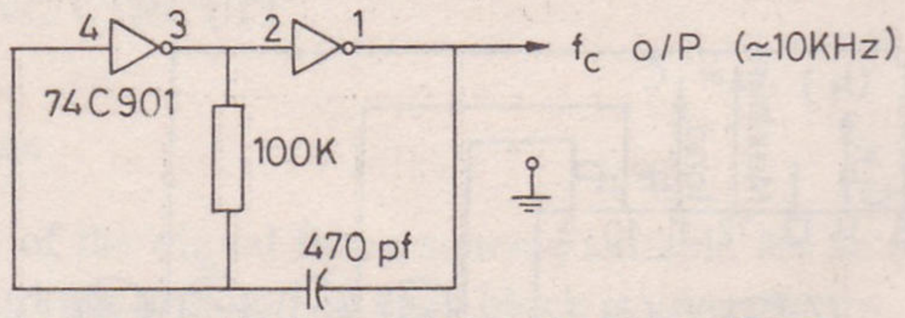
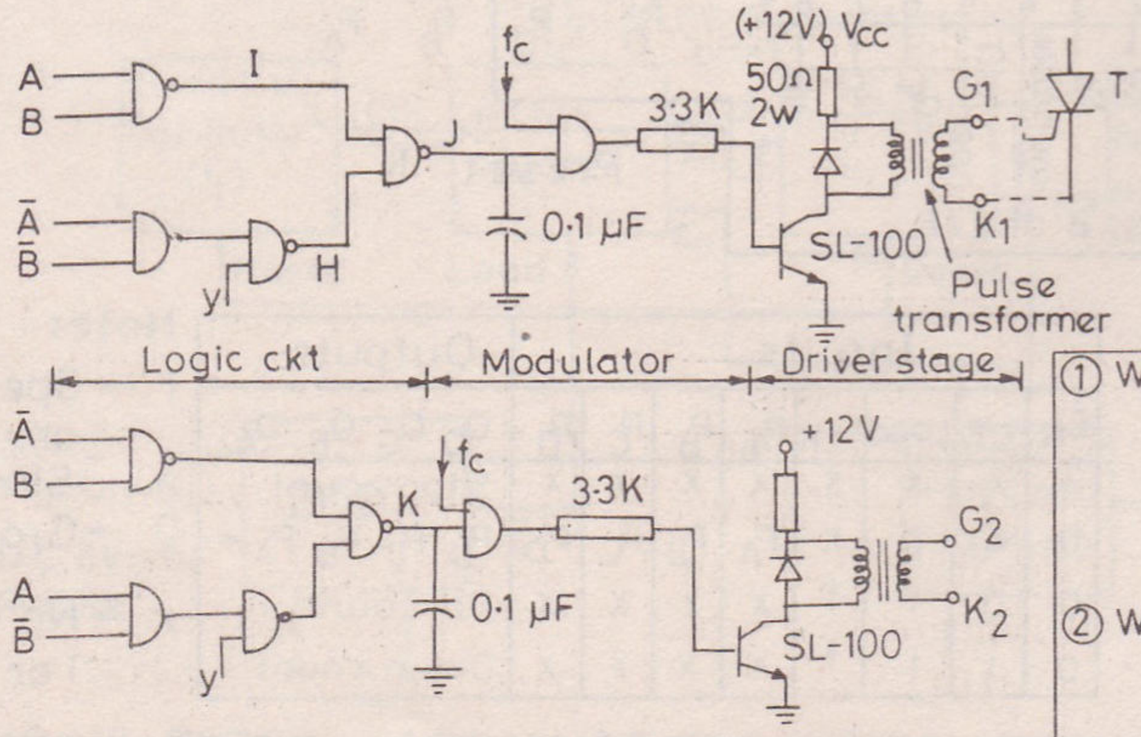


FIG.4·14(e): CARRIER FREQUENCY OSCILLATOR



① When $y = 0$
$I = \overline{A.B}$
$H = 1$
$J = A.B$

② When $y = 1$
$H = \overline{\bar{A}.\bar{B}}$
$J = \overline{(\overline{A.B}).(\overline{\bar{A}.\bar{B}})}$
$A.B + \bar{A}.\bar{B}$

FIG·4·14(f): LOGIC CIRCUIT, CARRIER MODULATOR AND DRIVER STAGE

(2) **Fixed Frequency Oscillator (f_f)**

A stable oscillator is shown in Fig. 4.14(b). The durations T_1 (high state period of a cycle), T_2 (low state period of the cycle) and t (= T_1+T_2; period of a cycle) of the rectangular output pulses can be calculated from the following equations :

$$T_1 \simeq 0.7\,(R_f+R_p)\,C$$

$$T_2 \simeq 0.7\,R_p.C$$

and $$T \simeq 0.7\,(R_f+2R_p)\,C$$

So, the frequency (f_f) of the output pulses is

$$f_f = \frac{1}{T} \simeq \frac{1}{0.7(R_f + 2R_p)\,C}$$

In order to cover the entire range of the firing angle (α) from 0 to 180°, the n-bits counter is required for obtaining 2^n rectangular pulses in a half-cycle of the ac source. Since source frequency (50 Hz) is used and a 4-bits counter is used here, 16 pulses are required in a half-cycle duration (10 ms) of the source.

Connect one channel of the oscilloscope to syncronised signal and other channel to the output pulses of the oscillator. Adjust the preset pot R_p" such that the oscillator generates 16 pulses in a half-cycle duration.

(3) **4-Bit Programmable Binary Counter (74191)**

Connect counter pins as shown in Figs. 4.14(a) and 4.14(c). Here the counter is being used in 'Down counting mode'. The 4 bit counter can count from 15 to 0 pulses (1111 to 0000 binary number). As soon as, the synchronised signal crosses zero, the Load (Pin No. 11) and *En* (Enable, Pin No. 4) become high and low respectively. And the counter starts counting the clock pulses (f_f) in down mode from the decimal value 15 until the present decimal value of the control signal '*N*' (*N* = Binary vlaue of pins status P_D, P_C, P_B, P_A respectively). The pins P_A, P_B, P_C and P_D can be made high (+5V or open) or low (ground) with the help of their two-way switches as shown in Fig. 4.14(c). The counter overflow signal (max/min) is processed to trigger thyristors. Thus, by varying the preset input one can control the firing angle of thyristors. The value of firing angle (α) can be calculated from the following equation :

$$\alpha = \left(\frac{2^n - N}{2^n}\right) 180^\circ = \left(1 - \frac{N}{16}\right) 180^\circ$$

where N : decimal equivalent of the control signal
(preset value of $P_D\,P_C\,P_B\,P_A$)

(4) **Modified R-S Flip-Flop**

Make Flip-Flop circuit as shown in Fig. 4.14(d). Reset input terminal (R) of Flip-Flop is connected with the output pulse $\overline{C}$ of ZCD and set input terminal (S) of the flip-flop is set according to the output (max/min) of the counter. The pulse $\overline{C}$ goes to low (O) at each zero-crossing of the synchronized signal. And a low value of $\overline{C}$, which is an input to flip-flop, resets $\overline{B}$ to 1 and B to 0. A high output of the counter sets the F/F's outputs $\overline{B}$ to 0 and B to 1. It state of flip-flop is latched till the next zero-crossing of the synchronised signal. The output terminal B of flip-flop is connected with 'En (enable)' pin of counter 74191. A high 'En' of counter stops counting till the next zero-crossing.

(5) Logic Circuit, Modulation and Driver Stage

The output pulses of the flip-flop, and pulses A and $\overline{A}$ of ZCD are applied to the logic circuit as shown in Fig. 4.14(f). The 'J' and 'K' waveforms are obtained at the output of logic circuit. The logic variable 'Y' equal to 0 or 1 enable us to select the firing pulse duration either from α to π or from α to $\pi + \alpha$.

When $Y = 0$ then the pulse duration is from α to π
and when $Y = 1$ then pulse duration is from α to $\pi + \alpha$

Observe and note down the waveforms at the output of each block. Verify these waveforms with those shown in Fig. 4.15.

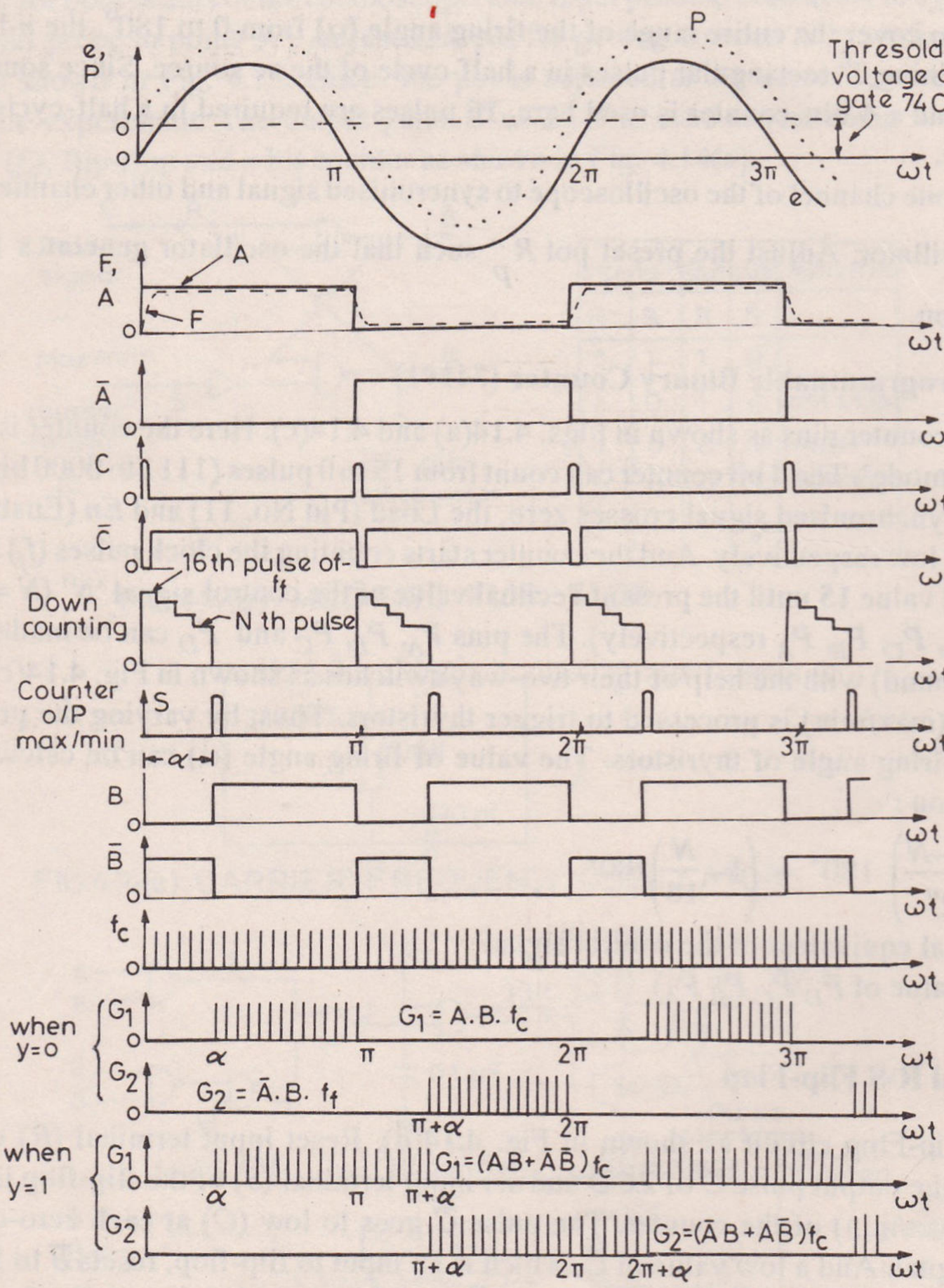


FIG. 4.15: WAVEFORMS OF DIGITAL FIRING CIRCUIT

QUESTIONS

3.1 Draw the following circuit by using the operational amplifier (op-amp 741) IC :

(i) Inverting and Non-inverting amplifiers and calculate amplification factor (gain) of both amplifiers when feedback resistor is double the input resistor.

(ii) Summing amplifier for four voltages e_1, e_2, e_3 and e_4 when all inputs resistors and feedback resistor are equal.

(iii) Oscillator circuit for 10KHz rectangular waveform with equal on and off periods. Explain its working also.

(iv) Comparator circuit for comparing sinusoidal input voltage and ground. Also draw input and output voltage waveforms with amplitude.

(Hint : Open loop gain of a op.amp. 741 $\simeq$ 10^5 to 10^6, input bias current max. = 500 mA, Max. supply voltage = ± 18V, Min. supply voltage - ± 5V, Max. input voltage = ± 15V, and Max. differential input voltage = ± 30V).

3.2 Ramp oscillator (Modified Integrator Circuit) is shown in Fig. Q. 3.2. Draw the waveforms of ramp with amplitude (> or = or < than V_{cc}) when time constant (t) = RC is as follows.

(i) $t > T_1$
(ii) $t = T_1$
and (iii) $t < T1$

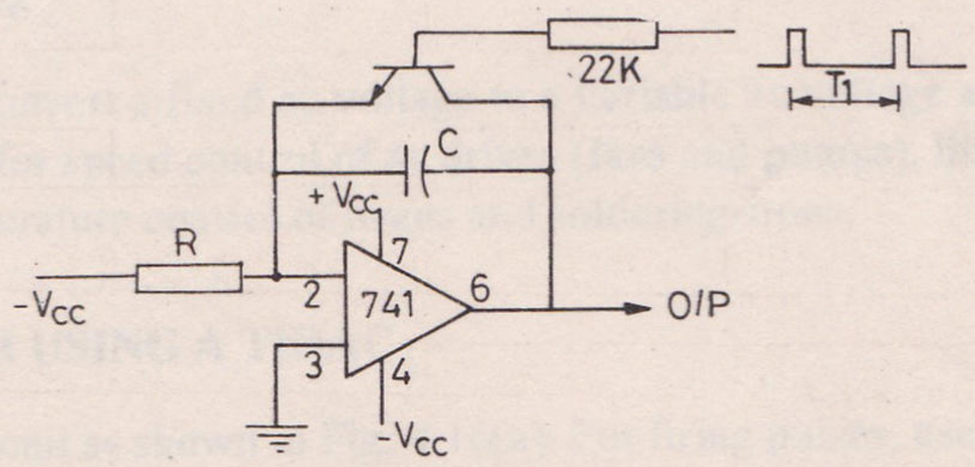


FIG. Q.3.2 : RAMP OSCILLATOR CIRCUIT

3.3 Fig. Q. 3.3 shows a phase shifter circuit. Calculate maximum and minimum phase-shifting angle (θ) of voltage v_c w.r.t. waveform e and also draw voltage waveforms v_c and e with their peak value. Let supply frequency be 50 Hz.

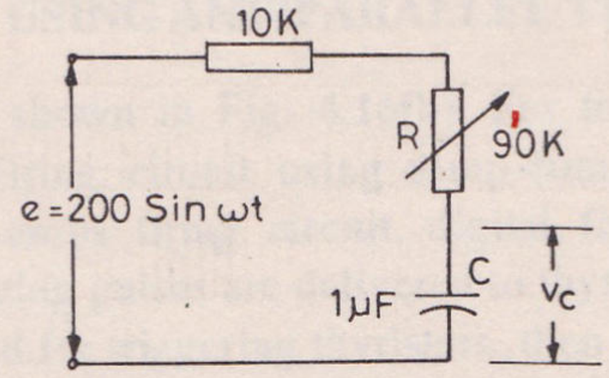


FIG. Q.3.3 : PHASE SHIFTER CIRCUIT

[**Hint** : $\theta = \tan^{-1}(\omega cr)$; $v_c = i(t)\left(\frac{1}{\omega C}\right)$

and $i(t) = \frac{V_m}{\sqrt{(R^2 + \frac{1}{W^2C^2})}} \sin(wt - \theta)$]

3.4. Draw the symbols and write the truth-tables of the following gates :

AND, NAND, NOR, EX.-OR AND NOT.

3.5 Draw and write on and off time period equation of the output voltage waveform for the following multivibrators by using the 555 timer :

(i)Astable Multivibrator circuit (also called free-running multivibrator)
(ii)Monostable multivibrator circuit (also called one-shot multivibrator)

3.6 Draw the symbol and characteristics of the schmitt-trigger inverter. And also draw output of the schmitt-trigger inverter when its input is a sinusoidal voltage.

Experiment No. 4

Objective : To study different types of Single-phase AC Regulators

4.1 : AC regulator using a triac

4.2 : AC regulator using thyristor connected in antiparallel

4.3 : AC regulator using a triac and a diac (with *R-C* triggering circuit)

4.4 : AC regulator using photo-devices (Automatic controlled road lights)

Apparatus Required

Dual beam Oscilloscope, Thyristor and Triac lab. module, Pulse-Transformers, Lamp load, Rheostat, Inductor, DC motor, Fabricated UJT firing circuit, Any one converter firing circuit, 230*V* : 6*V* to 15*V* transformer for synchronisation, Low voltage power supply, Diac, Photo-diodes and Photo-resistor. See appendix 1 for selecting the rating of the apparatus.

Description and Procedure

The ac regulators convert a fixed ac voltage to a variable ac voltage at the same frequency. The ac regulators are used for speed control of ac drives (fans and pumps), illumination (brightness of lamps) control and temperature control of ovens and soldering-irons.

4.1 AC REGULATOR USING A TRIAC

Make the power circuit as shown in Fig. 4.16(a). For firing pulses, use the UJT-firing circuit as shown in Fig. 4.7 of Experiment 2. Before releasing the firing pulses, one must ensure right polarity of the gate pulses, (i.e., gate must be positive w.r.t. cathode) in each half-cycle of the power supply. Release the firing pulses to the gate of the triac. Observe the load and triac voltage waveforms for various firing angles.

4.2 AC REGULATOR USING ANTIPARALLEL THYRISTORS

Connect the circuit shown in Fig. 4.16(b). For triggering thyristors, use anyone of the following firing circuits; firing circuit using ramp-comparator approach, firing circuit using cosine-wave approach, op-amps firing circuit, digital firing circuit and UJT-firing circuit of Experiments 2 and 3. The firing pulses are delivered to thyristor's gate through pulse transformers. If a UJT-firing circuit is used for triggering thyristors, then pulse transformer with two secondaries is required. The primary is connected to the firing circuit. One secondary is connected to the gate of thyristor T_1 while the other secondary is connected to the gate of thyristor T_2.

Before releasing the firing pulses to the gate of thyristors T_1 and T_2, one must ensure right polarity and phase for the gate pulses with respect to the power supply. For testing the polarity and phase for each thyristor, disconnect the secondary windings of the pulse-transformers by removing connecting leads *A-B* and *C-D* from the gates of thyristors T_1 and T_2 respectively. Connect one channel of the oscilloscope across thyristors in such a way that common terminal (Common or Ground

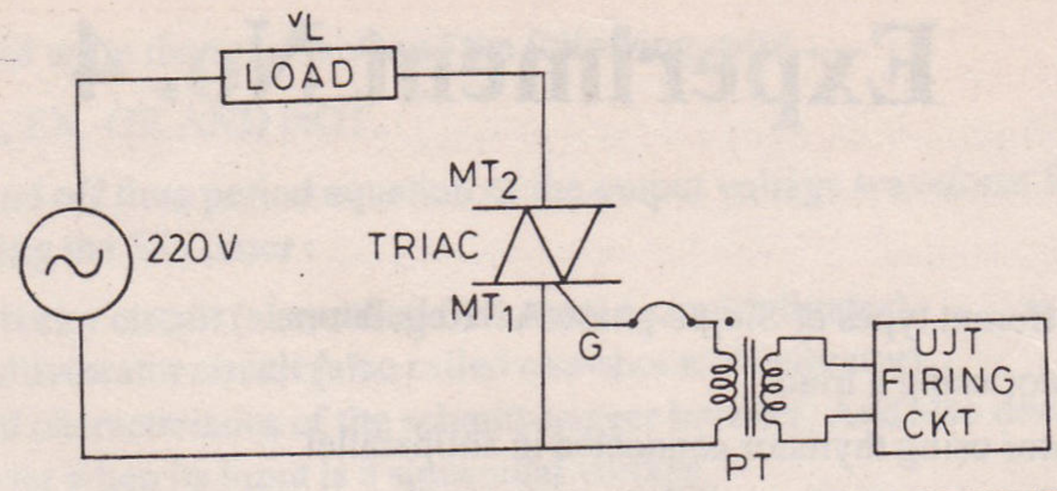


FIG. 4·16(a): A SINGLE-PHASE AC REGULATOR USING A TRIAC

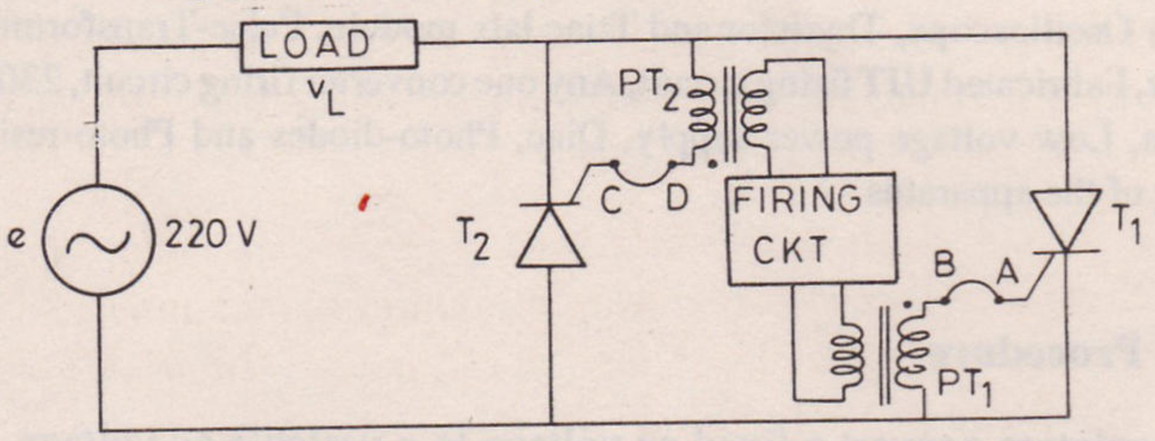


FIG. 4·16(b): A SINGLE-PHASE AC REGULATOR USING ANTIPARALLEL THYRISTORS

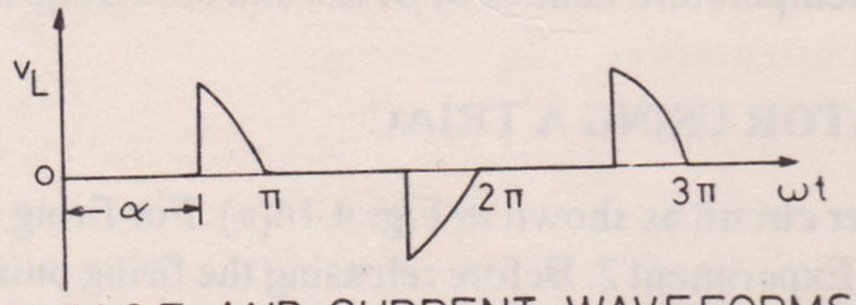


FIG. 4·17 : VOLTAGE AND CURRENT WAVEFORMS ACROSS RESISTIVE LOAD

terminal of both channels) is connected with the cathode of thyristor T_1. And other channel is connected to the secondary winding of the pulse transformer PT_1. Check that the terminal of the secondary to be connected to the gate of thyristor T_1, must be positive with respect to the terminal to be connected to the cathode. Otherwise interchange the secondary or primary winding terminals. Also check that the firing pulses must be presented in the half-cycles of the power supply for which anode is positive with respect to cathode. Otherwise, interchange the terminals of the power supply (e). Similarly, test the polarity and phase for the gate pulses of thyristor T_2.

(a) Connect a lamp load and observe the load voltage waveform for various firing angles. Also observe the change in the brightness of the lamp with a change in firing angle.

(b) Now connect a R-L load and observe the load voltage waveforms for various firing angles.

4.3 AC REGULATORS USING A TRIAC AND A DIAC (WITH R-C TRIGGERING CIRCUIT)

Make the circuit as shown in Fig. 4.18(a) with lamp load or resistive load (rheostat). Open the switch '*S*'. Measure and note down the maximum and minimum phase-difference between the

input voltage (e) and capacitor voltage (v_c) by varying 100K Pot (R_p). Draw the capacitor voltage (v_c) waveform w.r.t. the input voltage (e) waveform and also observe maximum capacitor voltage (v_c) for both maximum and minimum resistance positions of the 100K pot (R_p).

After closing switch 'S', the circuit works as follows. As the input voltage (e) increases positively or negatively, capacitor C is charged through the load, Resistor R and 100K Pot (R_p). The charging rate of the capacitor C is controlled by the 100 K Pot (R_p). When the capacitor voltage (v_c) exceeds the breakover voltage ($\pm V_{BO}$) of the diac (the breakover voltage of the Diac SD32, is 32 volts), the diac is turned-on. The capacitor, C discharge through diac and the gate and MT_1 junction of the triac. Hence, the triac is turned-on and allows ac power to flow in the load. The firing angle (α) for both half-cycles of the power supply (e) can be controlled by varying the position of the 100K Pot, R_p.

Connect lamp as a load in the circuit of Fig. 4.18(a). Close the switch 'S'. If this circuit works satisfactorily (lamp brightness can be controlled by varying the 100K Pot) as expected. Then do the following tests :

Test -1 : Connect R-load (lamp or rheostat) and observe load voltage and load current waveforms as the firing angle, α is varied from minimum to maximum. Also measure the minimum and maximum firing angle of the triac. Observe the triac voltage waveform w.r.t. the capacitor voltage (v_c) waveform.

Test-2 : Repeat the above test for an R-L load. Connect the oscilloscope across R (resistor) for observing load current waveform. Also observe the effect of the variation of R (resistance) on the load current waveform.

Test-3 : Connect an ac motor (driving fan, pump, etc.) as a load. Connect a shunt (low value resistance between 0.1Ω to 1.0Ω) in series with the motor for observing motor current waveform. Observe the effect of the variation of the firing angle on the motor speed. Observe the motor current and terminal voltage waveforms.

4.4 AC REGULATOR USING PHOTO-DEVICES (AUTOMATIC CONTROL OF ROAD LIGHTS)

Make the circuit as shown in Fig. 4.18(b). Close the windows of photo-diodes D_1 and D_2 by insulation tape. Now circuit works as explained in Experiment 4.3. The firing angle (α) of the triac can be controlled by changing the position of 100K Pot R_p.

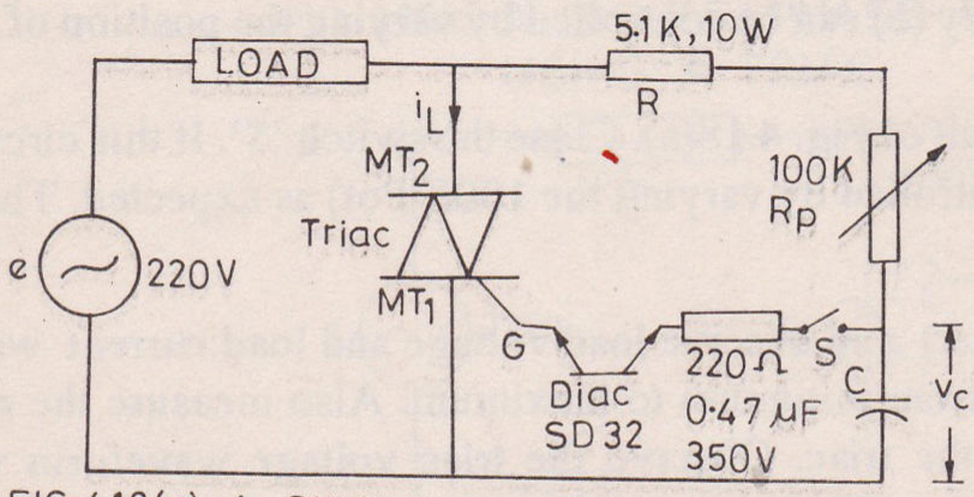
(a) Now remove the tape from the window of the photo-diode D_1 *(Photo-diode is a light sensitive device; it's resistance decreases with light)*. The light (torch light, sunlight, etc.), is allowed to fall on the window of photo-diode D_1. In the negative-half-cycle (when terminal MT-2 of the triac is negative w.r.t. terminal MT-1), the photo-diode D_1 conducts. Therefore, the diac does not conduct because the voltage drops across the diode D_1 ($\simeq$ 0.6 volts) is much less than the breakover voltage ($+V_{BO}$) of the diac. So, the power cannot flow into the load in the negative half-cycle of the supply. The circuit works as a half-controlled converter.

Now remove the tape from the window of the photo-diode D_2. The light is allowed to fall on the window of photo-diode D_2. It stops the flow of power in the load in the positive-half-cycle of the supply. So, the power does not flow in load when the windows of both the photo-diodes D_1 and D_2 are opened.

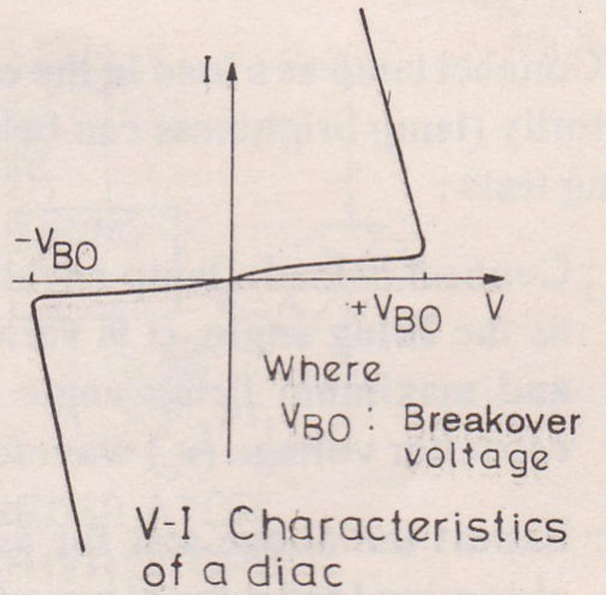
This circuit also can be used for controlling road light automatically by using lamp as a load. The circuit is turned ON automatically at night and the lamp glows. It is turned OFF in the day, so the lamp does not glow in the day.

Repeat the tests 1, 2 and 3 of Experiment 4.3 by closing and opening the windows of photo-diodes D_1 and D_2.

(b) Changes the 100*K* Pot R_p of Fig. 4.18(b) by a *photo-resistor R, which is a device whose resistance decreases with the increase in the light intensity.* Repeat the Experiment 4.4(a) by controlling the intensity of the light which is allowed to fall on the photo-resistor R_p.



FIG·4·18(a) A SINGLE-PHASE REGULATOR USING A TRIAC AND A DIAC (R-C TRIGGERING CIRCUIT)



V-I Characteristics of a diac

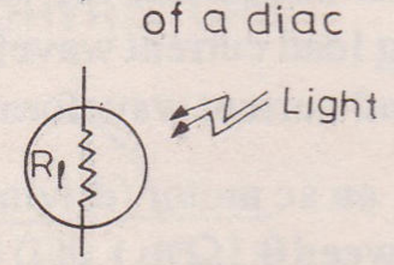
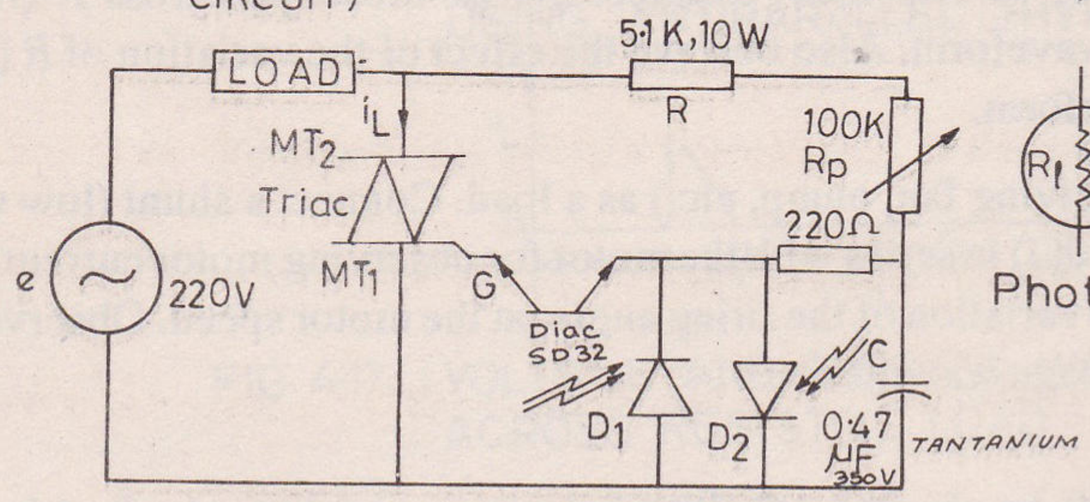
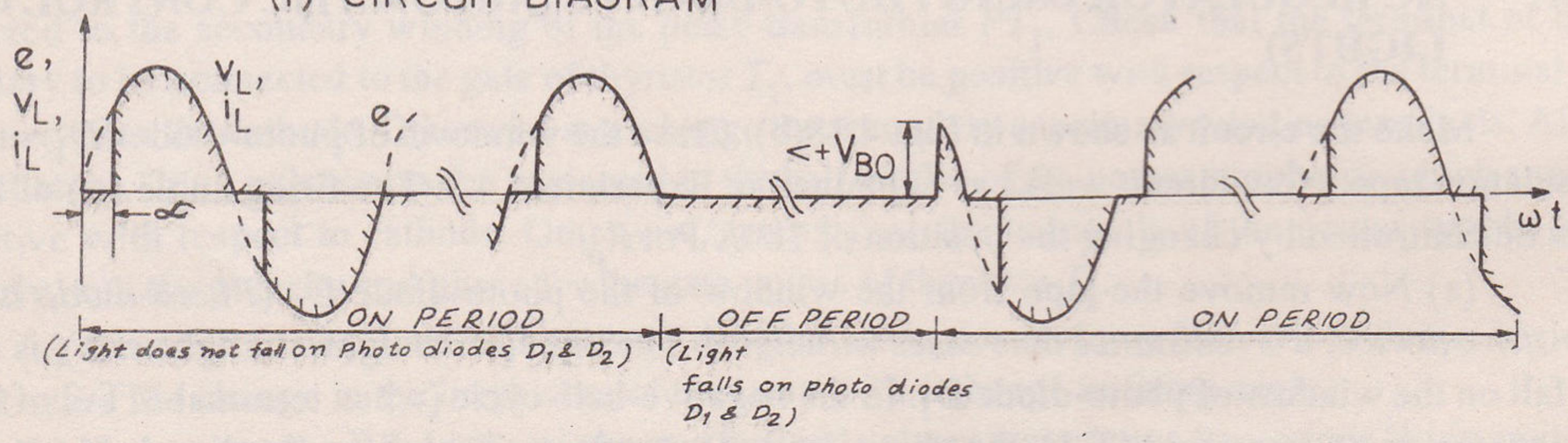


Photo-resistor



(i) CIRCUIT DIAGRAM



(ii) VOLTAGE AND CURRENT WAVEFORMS ACROSS R-LOAD

FIG·4·18(b) TRIAC AC REGULATOR WHOSE ON AND OFF TIME-INTERVALS ARE CONTROLLED BY PHOTO-DIODES

QUESTIONS

4.1 Fill in the Blanks :

(i) A triac is equivalent to two thyristors connected in _____.

(ii) A triac can be triggered with _____ polarity gate voltage when MT_2- terminal is at positive or negative voltage w.r.t. MT_1 terminal.

(iii) Generally, a diac is preferred to trigger a _____.

(iv) A triac is used as an _____ switch.

(v) A thyristor can control only _____ half-cycle of the supply voltage.

(vi) A triac can be triggered in _____ modes. Write these modes : _____

(vii) A high current thyristor and GTO-Thyristor can be triggered with a _____ gate current.

4.2 Find the rms value of the following waveform :

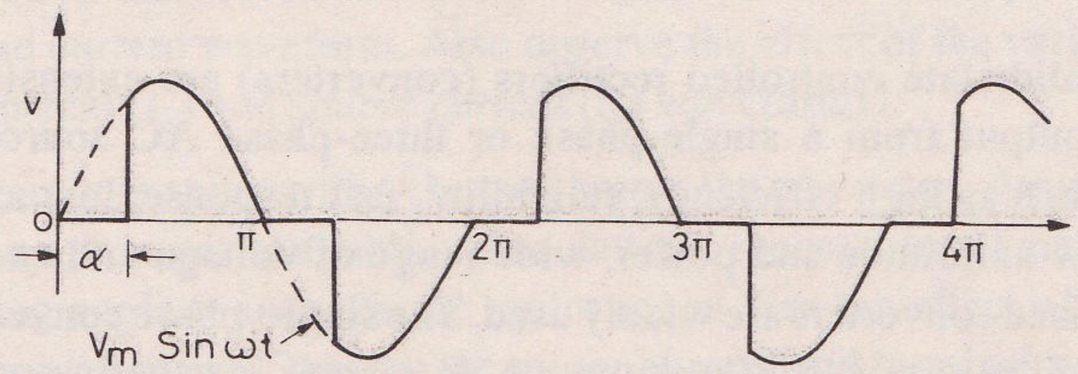


FIG. Q·4·2 : LOAD VOLTAGE WAVEFORM OF THE SINGLE-PHASE A C REGULATOR

4.3 Why is the isolation (pulse transformer or opto-coupler) required between control circuit and power circuit?

4.4 Why is the isolation required between oscilloscope power supply and power circuit or control circuit power supply ?

4.5 Which type of oscilloscope is used if isolation is not presented between oscilloscope and power circuit supply?

Experiment No. 5

Objective : To study the operation of Single-phase Fully- Controlled Bridge Converter.

Apparatus Required

Oscilloscope, Thyristor and diode lab. module, Pulse-Transformers, Rheostat, Inductor, DC motor, Any one fabricated converter firing circuit, 230*V* : 6*V* to 15*V* transformer for synchronization, Shunts (low value and high voltage resistance for tracing current waveform at any place of the circuit on the oscilloscope), and Low voltage dc power supply.

Description

Presently, the solid-state controlled rectifiers (converters) are extensively used for getting controlled DC power output from a single-phase or three-phase AC source. A thyristor offers numerous advantages such as high efficiency, reliability, fast response, low maintenance, compact size, firing pulses of low amplitude and power, wide range of voltage and current. Owing to these advantages the thyristorised converters are widely used. The single-phase converter may be connected either in midpoint of bridge circuit configuration. A dc reactor is usually connected in the output circuit in order to reduce ripple and to obtain continuous output current.

Fully controlled converters find wide application in dc motor control. For low power applications (upto around 10 *KW*) single-phase converters are used and for larger power applications, three-phase converters are used. The supply power factor is generally poor compared with the half-controlled converters specially at large phase delay angles. However, they generate relatively less harmonic currents in the input lines. Another advantage of a fully controlled converter is that the output voltage can be made negative by keeping the firing angle more than $\pi/2$. And with a source of proper polarity in the output circuit as shown in Fig. 4.20, the output power can be returned to the ac source. When the converter operates in this mode, it is called a line-commutated inverter.

Procedure

Single-phase fully controlled bridge converter circuit is shown in Fig. 4.19. Use any one of the firing circuits from Expt. 3 (ramp-comparator approach, cosine-wave approach, op-amp or Digital firing circuit) and modified UJT-firing circuit, the block diagrams and circuits of which are shown in Fig. 4.22(a) and Fig. 4.22(b) respectively. The voltage waveforms at different points of the modified UJT-firing circuit and across *R-L* load of the converter, are shown in Fig. 4.22(c). Fig. 4.22(d) shows the oscilloscope traces of the single-phase fully-controlled converters. The firing pulses are delivered to thyristor-gates through pulse transformers. Each pulse transformer has two secondaries. The primary is connected to the firing circuit and two secondaries are connected to the diagonally opposite thyristor-gates. If pulse transformers with one primary and two secondaries (1:1:1) are not available then use four pulse transformers of one primary and one secondary (1:1) as shown in Fig. 4.21.

Before thyristors are to be connected to form the bridge converter circuit shown in Fig. 4.19, one must ensure right polarity and phase of the gate pulses with respect to the polarity of the supply

voltage. The polarity and phase of the firing pulses for each thyristor can be checked as explained in Experiment No. 4. After this has been done, connect the circuit as shown in Fig. 4.19. Initially release gate pulses to only thyristors T_1 and T_3 and check whether the circuit is working as a half-wave controlled converter or not. If it is working as expected, remove gate pulses from T_1 and T_3 and release to T_2 and T_4 and examine whether the circuit works as expected.

After the above tests have been done satisfactorily, release the gate-pulses to all four thyristors T_1, T_2, T_3, and T_4. Do the following tests. Use the oscilloscope in *A-B* mode (differential mode) when observing waveforms in these tests.

Test-1 : Connect *R*-load and observe load voltage and load current waveforms as the firing angle is varied from 0 to π. Observe the input voltage and input current (voltage across R_s resistance) waveforms also.

Test-2 : Repeat the above test for an *R-L* load. Connect the oscilloscope across *R* (resistor) for observing load current waveform. Also observe the effect of the variation of *R* (resistance) on the load current (i_L) and source current (i_S) waveforms.

Test-3 : Connect a dc motor in series with a rheostat across the converter. Adjust the converter output voltage to the minimum available value. Set the rheostat to a small value. Decrease the converter firing angle to increase the motor speed. See the effect of variation of the firing angle on the motor speed. Observe the motor current and terminal voltage waveforms.

Test-4 : For inverter operation, connect the circuit as shown in Fig. 4.20 . Adjust the firing angle at more than $\pi/2$. Observe the load voltage, load current, input voltage and input current waveforms as the firing angle is varied from $\pi/2$ to little less than π. Also see the effect of the variation of the dc source on these waveforms.

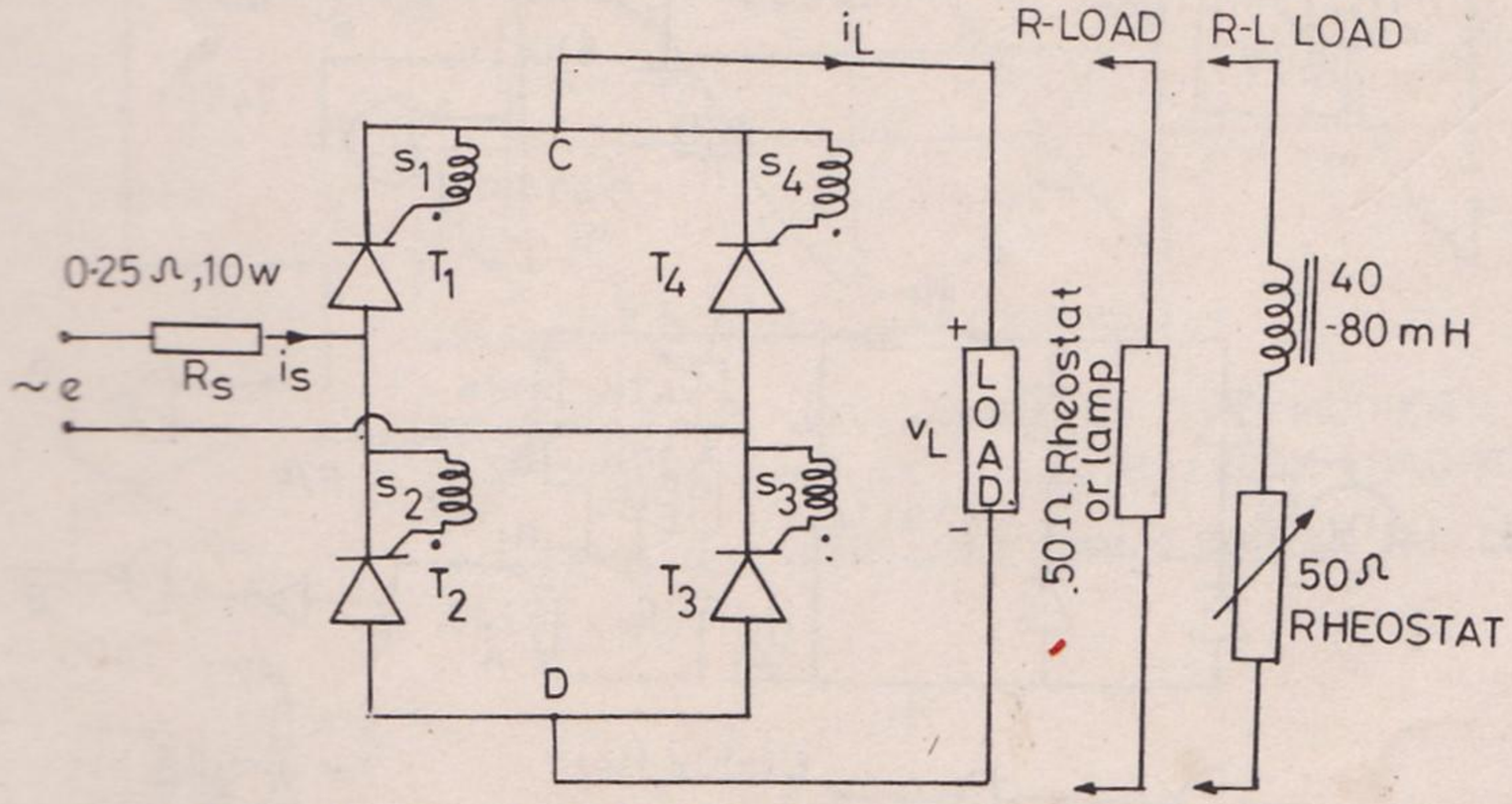


FIG.4.19: SINGLE-PHASE FULLY CONTROLLED CONVERTER

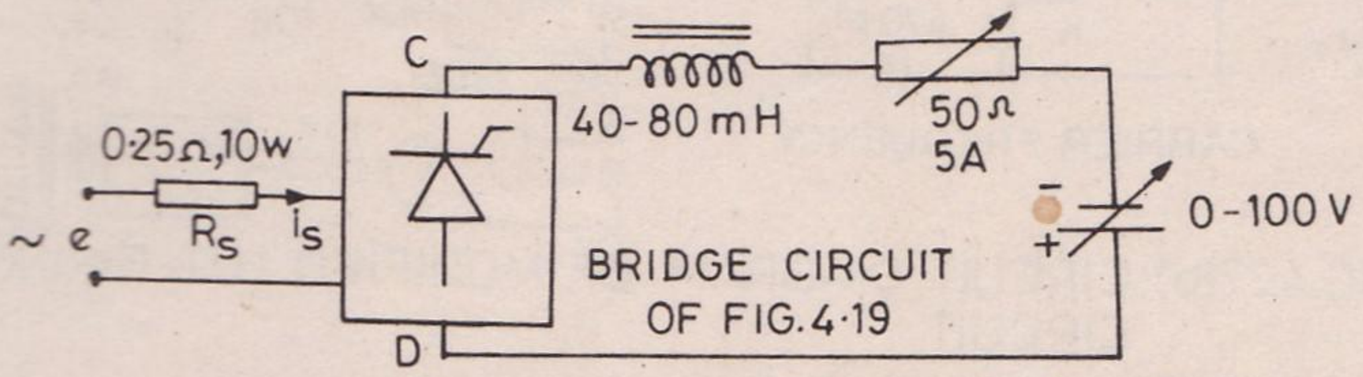
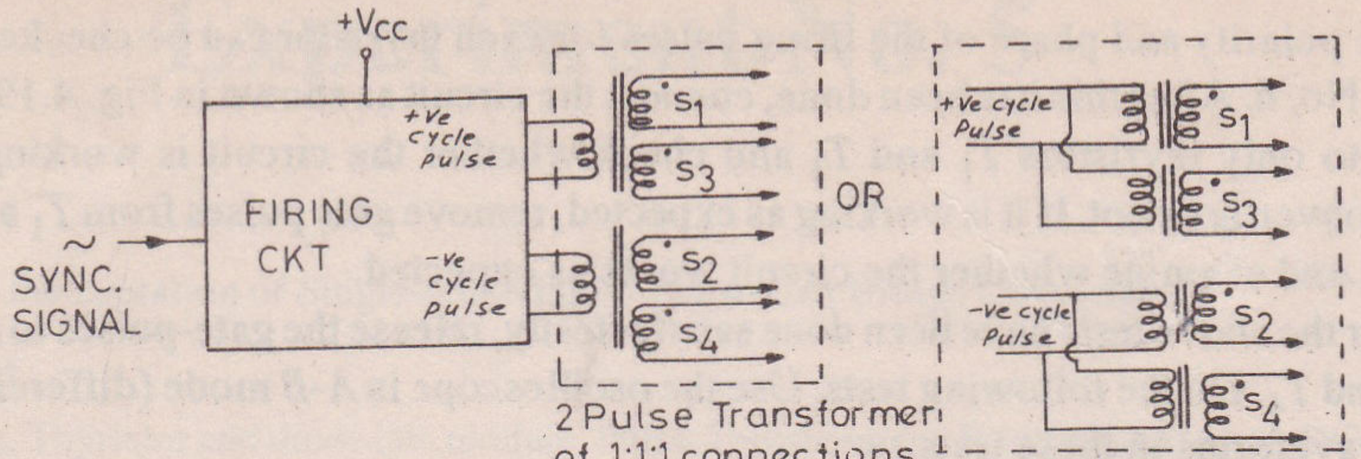
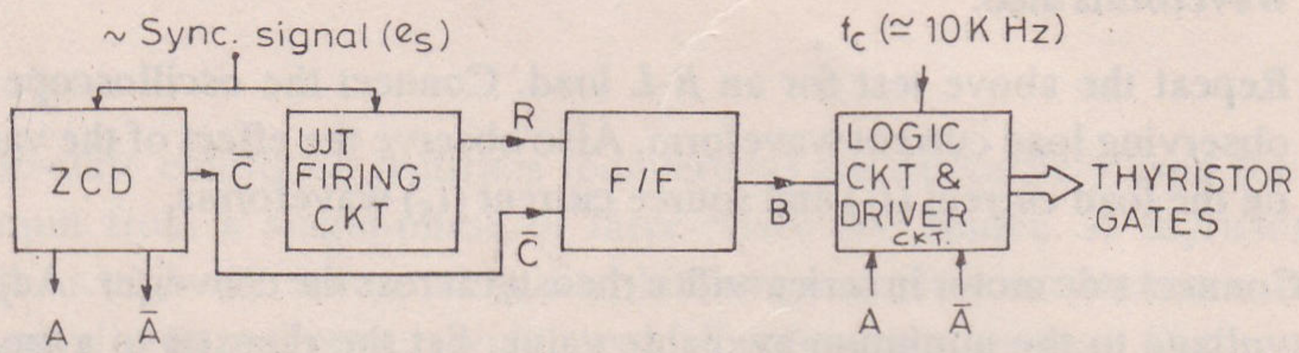


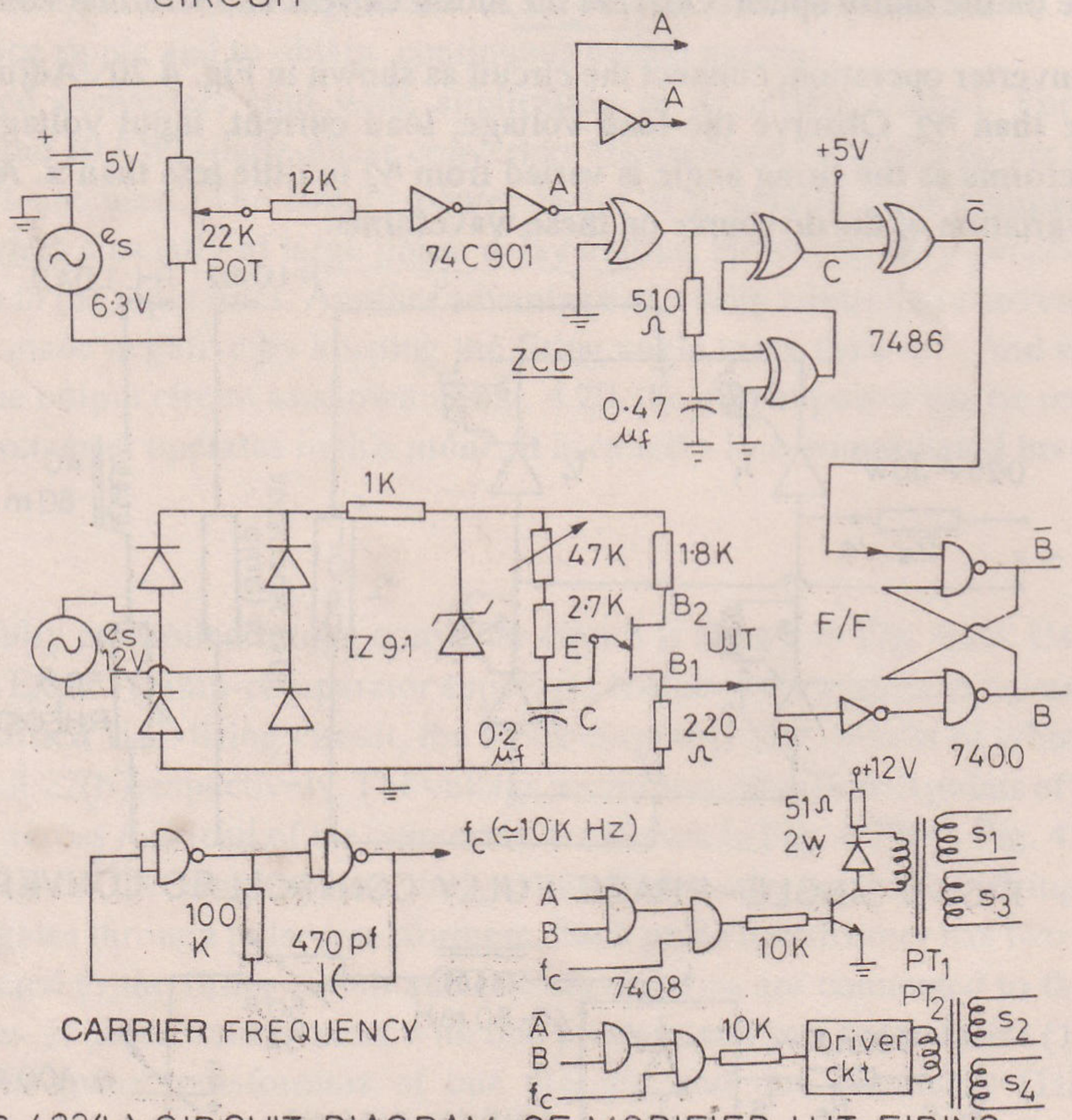
FIG.4.20: SINGLE-PHASE INVERTER OPERATION



FIG·421: PULSE TRANSFORMER CONNECTIONS



FIG·422(a): BLOCK DIAGRAM OF THE MODIFIED UJT-FIRING CIRCUIT



FIG·422(b): CIRCUIT DIAGRAM OF MODIFIED UJT-FIRING CIRCUIT

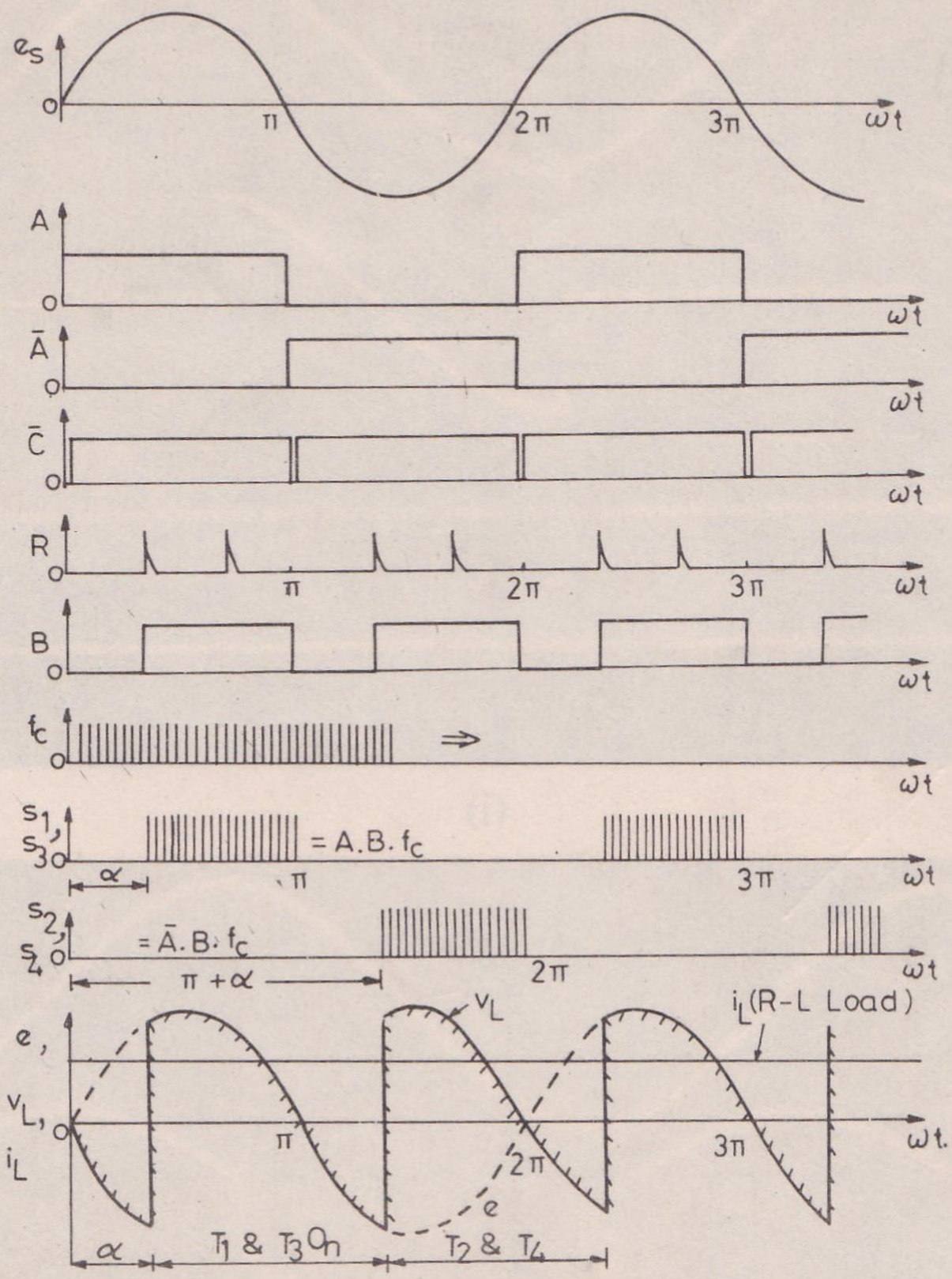
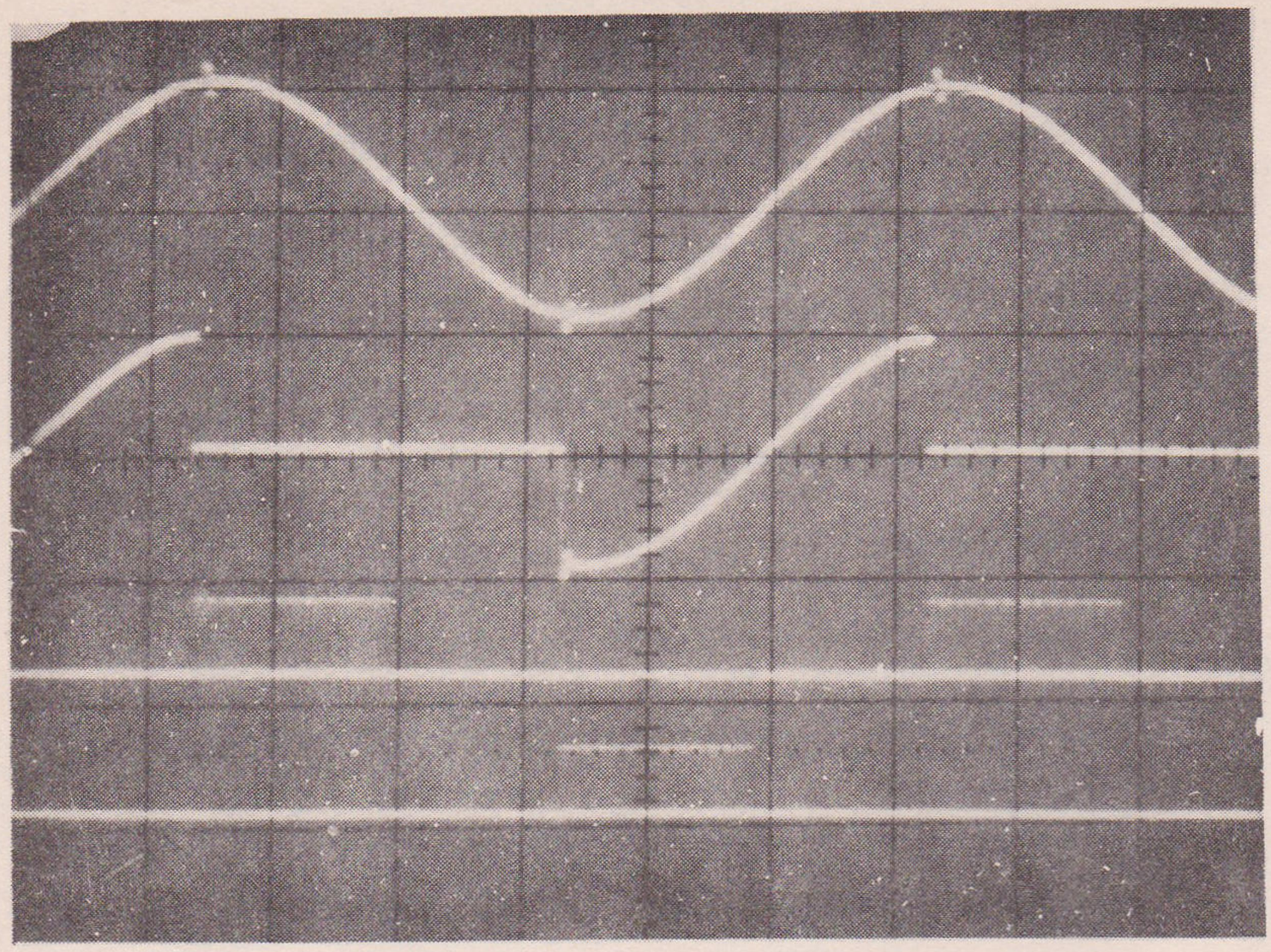
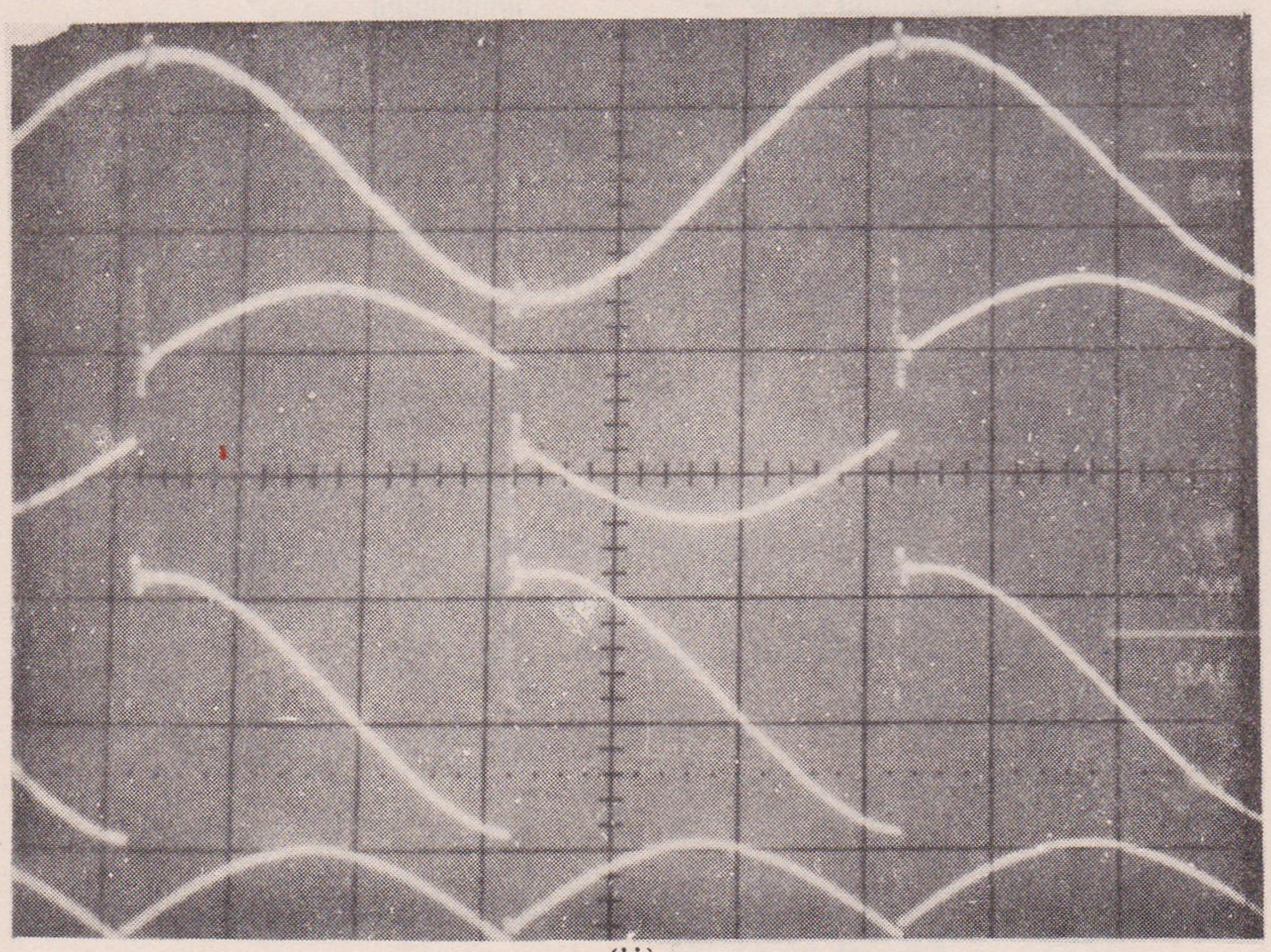


FIG.4·22(c) VOLTAGE WAVEFORMS OF THE MODIFIED UJT-FIRING CIRCUIT (FIG·4·22(b)) WITH LOAD VOLTAGE AND CURRENT WAVEFORMS FOR AN R-L LOAD (FIG. 4·19)



(i)



(ii)

FIG. 4.22(d) : OSCILLOGRAMS FOR WAVEFORMS OF SINGLE-PHASE FULLY-CONTROLLED BRIDGE CONVERTER WITH R-L LOAD (R = 10 Ω AND L = 240 mH) FOR THE TRIGGERING ANGLE (α) $\simeq 85^\circ$
(i) LINE VOLTAGE, THYRISTOR T_1 VOLTAGE AND TRIGGERING PULSES S_1 AND S_2
(ii) LINE VOLTAGE, LINE CURRENT, LOAD VOLTAGE AND LOAD CURRENT

QUESTIONS

5.1 Draw the 1–ϕ uncontrolled full-wave bridge rectifier (also called diodes bridge rectifier). Also draw and explain the waveforms of load voltage, load current and input current w.r.t. input voltage for the following loads :

(i) *R*-Load
(ii) High-inductive *R-L* load.

5.2 Draw 1–ϕ fully-controlled thyristorised converter with connected Free-wheeling diode. Also draw and explain the waveforms of the load voltage, load current and input current w.r.t. input voltage for a *R*-load and a *R-L* load.

5.3 Draw the graph between firing angle (α) and load voltage (V_L) for *R*-load and *R-L* load connected in 1–ϕ fully-controlled converter shown in Fig. 4.19.

5.4 What happens if we connect *D*-point of Fig. 4.19 with supply ground ?

5.5 Draw circuit diagram and waveforms of the load voltage, load current and input current w.r.t. input voltage for *R*-load and *R-L* load connected to 1–ϕ fully-controlled converter fabricated by two thyristors and a transformer. Which type of transformer is required ?

Experiment No. 6

Objective : Single-phase half-controlled Symmetrical and Asymmetrical bridge converters.

Apparatus Required

Oscilloscope, Thyristor and diode lab. module, Pulse-Transformers, Rheostat, Inductor, DC motor, Any one fabricated converter firing circuit, 230*V* :6V to 15 *V* transformer for synchronization, Shunts (low value and high voltage resistance for tracing current waveform at any place of the circuit on the oscilloscope) and Low voltage dc power supply.

Description

Fig. 4.23(a) shows a single-phase half-controlled symmetrical bridge converter circuit. Since thyristors and diodes conduct for equal intervals of π, in each cycle of the power supply, this circuit is known as symmetrical type. Fig. 4.24(a) shows a single-phase half-controlled asymmetrical bridge converter circuit where thryistors and diodes conduct for unequal intervals with inductive load. These bridge circuits of Fig. 4.19, Fig. 4.23(a) and Fig. 4.24(a) are also known as two-pulse converters, since there are two pulses of load current in each supply cycle. With the increase in the pulse number, the output voltage ripple and harmonic contents in the input supply current decrease and supply power factor improves.

A half-controlled converter has a number of advantages compared to a fully-controlled converter. Few of these are: low cost, good power factor and low load current ripple. The disadvantages are: higher harmonic content in the source current and since the output voltage cannot be made negative, inverter-operation is not possible.

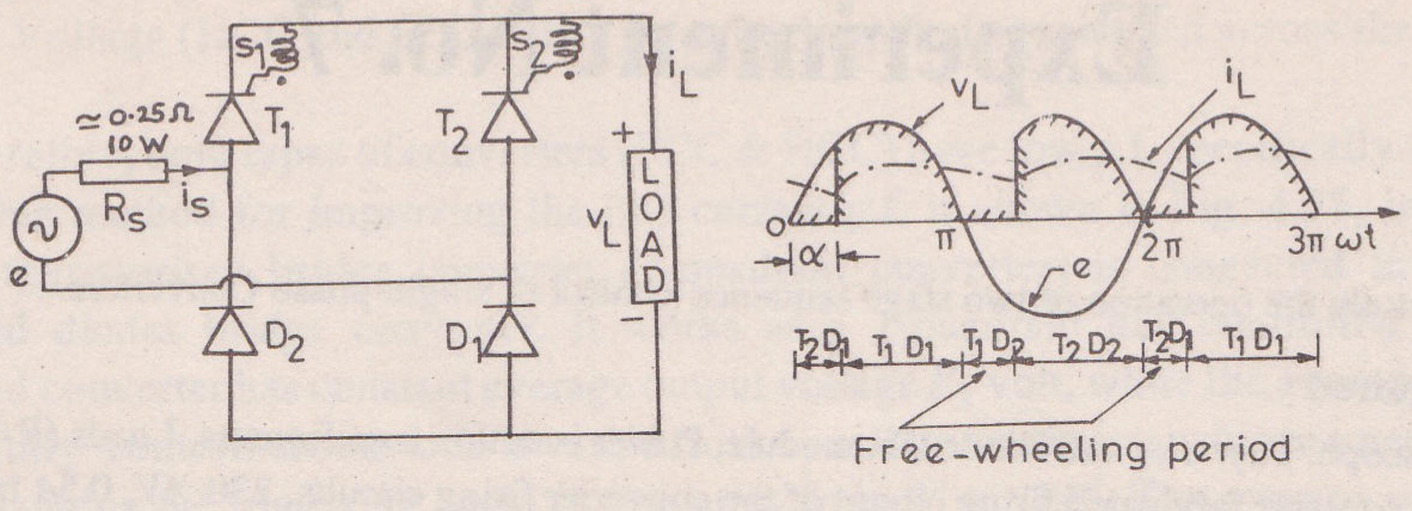
The symmetrical half-controlled converter may switch into 'Half-Waving' effect, with highly inductive loads when the firing pulses are inhibited. As a result of this, the output voltage becomes uncontrolled half-wave. But the asymmetrical converter cannot switch into 'Half-Waving' effect, since the load current freewheels through both diodes in each half-cycle.

Procedure

Connect two thyristors and two-diodes of the power module to form the half-controlled symmetrical converter circuit as shown in Fig. 4.23(a). Use any firing circuit of Experiment No. 3 or modified UJT-firing circuit shown in Fig. 4.22. In this Experiment only two pulse transformers each with one primary and one secondary winding, are required. For ensuring the right phase and polarity of the gate pulses (with respect to the supply voltage), test the polarity and phase of gate pulses for each thyristor, as explained in Experiment No. 4. Initially release gate pulses to only Thyristor T_1 and check whether the circuit is working properly or not. If it is working as expected remove gate pulses from T_1 and release T_2 and examine whether the circuit works as expected.

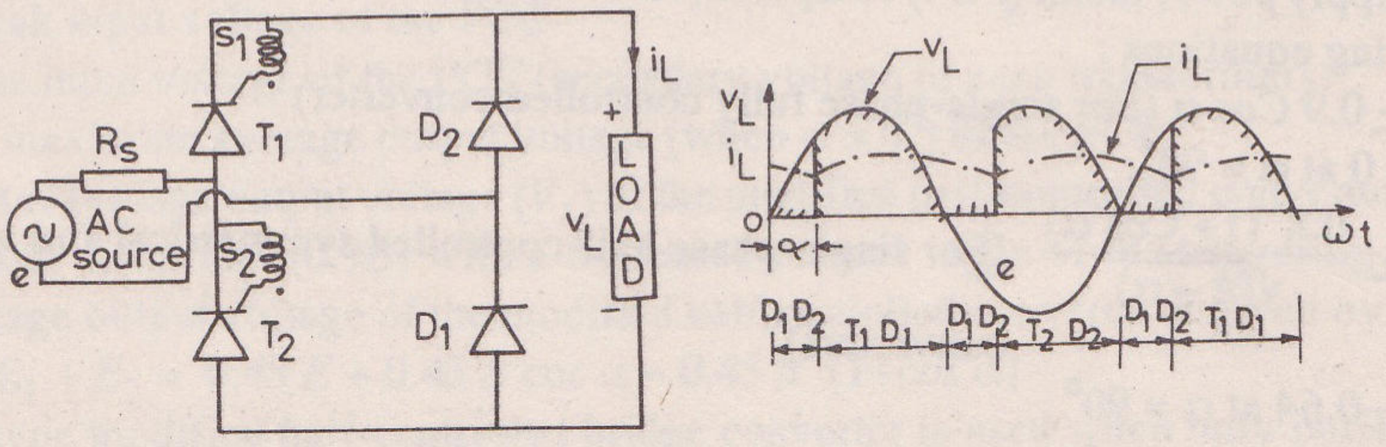
Release the gate pulses to both thyristors T_1 and T_2. Do the tests 1, 2 and 3 of Experiment No. 5. Compare waveforms of the single-phase half-controlled converter with the waveforms of the single-phase fully-controlled converter for each test.

Test-4 : Repeat tests 1, 2 and 3 with asymmetrical converter circuit of Fig. 4.24.



(a) CIRCUIT DIAGRAM (b) LOAD VOLTAGE AND CURRENT WAVEFORMS FOR R-L LOAD

FIG.4·23: SINGLE-PHASE HALF CONTROLLED SYMMETRICAL CONVERTER



(a) CIRCUIT DIAGRAM (b) LOAD VOLTAGE AND CURRENT WAVEFORMS FOR R-L LOAD

FIG.4·24 :SINGLE-PHASE HALF-CONTROLLED ASYMMETRICAL CONVERTER

QUESTIONS

6.1 What are the advantages and disadvantages of a half-controlled converter as compared to a fully-controlled converter ?

6.2 What is the difference between 1–ϕ half-controlled symmetrical and asymmetrical converters and why one is called symmetrical converter ?

6.3 What happens if common anodes point of the diodes D_1 and D_2 of half-controlled symmetrical converter (Fig. 4.23) is connected with supply ground ?

6.4 What happens if common anodes point of a diode D_1 and a thyristor T_2 of the half-controlled asymmetrical converter (Fig. 4.24) is connected with supply ground ?

6.5 What happens if we connect a free-wheeling diode in the 1–ϕ half-controlled symmetrical converter with an *R-L* load ?

6.6 What is "half-waving" effect and when can it occur in both types 1–ϕ half-controlled converters (symmetrical and asymmetrical) ?

Experiment No. 7

Objective : To study the operation of two stage sequence control of single-phase Converters. .

Apparatus Required

Oscilloscope, Thyristor and Diode lab. module, Power isolation transformers, Loads (*R*-load, *R-L* load and DC motor), Any one fabricated firing circuit of the converter firing circuits, 230 :6*V*, 0.5*A* transformer for synchronization, Pulse-Transformers, Shunts and Low voltage dc power supply.

Description

The fully-controlled converters (FCC) generate less harmonic currents in the input lines but have a poor supply power factor (*P.F.*) compared with the half-controlled converters (HCC) as shown by the following equations :

$P.F \simeq 0.9 \cos \alpha$ (For single-phase fully controlled converter)

$\simeq 0$ at $\alpha = 90^\circ$

$P.F. \simeq \dfrac{0.8\ (1+\cos \alpha)}{\sqrt{(\pi - \alpha)}}$ (For single-phase half-controlled symmetrical and asymmetrical converters)

$P.F \simeq 0.64$ at $\alpha = 90^\circ$

and Distortion factor, $\mu = \dfrac{I_1}{I}$

where I_1 : Fundamental component of line current (rms)

I : RMS line current

α : Triggering angle of thyristors

$$P.F. = \frac{\text{active power}}{\text{apparent power}} = \frac{EI_1 \cos \phi}{EI}$$

$$= \frac{I_1}{I} \cos \phi = \mu \cos \phi$$

where ϕ : Phase difference between input voltage (E) in rms and rms value of the fundamental component of the line current (I_1)

$\cos \phi$: Displacement factor or fundamental *p.f.*

$\mu = \dfrac{2\sqrt{2}}{\pi} \simeq 0.9$ (For fully-controlled converter)

and

$$\mu = \frac{2\sqrt{2}\ \cos \alpha/2}{\sqrt{\pi\ (\pi - \alpha)}} \simeq \frac{1.596\ \cos\ \alpha/2}{\sqrt{(\pi - \alpha)}}$$

(For half-controlled symmetrical and asymmetrical converters and FCC with a freewheeling diode connected across the load)

$\simeq 0.9$ at $\alpha = 90^\circ$

$\simeq 0.57$ at $\alpha = 150^\circ$.

The higher value of the distortion factor (μ) of a line indicates lower magnitude of harmonics in the line current.

Output voltage (FCC) $\simeq 0.9\,E\,\text{Cos}\alpha$)
and Output Voltage (HCC and FCC with a freewheeling diode connected across the load) $\simeq 0.45\,E$ $(1+\text{Cos}\alpha)$

Therefore, both types of converters (FCC & HCC) have low p.f. specifically for lower output voltages. One method for improving the line current p.f. is shown in Fig. 4.25, in which a fully-controlled thyristorised bridge converter (2-quadrant converter) is connected in series with an uncontrolled diodes bridge converter. It works as a 1-quadrant half-controlled converter. The uncontrolled converter has constant average output voltage E_1 volt, while the average output voltage (E_2) of the fully- controlled converter is varied from a positive maximum value to a negative minimum value by changing the triggering angle of thyristors from 0° to 180°. The average output voltage of the fully-controlled converter (FCC) is given by equation :

$$E_2 = \frac{2E_p}{\pi}\cos\alpha = \frac{2E}{\sqrt{2}\pi}\cos\alpha = 0.45E\cos\alpha$$

or $E_{2m} \simeq \pm 0.45\,E$
and E_1 (average output voltage of diodes bridge converter) $\simeq 0.45E$
where E_p: peak input voltage of the FCC
E : rms input voltage of the FCC (secondary voltage of each transformer)
and E_{2m} : maximum average output voltage (when $\alpha = 0^\circ$) of the FCC
So, the resultant average output voltage (V_L) of the modified half-controlled converter is varied from virtually zero to maximum $(0.9E)$ with a decreased control range of the triggering angle (α). The resultant average output voltage of the modified half-contolled converter is given by

$$V_L = E_1 + E_2 = 0.45\,E + 0.45\,E\cos\alpha = 0.45\,E\,(1+\cos\alpha)$$

This type modified half-controlled bridge converter is used when only positive variable dc voltage from 0 to $0.9E$ volts is required. If the variable load voltage required from zero to maximum (the sum of maximum average output voltage of all employed converters in the multi stage sequence control converter) with improved line *p.f.* then two or more than two stage sequence control of half-controlled converters can also be employed. In these type converters, the output voltage (V_L) cannot become negative, so inverter operation is not possible.

When negative output voltage (i.e., inversion) is required with improved line p.f., then two or more than two FCC are connected in series. And each bridge is triggered sequencely.

Sequence Control

In two stage sequence control (used converter in each stage may be any type, i.e., FCC or HCC), the variable output voltage from 0 to E_{1m} (maximum output voltage of 1st converter) is obtained by controlling first converter and bypassing other converters. If the variable load voltage is required between E_{1m} and E_{2m} volts then 1st converter is triggered at 0° triggering angle and other converter is controlled according to the required output voltage. This type of operation of converters, is called sequence control of series converters.

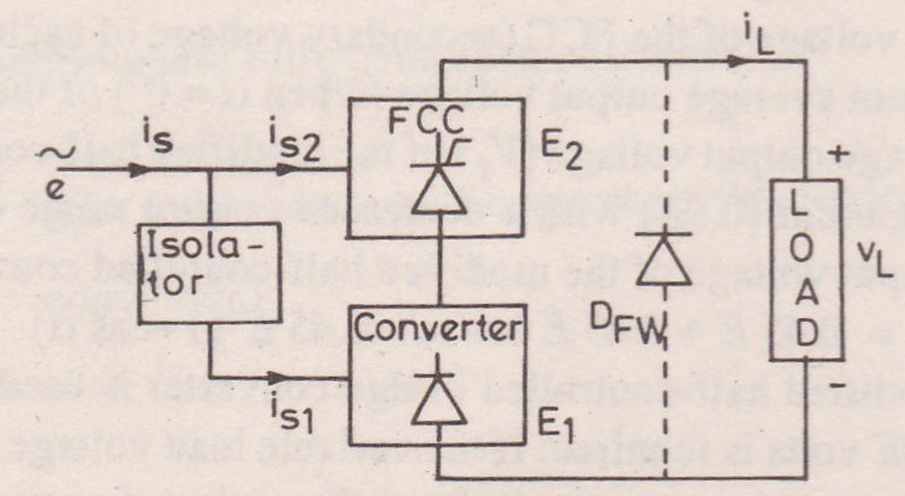
Procedure

Make a single-phase full-wave uncontrolled diode bridge converter (FW—UCC) and a fully-controlled thyristorised bridge converter (FCC). Interconnect these power converters in series

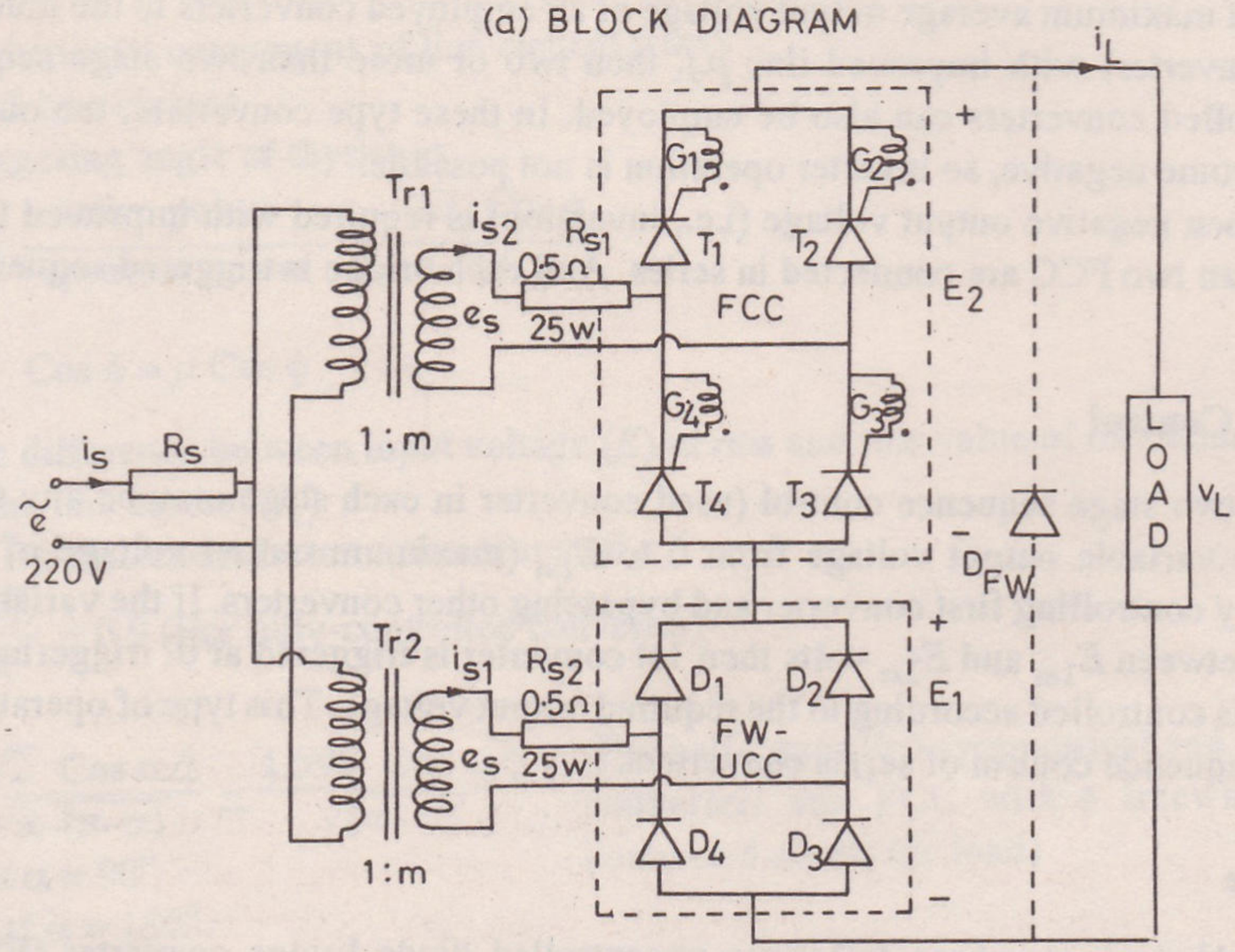
as shown in Fig. 4.25. *Isolation between the power supplies of each converter is a must, otherwise converters will produce short-circuit in the power supply.* So connect at least one converter to the power supply through power transformer. Connect a high value inductor in series with load (i.e., make the load highly inductive for maintaining nearly a constant current I_L through the two bridges and load). Use any one of the firing circuits from Experiment No. 3 (Op-amp, Digital, Cosine-Wave Scheme or a simple Ramp Comparator Scheme) and modified UJT-firing circuit which is shown in Fig. 4.22(a and b).

The firing pulses are delivered to thyristor-gate through pulse transformers. Each pulse transformer has two secondaries. The primary is connected to the firing circuit and two secondaries are connected to the diagonally opposite thyristor-gates. If pulse transformers with one primary and two secondaries (1:1:1) are not available then use four pulse transformers of one primary and one secondary (1:1) as shown in Fig. 4.21.

Before releasing the firing pulses to thyristors of the bridge converter circuit shown in Fig. 4.25, one must ensure right polarity and phase of the gate pulses with respect to the phase of the supply voltage. The polarity and phase of the firing pulses for each thyristor can be checked by the following easy methods.



(a) BLOCK DIAGRAM

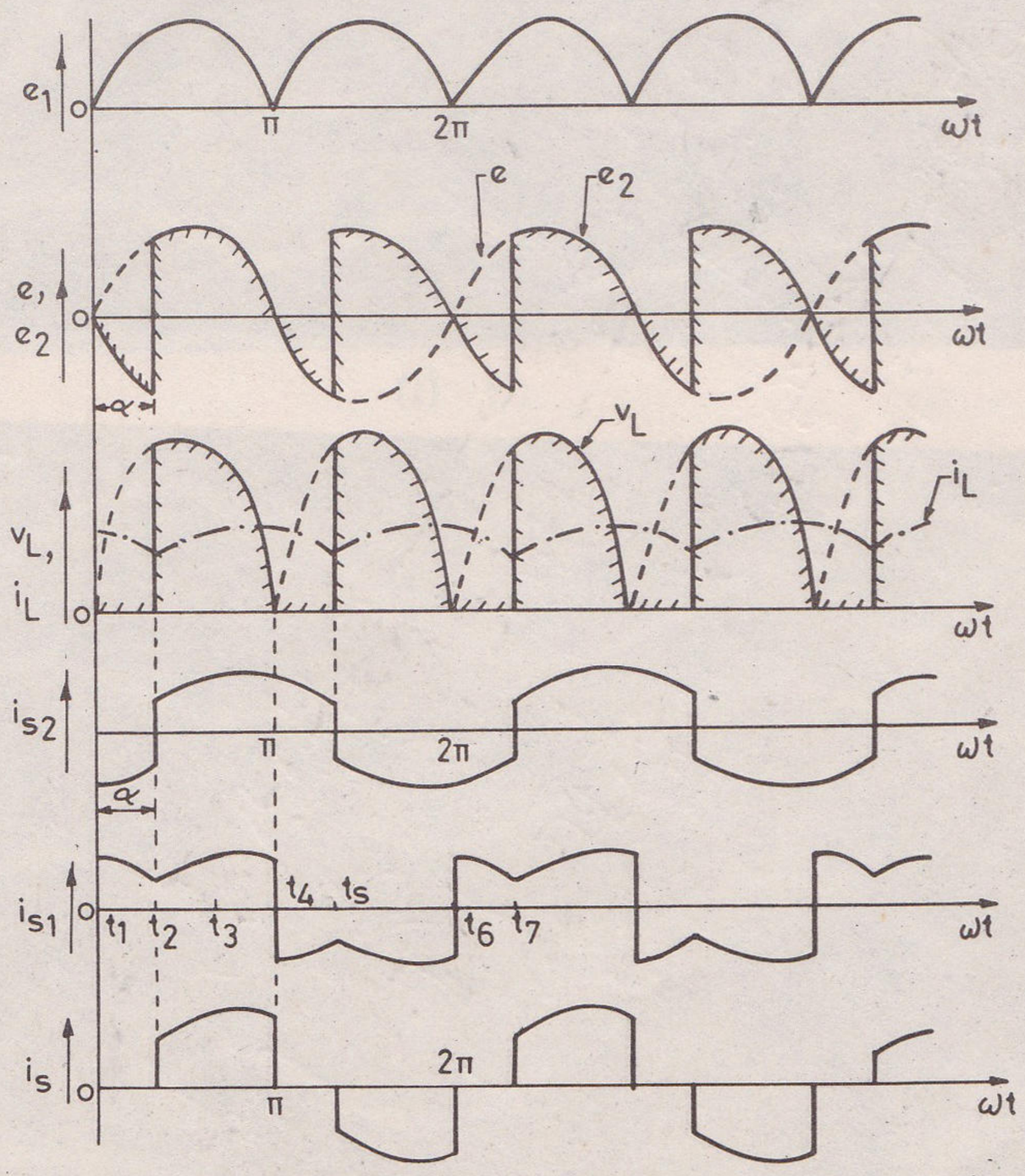


(b) CONNECTION DIAGRAM

FIG. 4·25: MODIFIED HALF-CONTROLLED CONVERTER CONSISTING OF TWO CONVERTERS IN SERIES

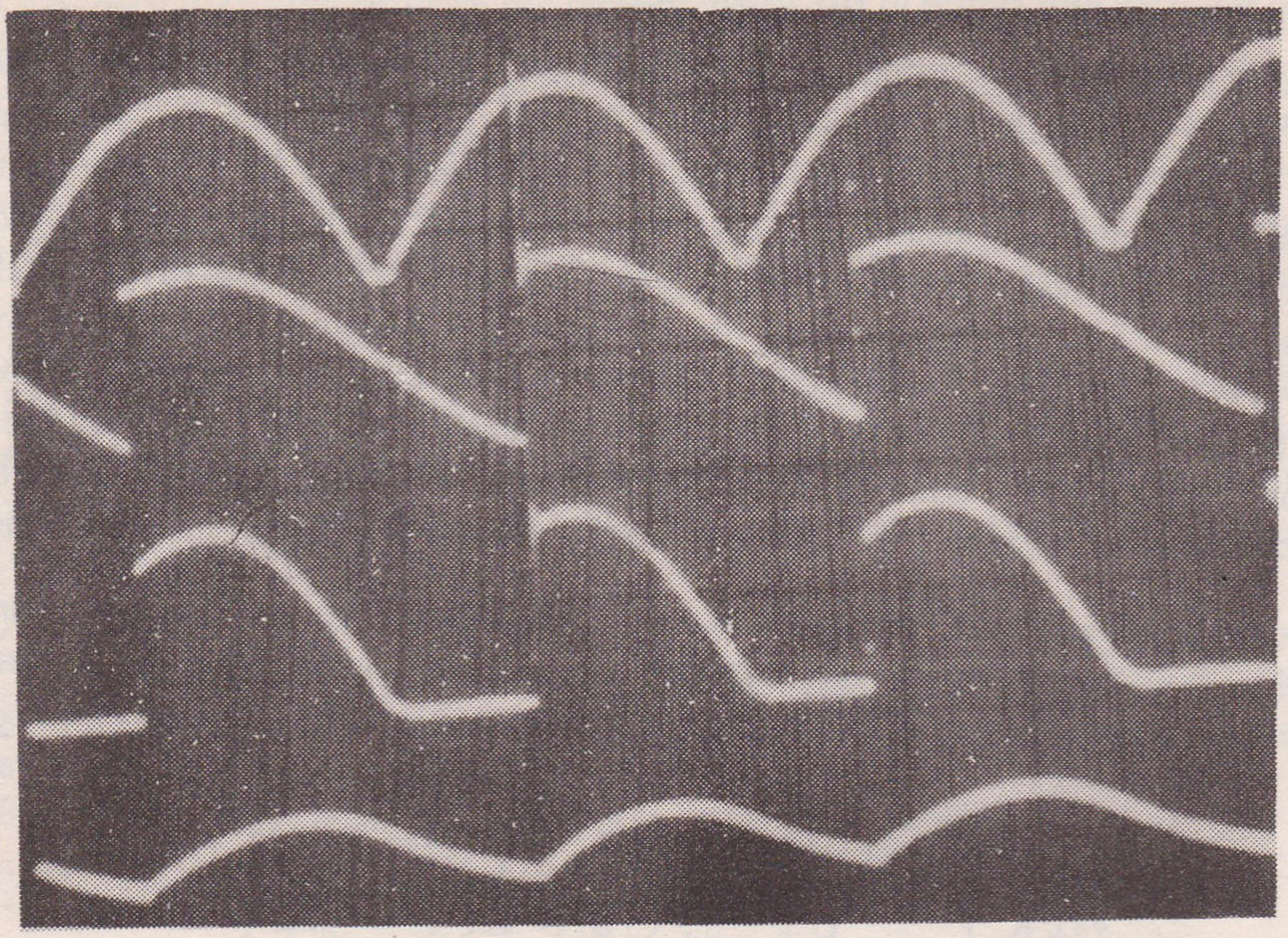
Testing the polarity and phase of the firing pulses

Disconnect the power supply from the FW-UCC of the modified half-controlled converter shown in Fig. 4.25. And also open the connections between gates of thyristors. Short the anode and cathode of T_3 thyristor. Connect common terminal of both probes of the oscilloscope with cathode of T_1 thyristor. Connect other lead of one probe with anode of T_1 thyristor and second probe's opened lead with opened terminal of the secondary of pulse-transformer G_1. If the firing pulses are coming in the negative half-cycle then interchange the power supply terminals of FCC or the synchronising single ($\simeq 6v$) terminals of the firing circuit. Now, do not interchange power supply terminals of FCC and the synchronisation single of the firing circuit during the experiment and test the polarity and phase of the firing pulses for other thyristors. If firing pulses have negative polarity then interchange the connections of the secondary terminals or primary terminals of the pulse transformer G_1.

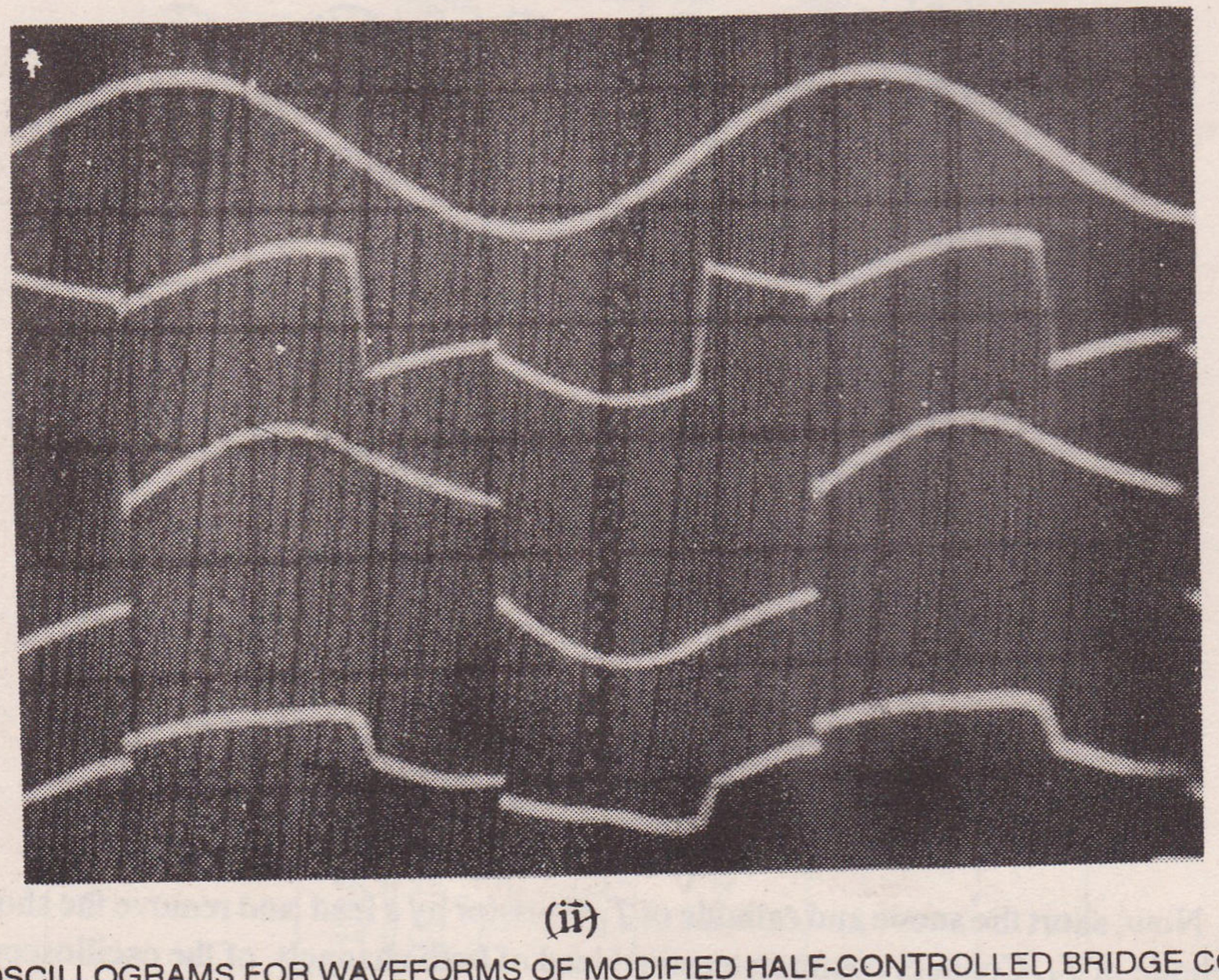


FIG·4·26: WAVEFORMS AT DIFFERENT STAGES OF FIG·4·25 FOR AN R-L LOAD (Without connecting free wheeling diode, D_{FW})

Now, short the anode and cathode of T_1 thyristor by a lead and remove the short lead of anode and cathode of T_3. Connect common terminal lead of both channels of the oscilloscope with cathode of T_3 and one channel lead with anode of T_3 while other channel lead with unconnected secondary terminals of G_3 pulse-transformer. Firing pulses must come in the positive half-cycle of the supply. If firing pulses are coming in the negative half-cycle then you have connected the probes wrongly. Check probes connection again and if the polarity of the pulses are negative then interchange the gate



(i)

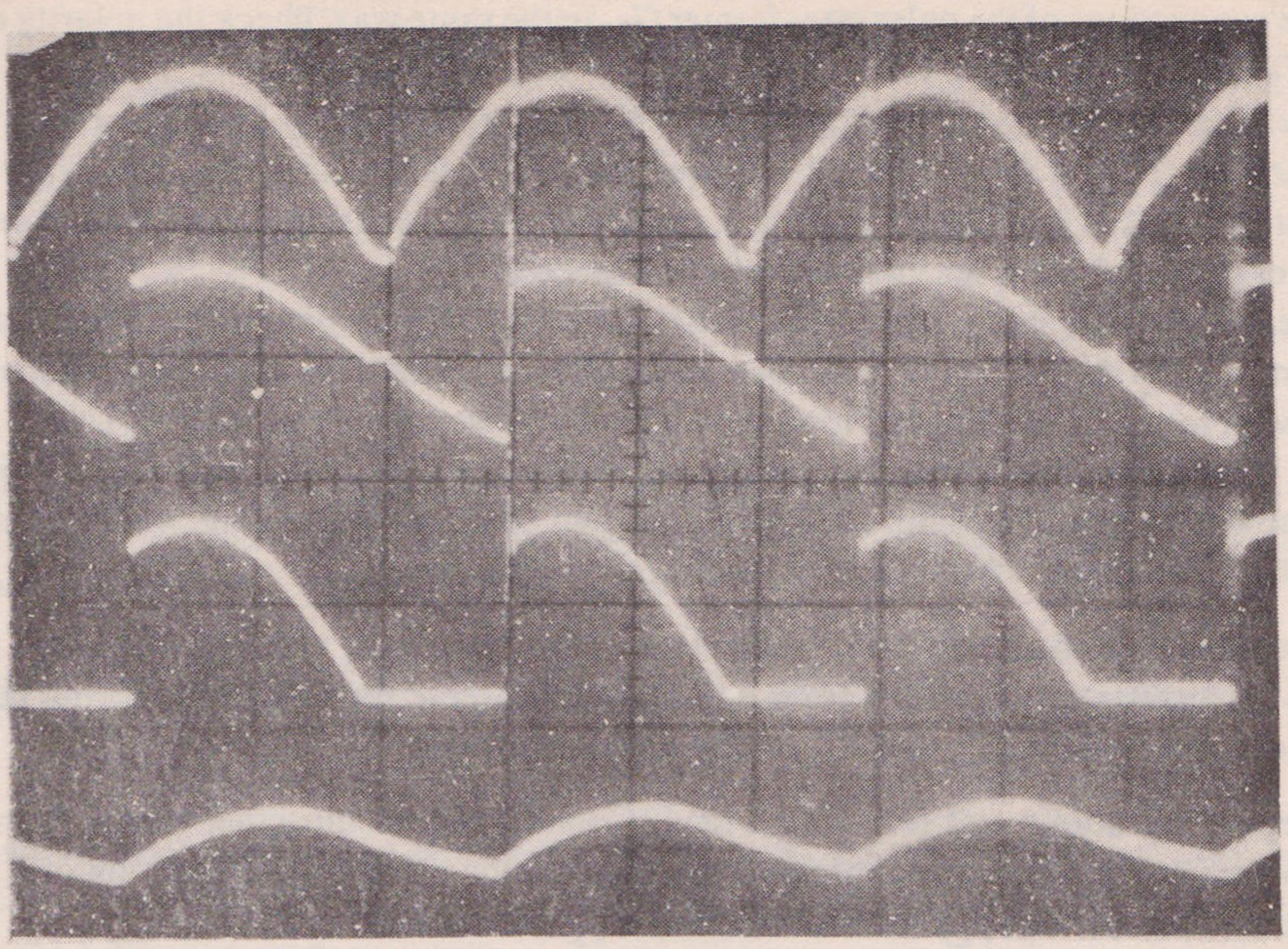


(ii)

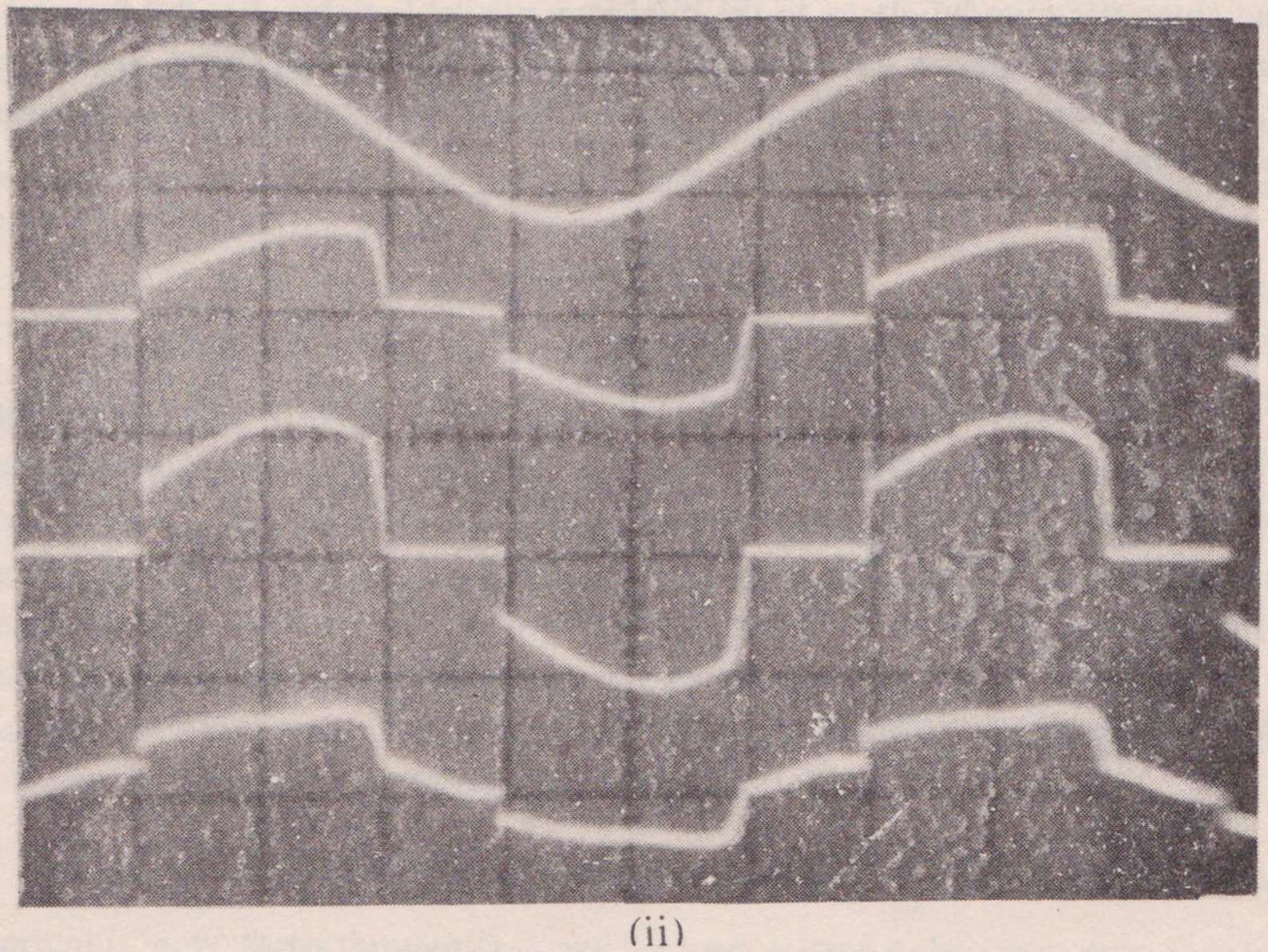
FIG. 4.27 : OSCILLOGRAMS FOR WAVEFORMS OF MODIFIED HALF-CONTROLLED BRIDGE CONVERTER (TWO STAGE SEQUENCE CONTROL OF SERIES CONVERTER) WITH R-L LOAD (R = 10 Ω AND L = 240 mH) AND WITHOUT FREE-WHEELING DIODE

(i) OUTPUT VOLTAGE OF THE DIODES BRIDGE, OUTPUT VOLTAGE OF THE THYRISTORS BRIDGE, LOAD VOLTAGE AND LOAD CURRENT

(ii) LINE VOLTAGE, INPUT CURRENT OF DIODES BRIDGE, INPUT CURRENT OF THYRISTORS BRIDGE AND LINE CURRENT



(i)



(ii)

FIG. 4.28 : OSCILLOGRAMS FOR WAVEFORMS OF MODIFIED HALF-CONTROLLED BRIDGE CONVERTER (TWO STAGE SEQUENCE CONTROL OF SERIES CONVERTER) WITH R-L LOAD (R = 10 Ω AND L = 240 mH) AND WITH FREE-WHEELING DIODE

(i) OUTPUT VOLTAGE OF THE DIODES BRIDGE, OUTPUT VOLTAGE OF THE THYRISTORS BRIDGE, LOAD VOLTAGE AND LOAD CURRENT

(ii) LINE VOLTAGE, INPUT CURRENT OF DIODES BRIDGE, INPUT CURRENT OF THYRISTOI BRIDGE AND LINE CURRENT

and cathode connections of the pulse transformer G_3. In the same way, check the polarity of the firing pulses for T_2 and T_4 thyristors.

After this has been done, connect the pulse transformers properly. Initialiy release gate pulses to only thyristors T_1 and T_3 and check whether the circuit is working as a half-wave controlled converter or not. If it is working as expected, remove gate pulses from T_1 and T_3 and release to T_2 and T_4 and examine whether the circuit works as expected.

After the above tests have been done satisfactorily release the gate-pulses to all four thyristors T_1, T_2, T_3 and T_4. Do the following tests. Use the oscilloscope in *A-B* mode (differential mode) when observing waveforms in these tests. Now, switch on the power supply of the FW-UCC.

Fig. 4.26 shows the waveforms at different stages of Fig. 4.25 for an *R-L* load. Fig. 4.27 and F.g. 4.28 show oscillograms of the waveforms for two stage converter (Fig. 4.25) for an *R-L* load without and with connected freewheeling diode (D_{FW}) respectively.

Test-1 : Connect R-load and observe load voltage, load current, e_1 voltage, e_2 voltage waveforms as the firing angle is varied from 0 to π. Also observe the input voltage and input current (voltage across R_s, R_{s1} and R_{s2} resistances) waveforms.

Test-2 : Repeat the above test for an *R-L* load. Connect the oscilloscope across *R* (resistor) for observing load current waveform. Also observe the effect of the variation of *R* (resistance) on the load current (i_L) and source current (i_s) waveforms.

Test-3 : Connect a dc motor in series with a rheostat (for limiting current) across the converter. Adjust the converter output voltage to the minimum available value. Set the rheostat to a small value. Decrease the converter firing angle to increase the motor speed. See the effect of the variation of firing angle on the motor speed. Observe the motor current and terminal voltage waveforms.

QUESTIONS

7.1 What are the advantages of half-controlled converters over fully-controlled converters ?

7.2 Draw a two stage sequence control of 1-phase fully-controlled converter. Explain its working and merits.

7.3 Why is the isolation required between the power supplies of the fully-controlled converter and the uncontrolled converter in the Modified Half-controlled Bridge Converter (Fig. 4.25) ?

7.4 Draw waveforms at some important points of Fig. 4.25 with *R-L* load. And explain why the main power supply current has zero value two times in a cycle while load has continuous current.

7.5 Draw the circuit diagram of a two-stage sequence-controlled half-controlled converter. And write some of its advantages over the single half-controlled converter.

Experiment No. 8

Objective : To study the step-down Thyristorised Choppers.

8.1 : Current Commutated Thyristorised Chopper

8.2 : Voltage Commutated Thyristorised Chopper

Apparatus Required

Oscilloscope, Thyristor and Diode module, Air-core inductor ($\simeq 1mH, 5A$), Capacitor ($\simeq 20\ \mu F, 400V$), Shunts, DC Source, Fabricated Thyristorised Chopper firing circuit, Low voltage power supply for firing circuit, Loads (R-load, R-L load and dc motor).

8.1 THE CURRENT COMMUTATED STEP-DOWN THYRISTORISED CHOPPER

Theory

A current commutated thyristor chopper is shown in the Fig. 4.29(a). The main thyristor (T_m) is commutated by a reverse current pulse generated by the commutation circuit. The chopper circuit operates in the following modes :

Mode I : The commutating capacitor C is already charged to $+E$ voltage from the source E_s through resistor R. The thyristor T_m and T_a are respectively triggered by pulses G_m and G_a shown in Fig. 4.32 and Fig. 4.34. The source voltage E appears across the load and the load current i_L flows through T_m.

Mode II : Due to this turn-on of the thyristor T_a, the capacitor C is charged to a reverse voltage E as the L-C forms a resonant circuit. See waveform e_c of Fig. 4.30. When the capacitor current i_c reaches zero (position b' in Fig. 4.30) thyristor T_a turns off.

Mode III : Current i_c flows through thyristor T_m in the opposite direction to that of load current i_L. The load current i_L is assumed constant during commutation process since the commutation interval is very small compared to the load time constant. Thyristor T_m is turned off when $i_c = I_L$ (point c' shown in the Fig. 4.30).

Mode IV : Soon after T_m is turned off, diode D_2 conducts as it is forward biased. The load current I_L and the capacitor current flow through D_2 (the forward current in D_2 is then i_c-i_L). When $i_c = I_L$ (Point d' in the Fig. 4.30), diode D_2 stops conducting as the current through it, becomes zero and then it gets reverse biased.

Mode V : Now the load currrent flows through E_s, C, L, D_1 and the load. Capacitor C is charged to voltage E of the positive polarity with the constant load current i_L. When the capacitor fully charges to E, the load current stops flowing through E, C, L and D_1.

Mode VI : The freewheeling diode D_{FW} now conducts due to $L.\ \frac{di_L}{dt}$ voltage developed by the load. The load current i_L, now, flows through D_{FW} and the load voltage e_L becomes zero. Due to the stored energy in the inductor $L\ \left(\frac{1}{2} L\ i_L^2\right)$, the capacitor is charged little over E.

Mode VII : The overcharge on capacitor C is reduced due to the current flowing through resistor R, C E_s in the reverse direction, while the load current freewheels.

The modes of operation corresponding equivalent circuits and waveforms of the chopper of Fig. 4.29(a) with *R*-load and *R-L* load, are shown in Fig. 4.29(b) and 4.30 respectively.

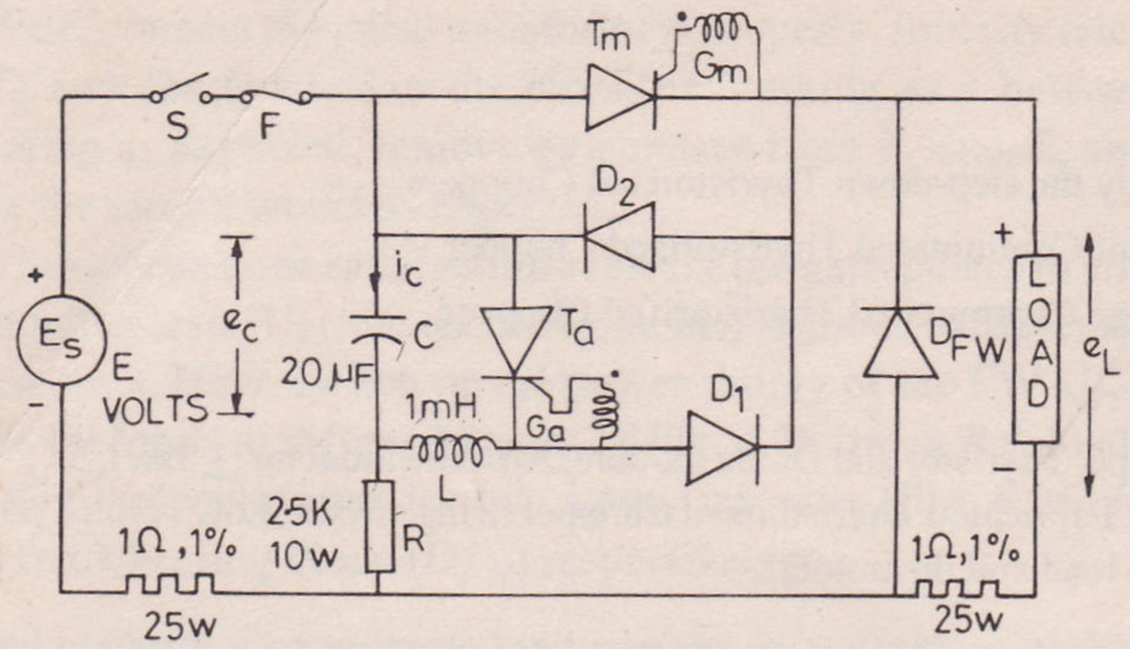


FIG.4.29(a): CURRENT COMMUTATED THYRISTORISED CHOPPER

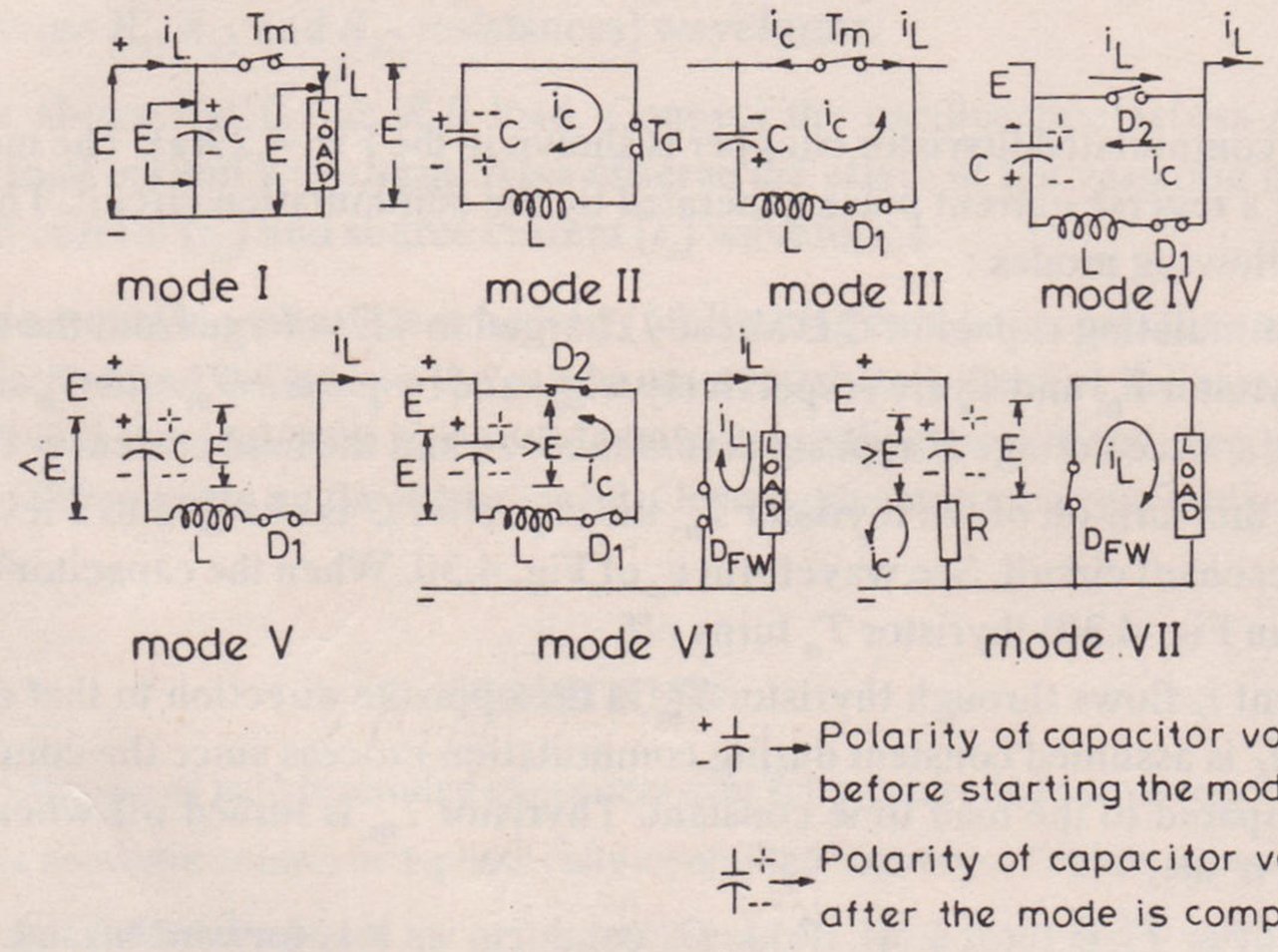


FIG.4.29(b): MODES OF OPERATIONS OF THE CHOPPER (FIG.4.29 a)

Firing circuit (Fig. 4.31)

The triggering circuit for the thyristor chopper of Fig. 4.29 is shown in Fig. 4.31. And waveforms at different points of the firing circuit are shown in Fig. 4.32. In the circuit of Fig. 4.31, a UJT relaxation oscillator is used as a variable frequency ramp generator. The pulses at point *B* are applied to the input of the monostable multivibrator through an inverter for generating the pulses of the duration which is sufficient for turning on thyristor T_m. The output pulses of monostable (point *D*) are applied to the driver circuit of the main thyristor T_m.

The ramp (waveform *A* of the Fig. 4.32) and the variable dc voltage, which controls t_{on} and t_{off} period of the chopper, are compared in the comparator *IC* 741. The output of the comparator (waveform-*E*) is applied to the differentiator circuit and its output (waveform-*F*) is used to trigger the auxiliary thyristor T_a through a driver circuit.

Alternative Triggering Circuit

Another triggering circuit for the chopper of Fig. 4.29 is shown in Fig. 4.33 and its waveforms are shown in Fig. 4.34. A variable frequency rectangular waveform (frequency 30 Hz to 330 Hz) is generated by the astable oscillator *NE*555. The durations t_h and t_l of the rectangular wave (waveform *A* in Fig. 4.34) are given by the following equations :

$$t_h = 0.7\,(R_a + R_b)\,C \tag{4.1}$$

$$t_l = 0.7\,R_b.C \tag{4.2}$$

Therefore, the total period

$$T = T_h + T_l = 0.7\,(R_1 + 2R_b).\,C \tag{4.3}$$

The leading edge of the rectangular wave *A*, is used to trigger the monostable *IC* 74121. The pulse (waveform at point *B*) of the duration ($\simeq$ 0.13 ms) which is sufficient for turning-on the main thyristor T_m, is generated at the output of the monostable. It is given by

$$t_h = 1.1\,RC \tag{4.4}$$

The saw-tooth waveform is produced at the output of the Op-amp integrator circuit (waveform at point *C*). The rising part of the saw-tooth waveform follows the equation.

$$e_o = \frac{1}{RC}\int_o^t e_i\,dt \tag{4.5}$$

But the input voltage (e_i) is constant (v_i), so the output (e_o) of the Integrator circuit is

$$e_o = \frac{V_i}{RC}\,t$$

The saw-tooth wave is added to a variable dc voltage by a op-amp adder circuit, and is compared with a dc voltage. The output of the comparator (*G*-waveform) is applied to the monostable circuit. The output of the monostable (*H*-waveform) is used to trigger the auxiliary thyristor T_a and its triggering instant can be controlled by 27*K* Pot P_2.

Testing Procedure

Consider any one of the chopper triggering circuits of Figs. 4.31 and 4.33. Check whether the circuit is working as expected.

Make the necessary connections between the power circuit and the triggering circuit. Release the triggering pulses to the main thyristor T_m and the auxiliary thyristor T_a. See the waveforms of load voltage, load current, commutating capacitor voltage and commutating capacitor current for a resistive load, an *R-L* load and a dc separated excited motor load. Compare these waveforms with the given waveforms in Fig. 4.30.

8.2 THE VOLTAGE COMMUTATED STEP-DOWN THYRISTORISED CHOPPER

In the voltage commutated thyristorised chopper, the main thyristor T_m is commutated (turned-off) by applying a reverse voltage across it. Fig. 4.35 shows the chopper circuit. Its modes of operation and waveforms are shown in the Figs. 4.36 and 4.37 respectively. Before releasing the firing pulses to the power circuit, make the push button (switch) *PS* ON, so that the commutating capacitor *C* gets charged upto voltage +*E* from the source E_s through resistor *R*, as shown in Fig. 4.35. The main thyristor T_m is turned-on by the firing pulses G_m. The commutating capacitor *C* is charged to –*E* volts through T_m, D_1 and L_1 in Mode I. When capacitor current (i_c) reaches the zero value, diode D_1 stops conducting.

When the auxiliary thyristor T_a is turned-on by the firing pulse G_a, capacitor C applies a reverse voltage E to the main thyristor T_m. Thyristor T_m is turned-off and capacitor C is charged to a voltage $+E$ through T_a, D_2 and L_2 in Mode II. Diode D_2 and the auxiliary thyristor T_a stop conducting when the capacitor current reaches the zero value. The load current freewheels through diode D_{FW}. The cycle repeats when the main thyristor T_m is triggered again.

Procedure

Use any triggering circuit out of the circuit of Figs. 4.31 and 4.33. Check whether it is working as expected.

The voltage commutated chopper is shown in the Fig. 4.35. Make the necessary interconnections between the power and triggering circuits. Release the triggering pulses to thyristors T_m and T_a. See the load and capacitor voltage and current waveforms (Fig. 4.35) for a resistive load, an R-L load and a separately excited DC motor load and compare the waveforms with those given in Fig. 4.37.

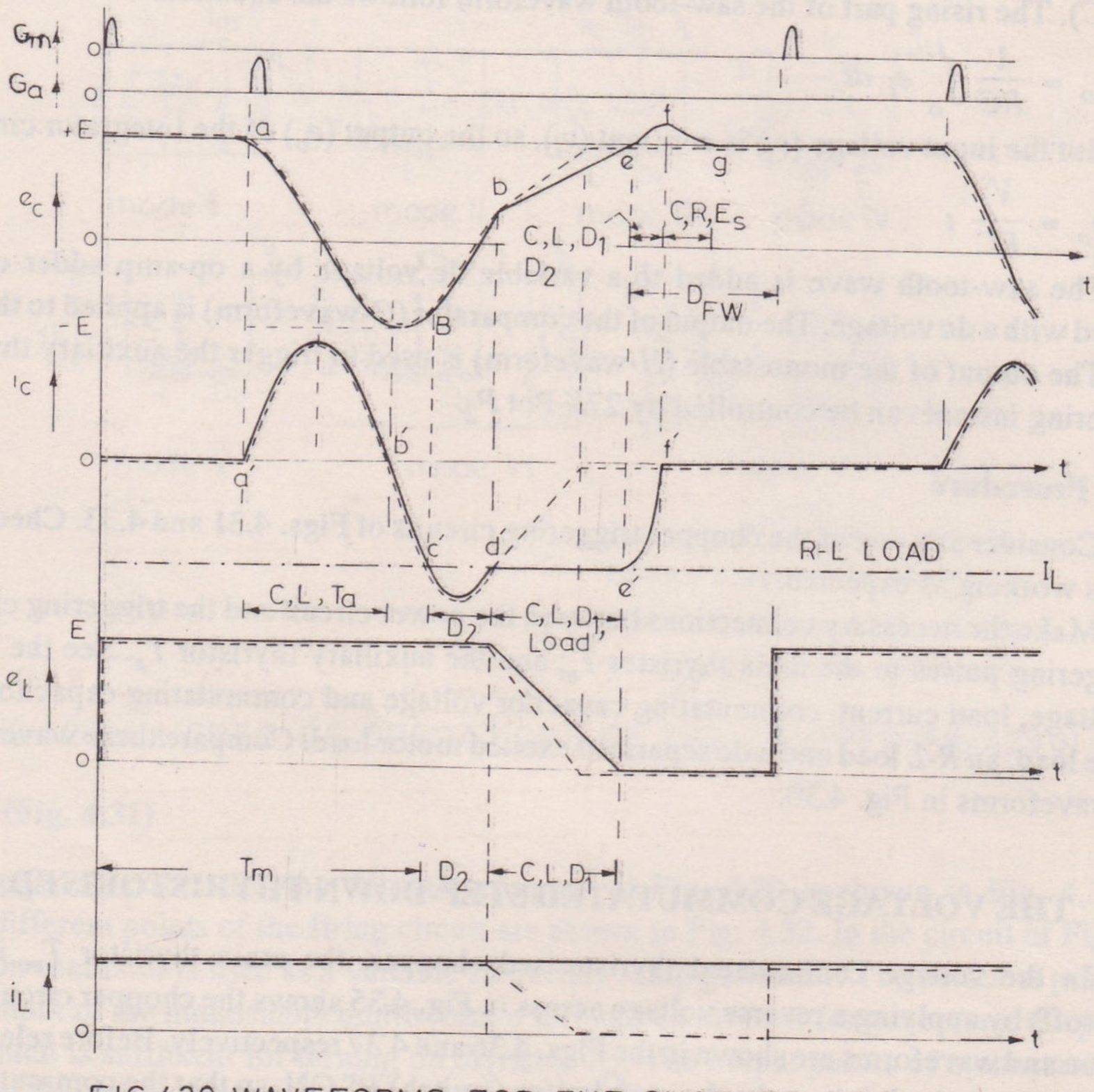


FIG.4.30 WAVEFORMS FOR THE CHOPPER CIRCUIT SHOWN IN FIG.4.29(a)

Where: — When R-L Load is connected

--- When R-Load is connected

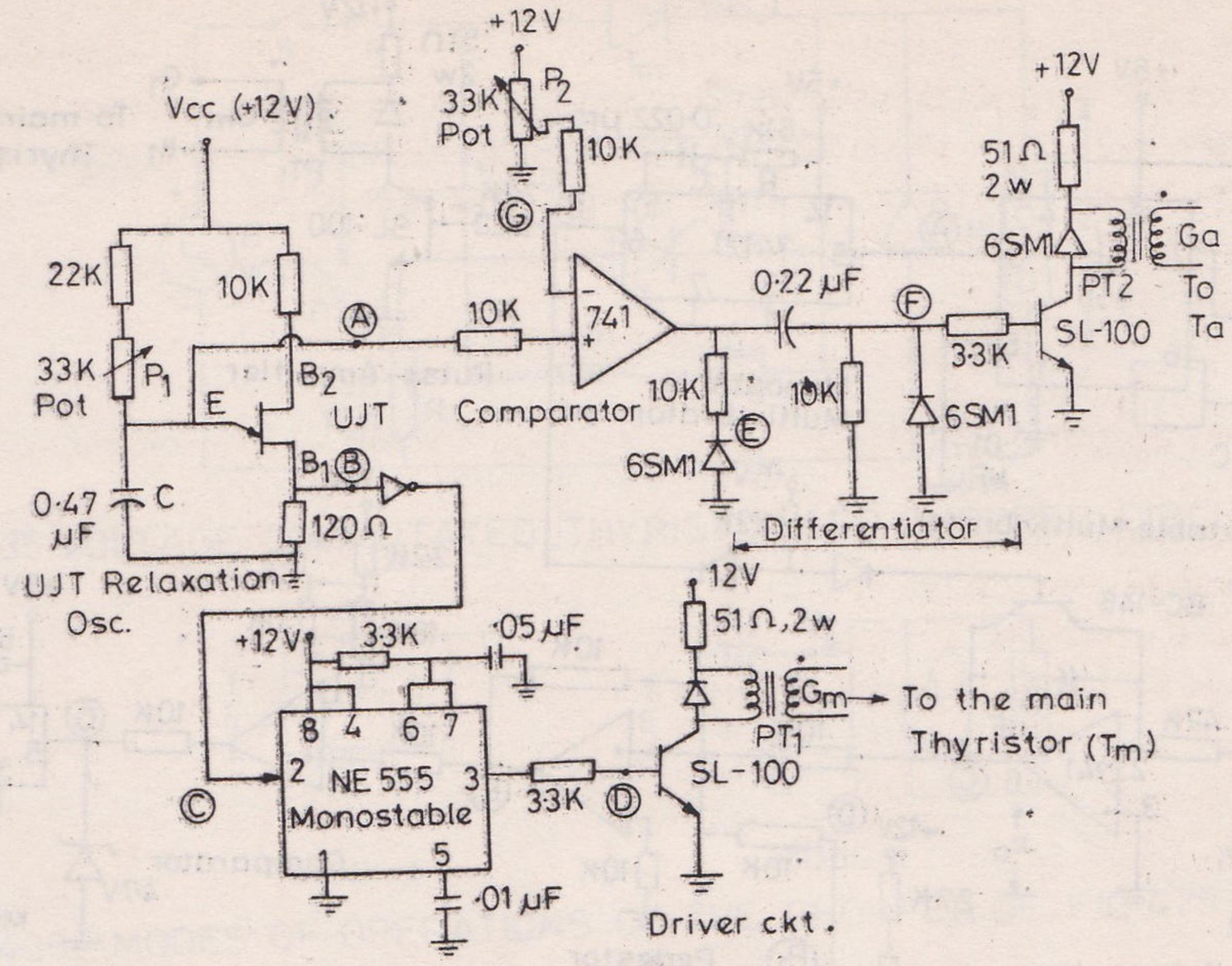


FIG. 4·31: TRIGGERING CIRCUIT FOR THE CHOPPER SHOWN IN FIGS. 4·29 AND 4·35

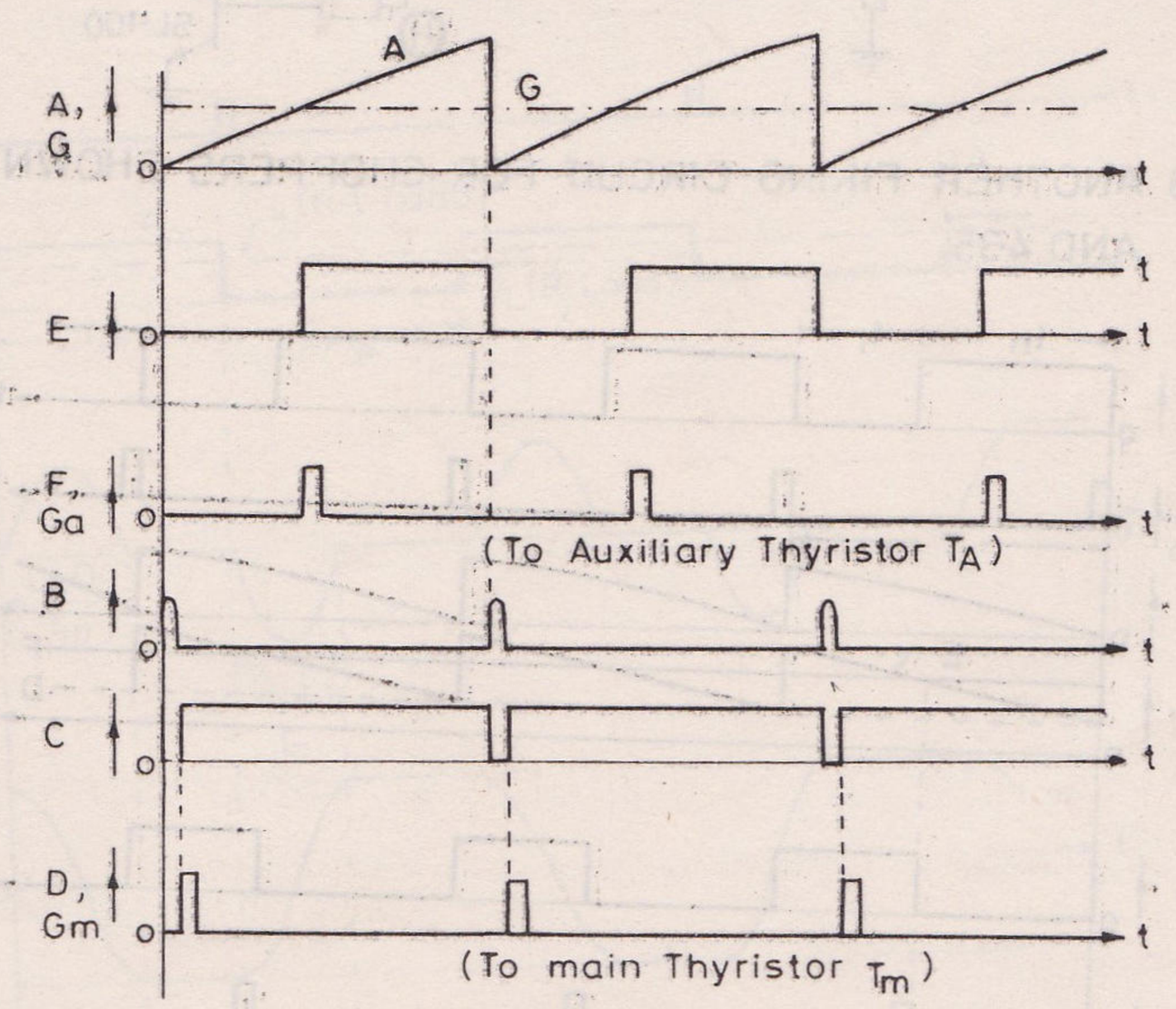


FIG. 4·32 WAVEFORMS OF THE TRIGGERING CIRCUIT OF FIG. 4·31

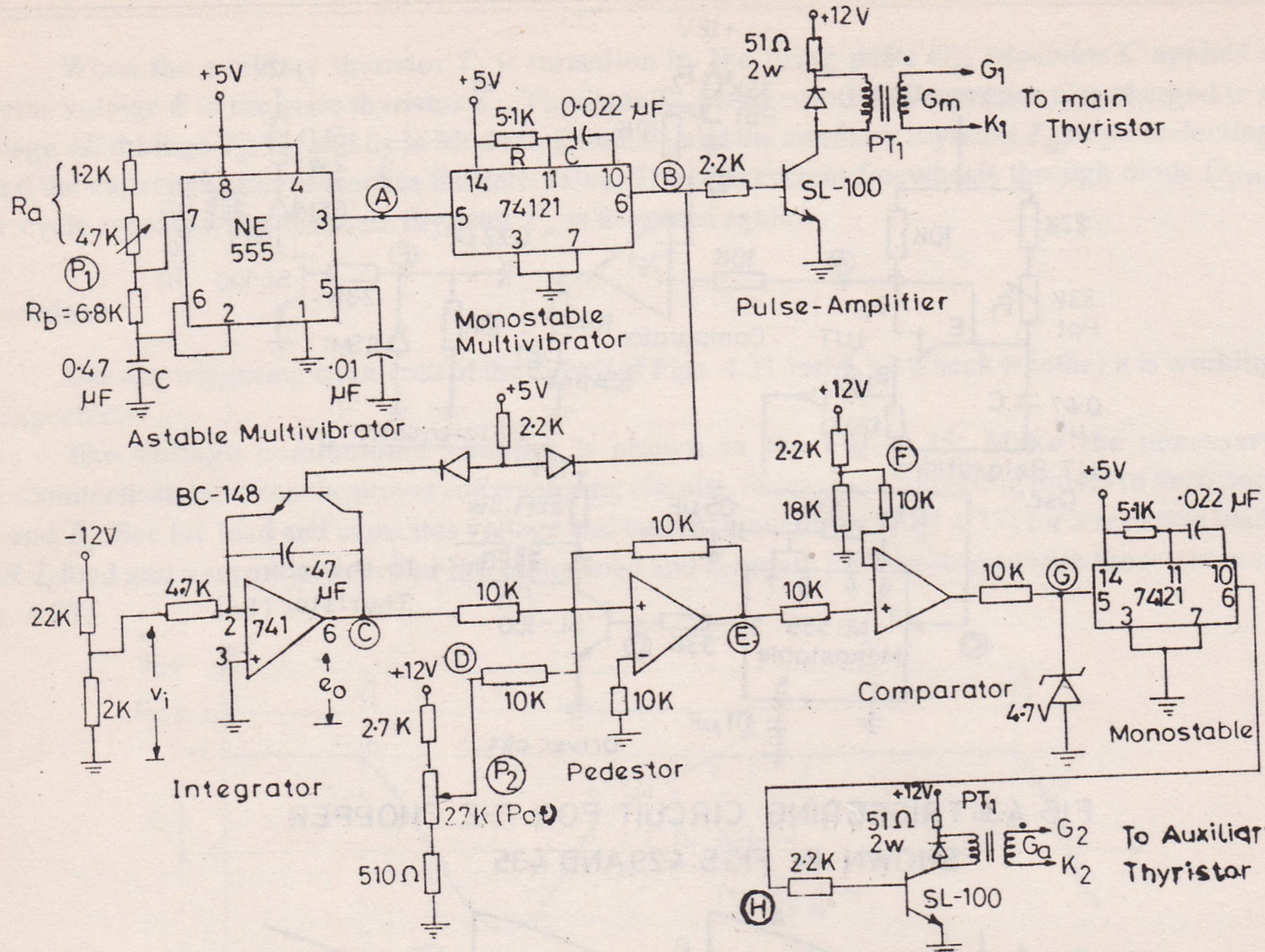


FIG.4·33 ANOTHER FIRING CIRCUIT FOR CHOPPERS SHOWN IN FIG.4·29(a AND 4·35.

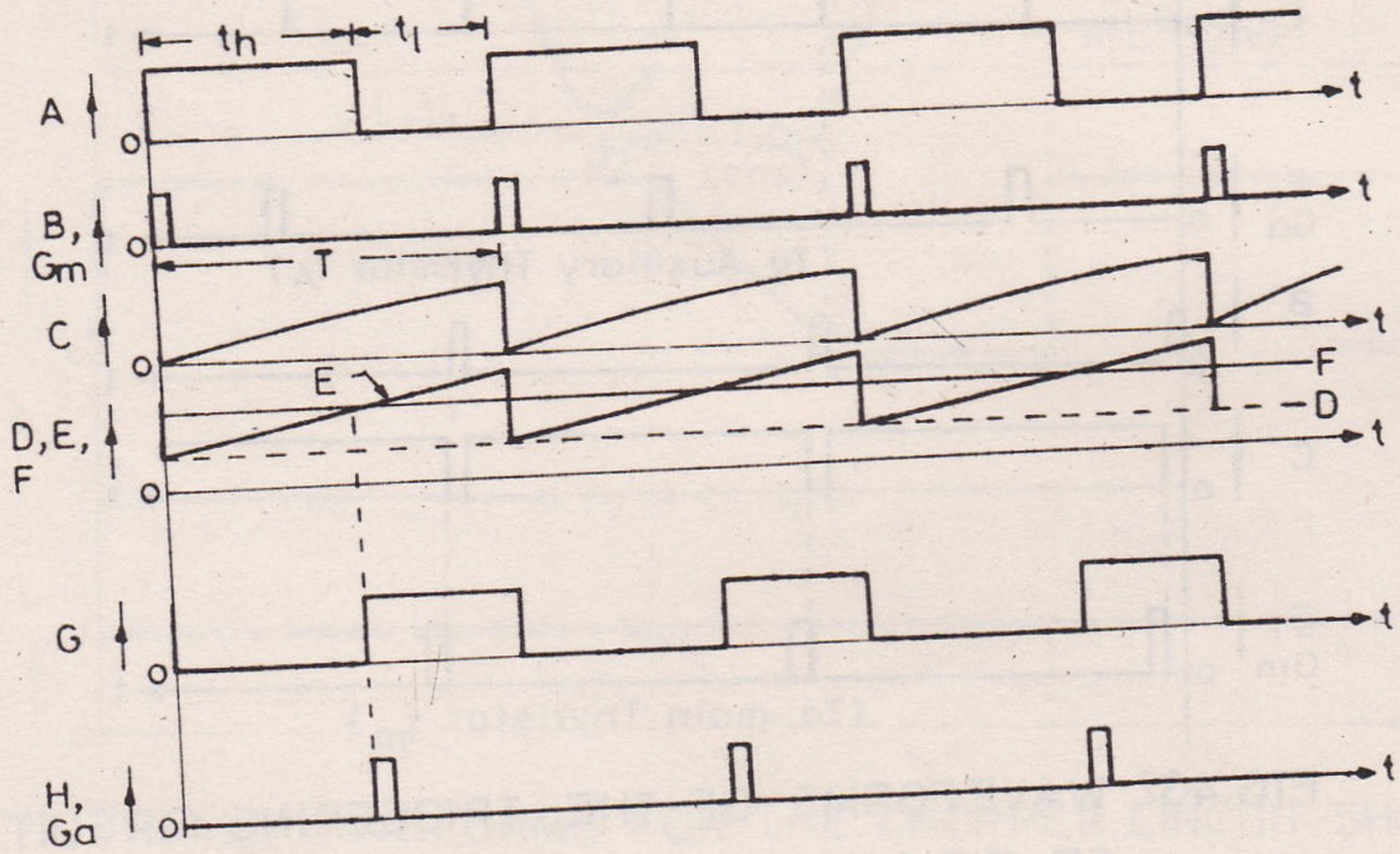


FIG.4·34 WAVEFORMS OF THE FIRING CIRCUIT SHOWN IN THE FIG.4·33

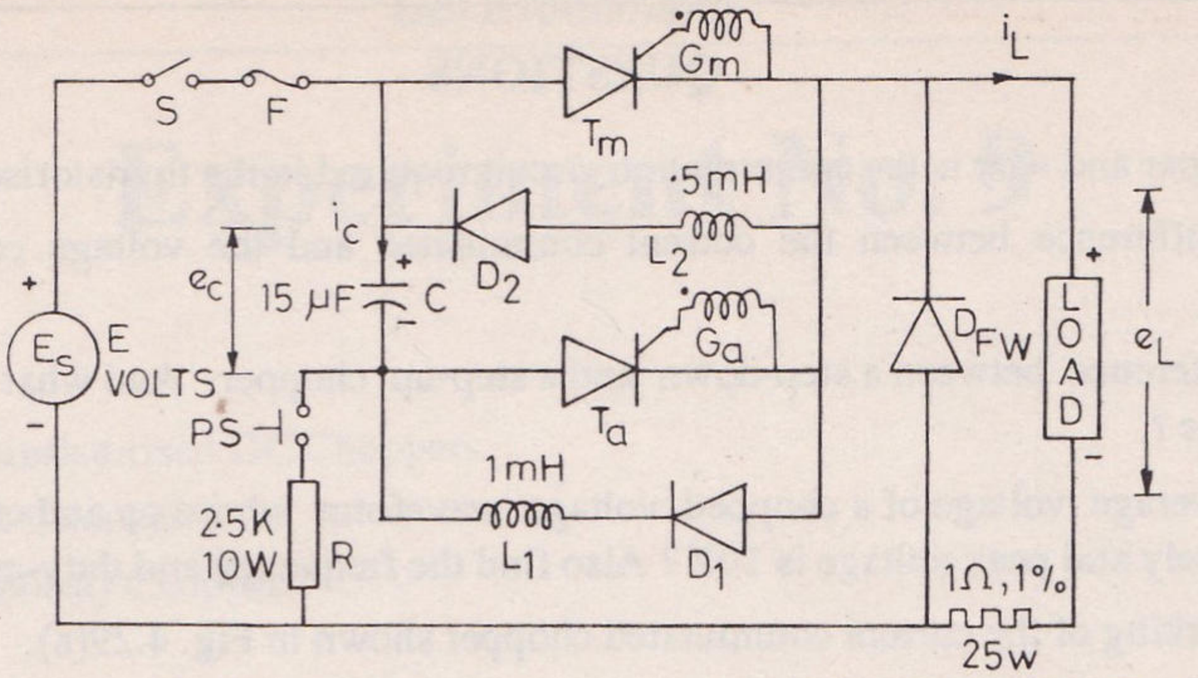
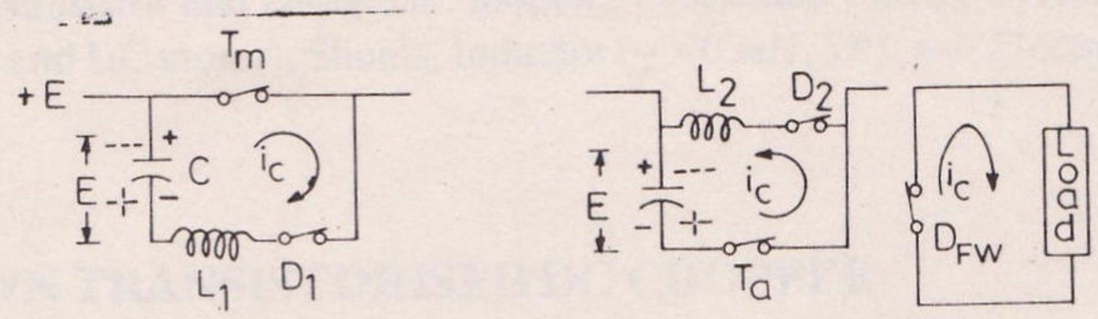
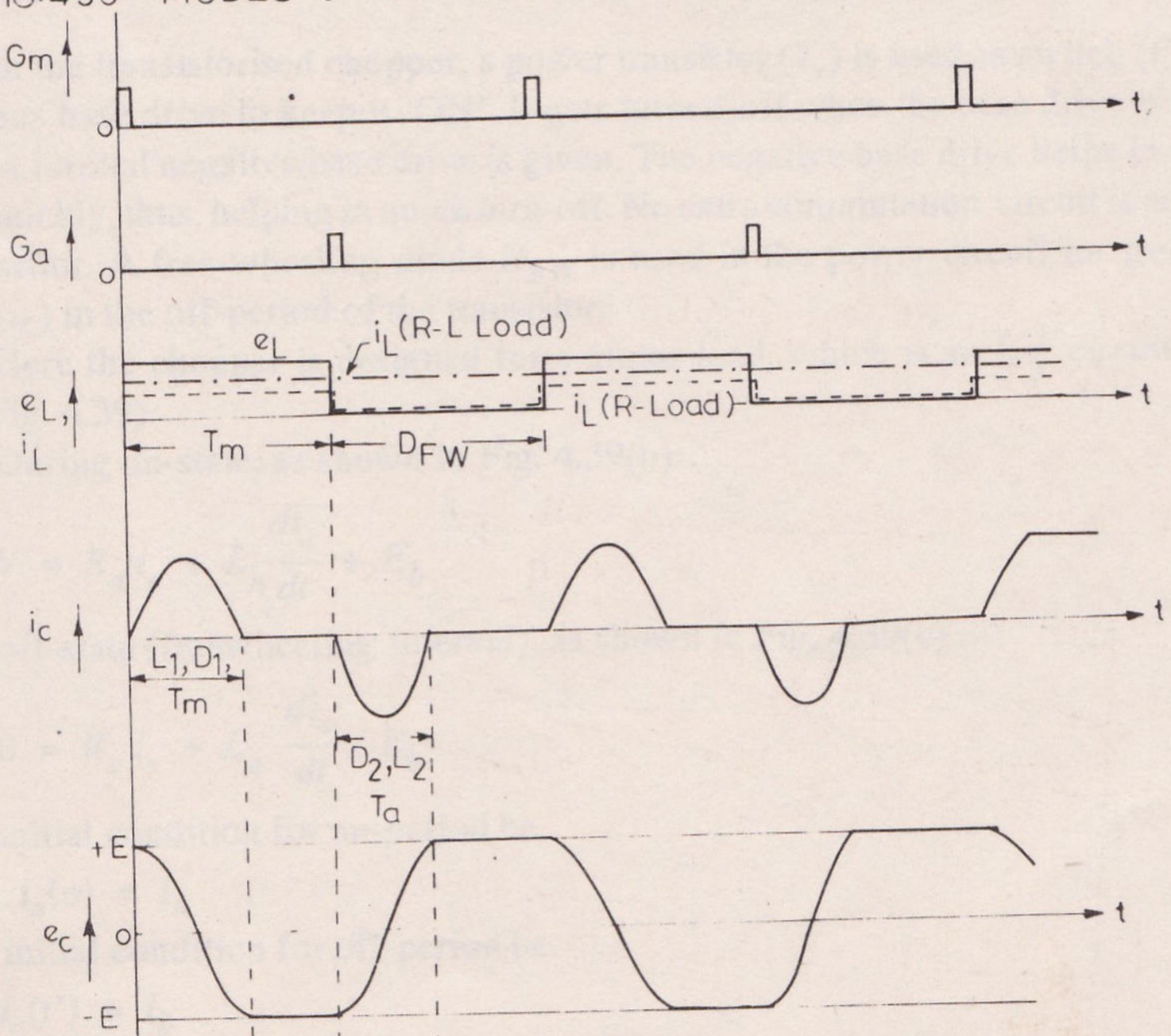


FIG.4·35: VOLTAGE COMMUTATED THYRISTORISED CHOPPER CIRCUIT



MODE I MODE II

FIG.4·36 :MODES OF OPERATIONS OF THE CHOPPER OF FIG.4·35



Where

$t_1 = \pi\sqrt{L_1 C}$

$t_2 = \pi\sqrt{L_2 C}$

FIG.4·37 WAVEFORMS OF THE CHOPPER SHOWN IN FIG.4·35

QUESTIONS

8.1 What is a chopper and why is the commutation circuit required in the thyristorised chopper circuit ?

8.2 What is the difference between the current commutated and the voltage commutated thyristorised choppers ?

8.3 What is the difference between a step-down and a step-up chopper. And what is the other name of the step-up chopper ?

8.4 What is the average voltage of a chopped voltage waveform whose on and off periods are 20 μs and 10 μs respectively and peak voltage is 10*V* ? Also find the frequency and duty-cycle of the chopper.

8.5 Explain the working of the current commutated chopper shown in Fig. 4.29(a).

Experiment No. 9

Objective : To study Transistorised DC Choppers.

9.1 : Step Down Chopper

9.2 : Step-Up (Boost) Chopper

Apparatus Required

Oscilloscope, Transistor and Diode lab. module, Fabricated control circuit for transistorised chopper, Loads (R-load, R-L load and DC motor), Shunts, Inductor ($\simeq$ 40 mH, 5A). and Electrolytic Capacitor ($\simeq$ 500 μF, 450V).

9.1 STEP-DOWN TRANSISTORISED DC CHOPPER

Description

In the transistorised chopper, a power transistor (T_r) is used as switch (Fig. 4.38). It requires continuous base drive to keep it 'ON'. It gets turned-off when the base drive is removed. For quick turn-off a limited negative base drive is given. The negative base drive helps in removing the stored charge quickly, thus, helping in quick turn-off. No extra commutation circuit is needed for turning-off the transistor. A free-wheeling diode D_{FW} is used in the power circuit for free-wheeling the load current (i_L) in the off-period of the transistor.

Here the chopper is designed for a motor load, which is an R-L circuit with a back emf in series (Fig. 4.39).

During on-state, as shown in Fig. 4.39(b):

$$V = R_a i_a + L_a \frac{di_a}{dt} + E_b \tag{4.7}$$

During off-state (freewheeling interval), as shown in Fig. 4.39(c) :

$$0 = R_a i_a + L_a \frac{di_a}{dt} + E_b \tag{4.8}$$

Let the initial condition for on-period be

$$i_a(o) = I_a$$

and the initial condition for off-period be

$$i_a(t') = I_b$$

The instantaneous current $i_a(t)$ during on-period from eqn. (4.7) will be

$$i_a(t) = \frac{V - E_b}{R_a}(1 - e^{-t/\tau}) + I_a e^{-t/\tau} \tag{4.9}$$

where τ = La/Ra (the load circuit time constant).

Solving eqn. (4.8), for the off-period gives

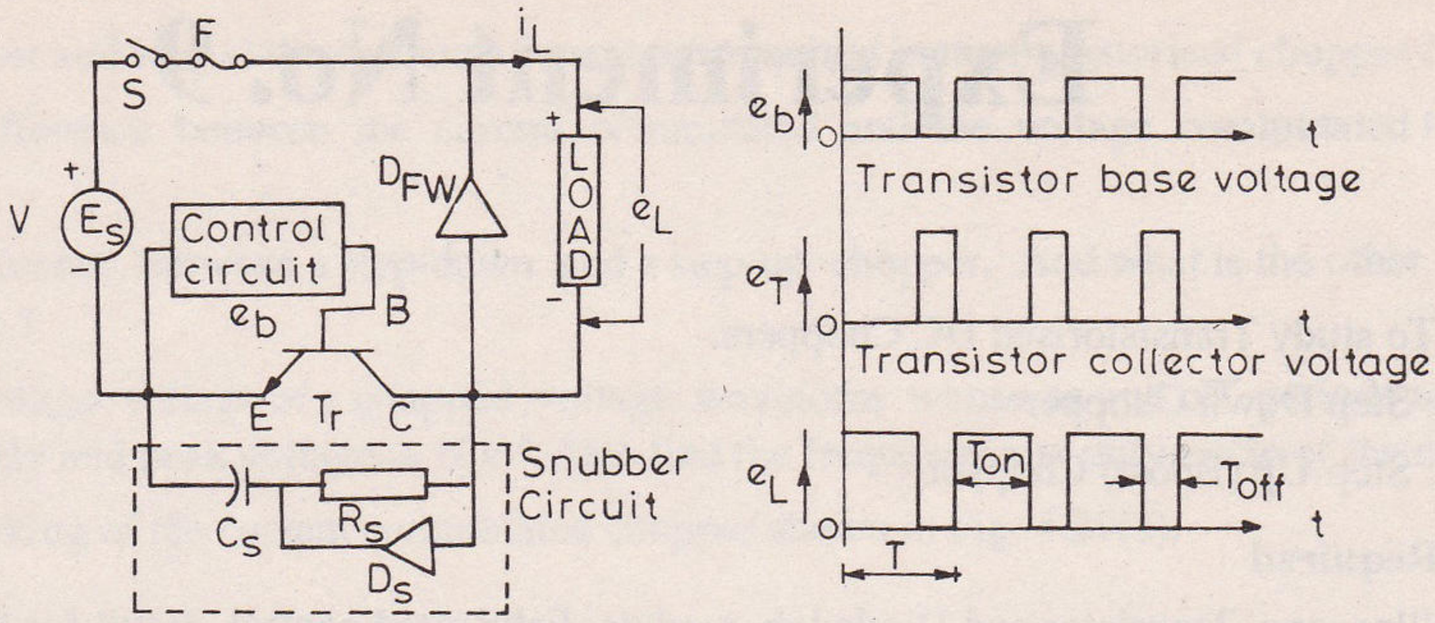
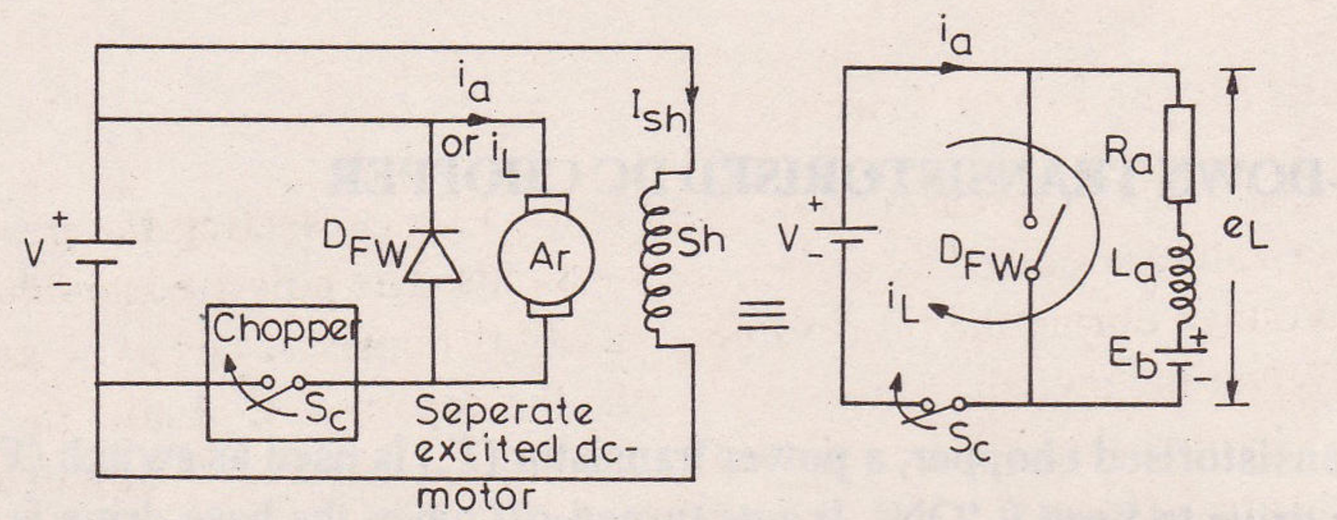


FIG.438:STEP-DOWN TRANSISTORISED DC CHOPPER



(a) CHOPPER WITH DC MOTOR LOAD

(b) EQUIVALENT CIRCUIT DURING ON-PERIOD

(c) EQUIVALENT CIRCUIT DURING OFF-PERIOD

(d) LOAD CURRENT AND VOLTAGE WAVEFORMS

FIG.439: EQUIVALENT CIRCUITS OF CHOPPER WITH DC MOTOR LOAD

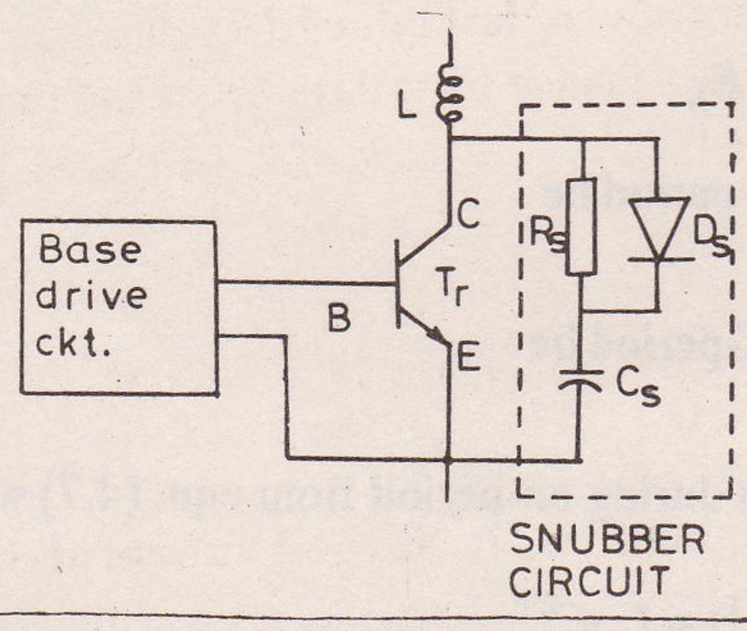


FIG. 4.40 : PROTECTION CIRCUITS FOR THE TRANSISTOR

(1) SNUBBER CKT : To protect from over voltage surges during turn-off period

(2) SMALL INDUCTOR (L) : 3 or 4 turns of Copper wire (≅40 μh) on Torotdal core for protecting device from high dI/dt

$$i_a\ (t) = -\frac{E_b}{R_a}\left[1-e^{-\left(\frac{t-t'}{\tau}\right)}\right] + I_b e^{-\left(\frac{t-t'}{\tau}\right)} \tag{4.10}$$

Average load current (I_L) is given by

$$I_L = \frac{\delta V - E_b}{R_a} \tag{4.11}$$

where δ = duty cycle = $\frac{t_{on}}{T} = \frac{t_{on}}{t_{on} + t_{off}}$

and average load voltage

$$V_L = \delta V = \frac{t_{on}}{T} V \tag{4.12}$$

Protection Circuits for the Power Transistor

The polarized snubber circuit of Fig. 4.40 is used for protecting the power-transistor from damage due to over voltages caused by switching transients. The polarised snubber circuit limits the rate of rise of the voltage during the turn-off periods of the transistor and avoids second breakdown in the transistor. When the switch (transistor) is off, the capacitor C_s limits the rate of rise of the voltage. It is also charged through the diode D_s. In the on-period of the switch, the capacitor C_s discharges through a resistance R_s, which also limits its discharge current.

The value of capacitor C_s is calculated by the following equation :

$$C_s \geq \frac{I_c \cdot (t_r + t_f)}{V} \tag{4.13}$$

where I_c : maximum collector current

t_r and t_f: permitted rise and fall time of the transistor (generally $t_r + t_f = 1$ μsec.).

If $I_c = 10$ Amps.

V = 220 Volts.

Then

$$C_s = \frac{10\ (1 \times 10^{-6})}{220} \simeq 0.05\ \mu F$$

The capacitor C_s should be discharged very fast through R_s during on-period (t_{on}) of the transistor. Then the t_{on}–period should be greater than at least three times the time constant ($R_s C_s$).

Let the minimum t_{on}–period = 10% of T (= 1 *m*sec.)

= 0.1 *m*sec.

and $3 C_s R_s < t_{on}$ (= 0.1 *m*sec).

$$R_s < \frac{0.1 \times 10^{-3}}{3 \times 0.05 \times 10^{-6}} \simeq 670\ \Omega$$

Another condition for selecting R_s is, discharging current of the capacitor $I_{dis} < 0.25\ I_c$

and $I_{dis} = \frac{V}{R_s} = \frac{220}{R_s} < 0.25\ I_c$

or $R_s > \frac{220}{0.25 \times 10} = 88\Omega$

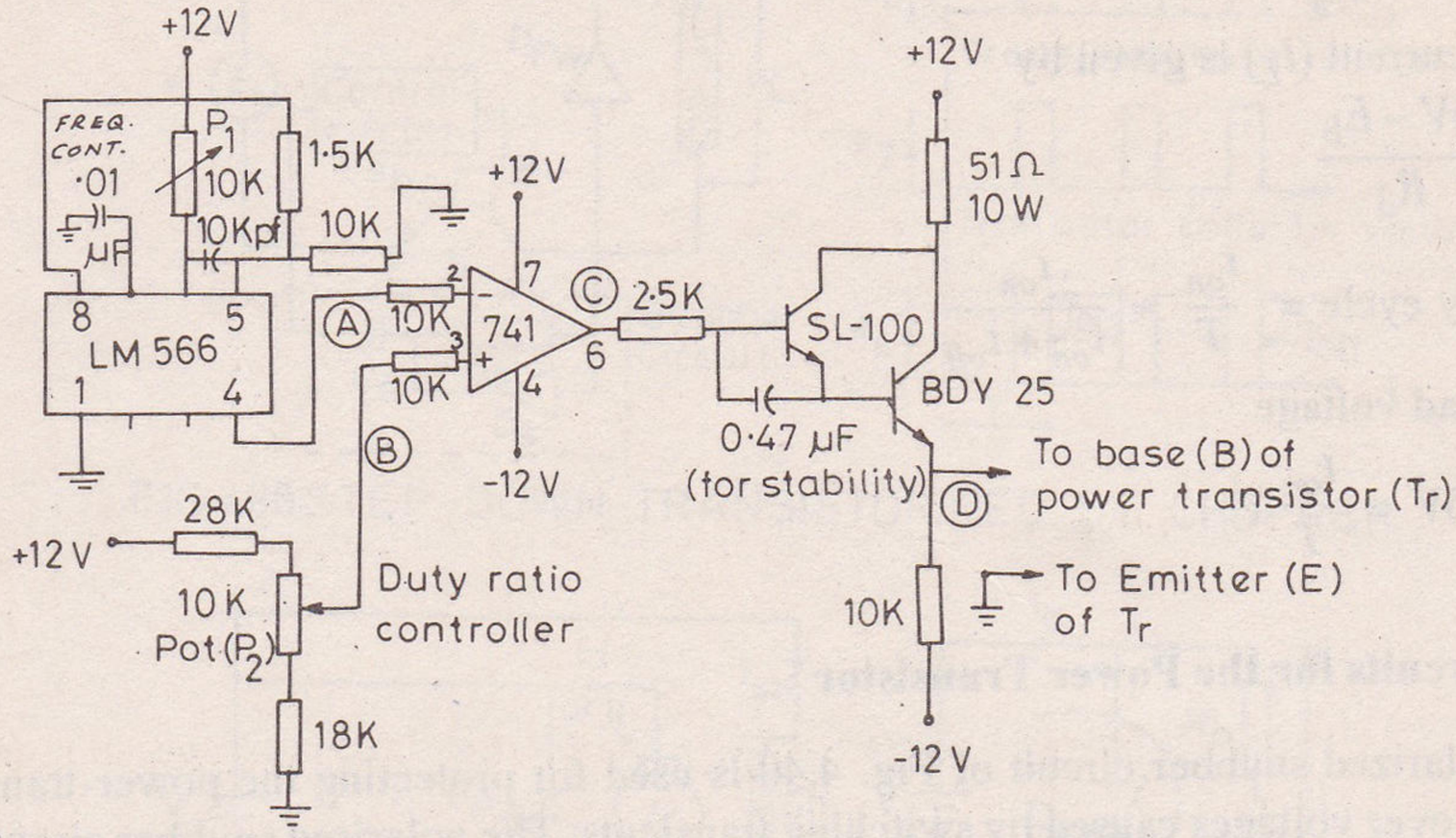


FIG.4·41 : CONTROLLER FOR TRANSISTORISED CHOPPER

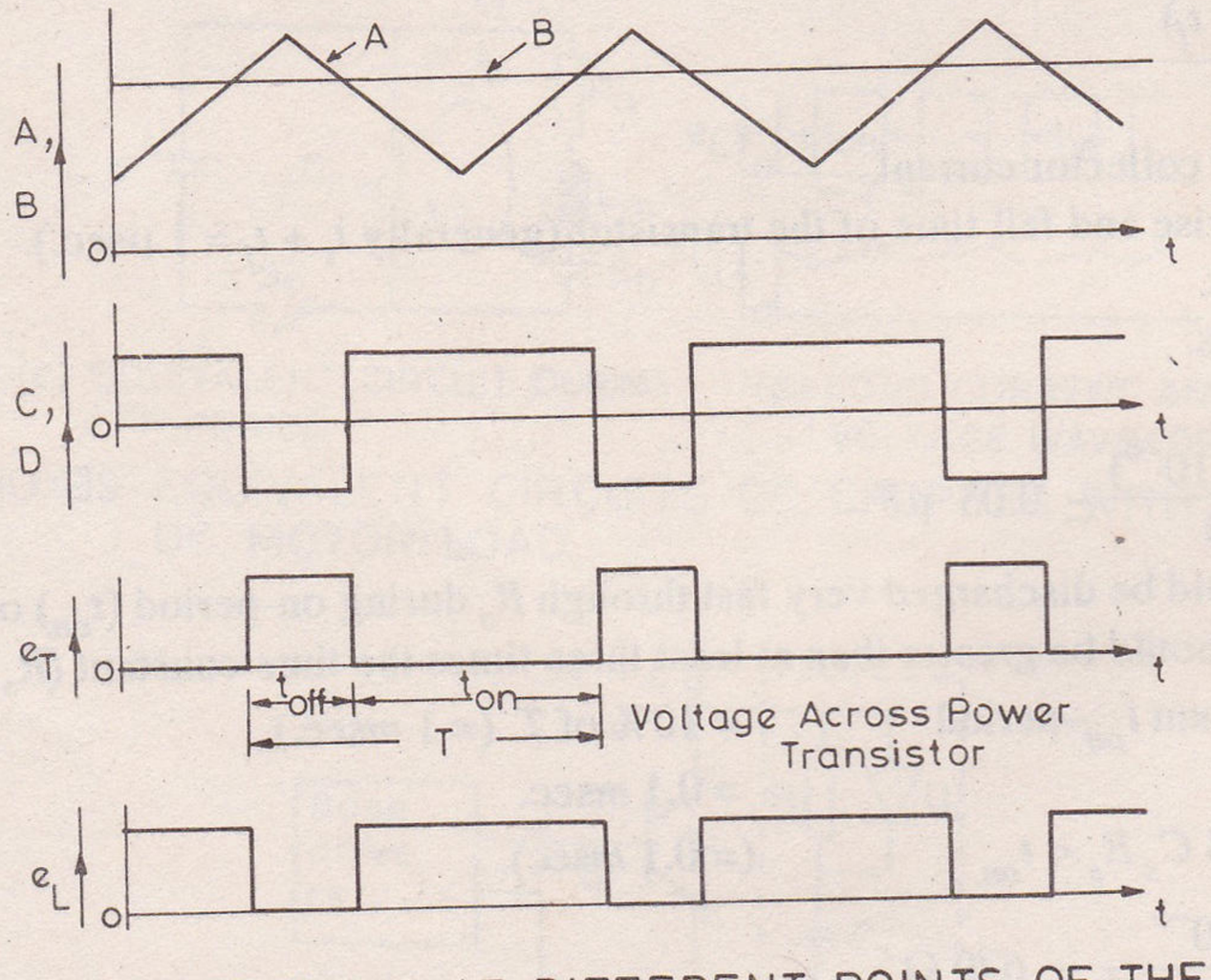


FIG.4·42: WAVEFORMS AT DIFFERENT POINTS OF THE CIRCUITS SHOWN IN FIG.4·38 AND FIG. 4·41

Thus, R_s should be greater than 88Ω and less than 670Ω.
Power dissipated across resistor (R_s) :

$$P_d = \frac{1}{2} C_s V^2 f \tag{4.14}$$

where f : frequency of operation.

Let $f = 1$ *K*Hz, $V = 220$ Volts and $C_s = 0.05$ μF

then $P_d \simeq 1.2$ Watts.

Generally, the values of R_s and C_s for the snubber circuit for the transistor (10*A*, 440*V*), used in the 5*A*, 220*V* chopper circuit are selected as :

$R_s \simeq 200\Omega$, 2 *W*

and $C_s \simeq 0.05$ μF, 400 *V*

Availability of the transistor voltage limits the supply voltage for the chopper.

Firing Circuit

The control circuit diagram of the transistorised chopper and the corresponding waveforms are shown in Figs. 4.41 and 4.42 respectively.

IC-LM566 generates a triangular wave whose frequency can be varied by 10*K* pot (P_1). This triangular wave is compared with a dc Voltage by *IC* 741 comparator. The output of the comparator is applied to the Driver-circuit for current amplification because output current of the comparator is not sufficient to turn-on the power transistor. Time period T (or frequency) of the load voltage can be controlled by potentiometer P_1 and the duration of the chopper is controlled by potentiometer P_2, which is connected with a 741 comparator.

Procedure

Connect the control circuit as shown in Fig. 4.41 and check whether the control circuit is working properly or not. If it is working as expected remove dc supply from the control circuit and inter-connect the control circuit and the power circuit as shown in Fig. 4.38. Release 220*V* to the power circuit and ± 12*V* to the control circuit. See the load voltage, load current and source current waveforms for an *R*-load, and *R-L* load and a DC motor load.

Precautions

1. Duty cycle should not be allowed to exceed beyond 80%.
2. The load current should be limited below 5*A*.

9.2 STEP-UP (BOOST) TRANSISTORISED DC CHOPPER

Description

The basic step-up chopper is shown in Fig. 4.43. The energy is stored in the inductor in the on-period of the switch S_c. The current flows in the inductor L through the switch during T_{on} –period, and the voltage e_L across inductor is equal to V. When switch S_c is opened, the stored energy in the inductance discharged into the capacitor C and the load. During t_{off} –period the inductor voltage is

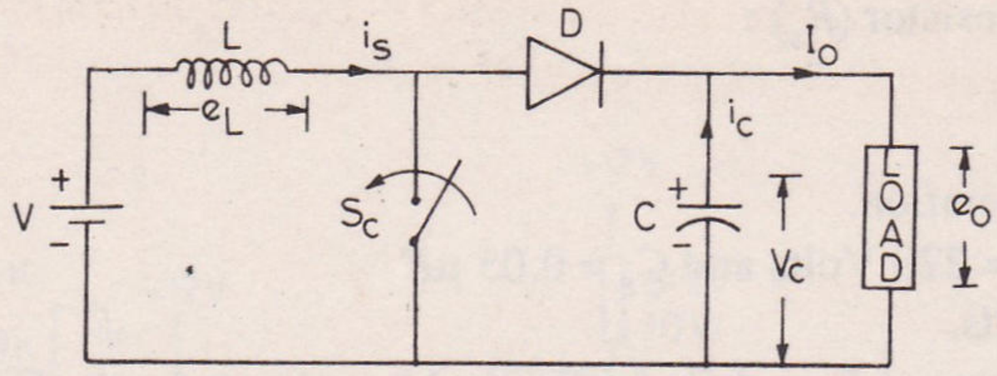


FIG.4.43:BASIC CIRCUIT DIAGRAM OF THE STEP-UP (BOOST) CHOPPER

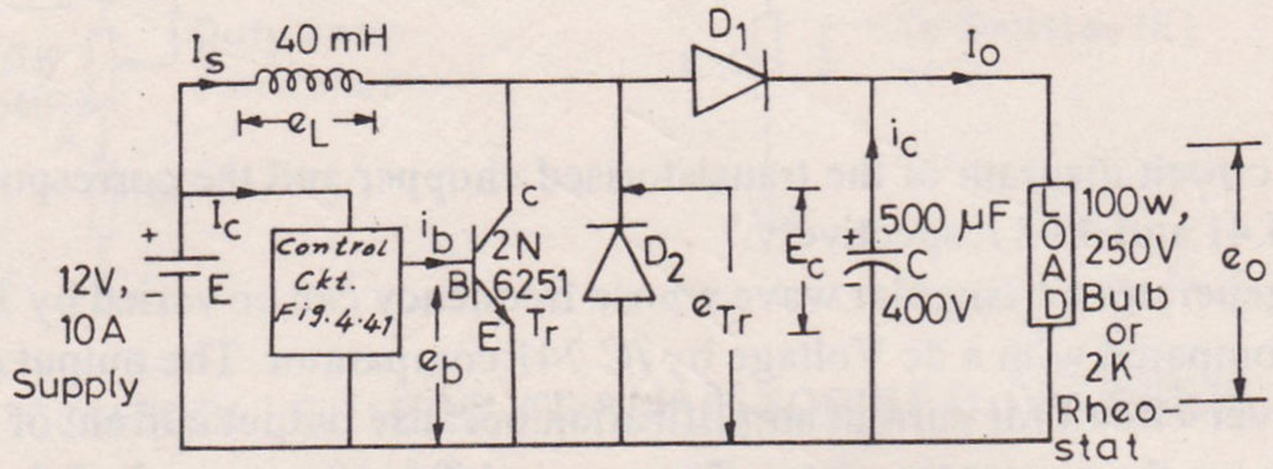
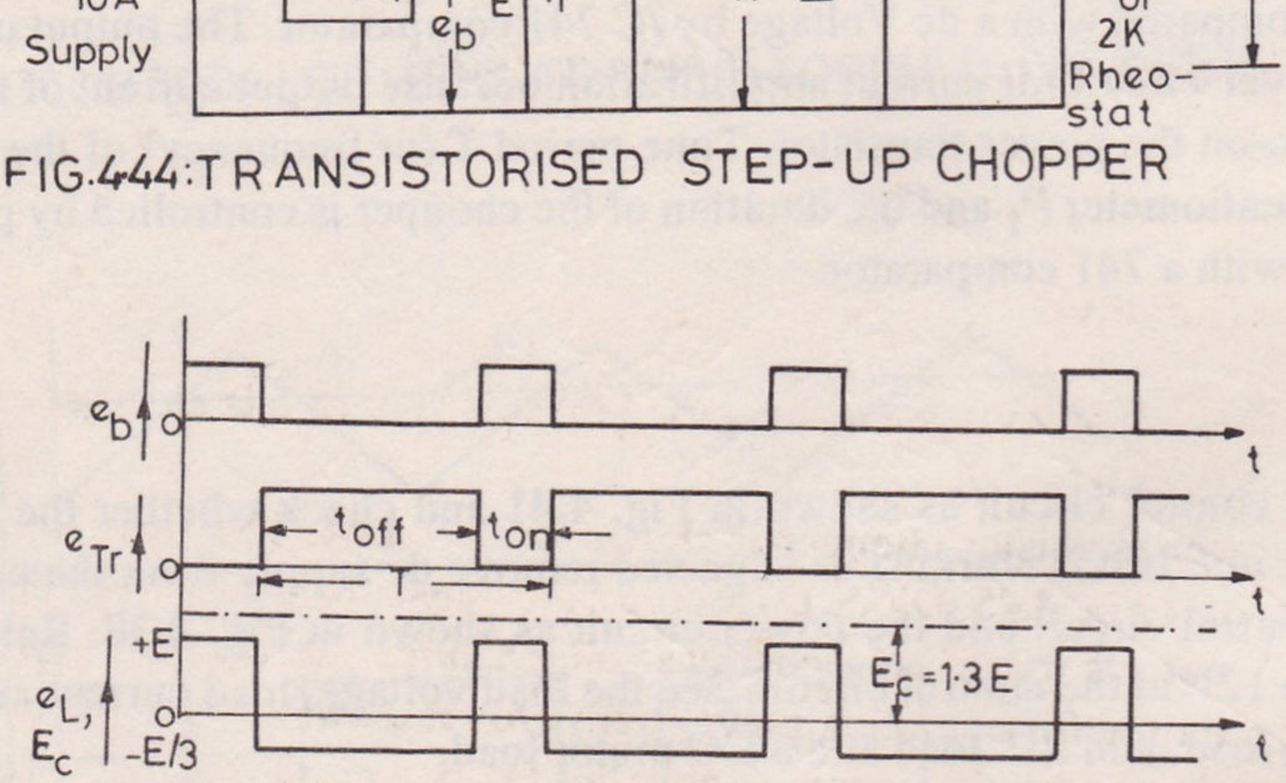
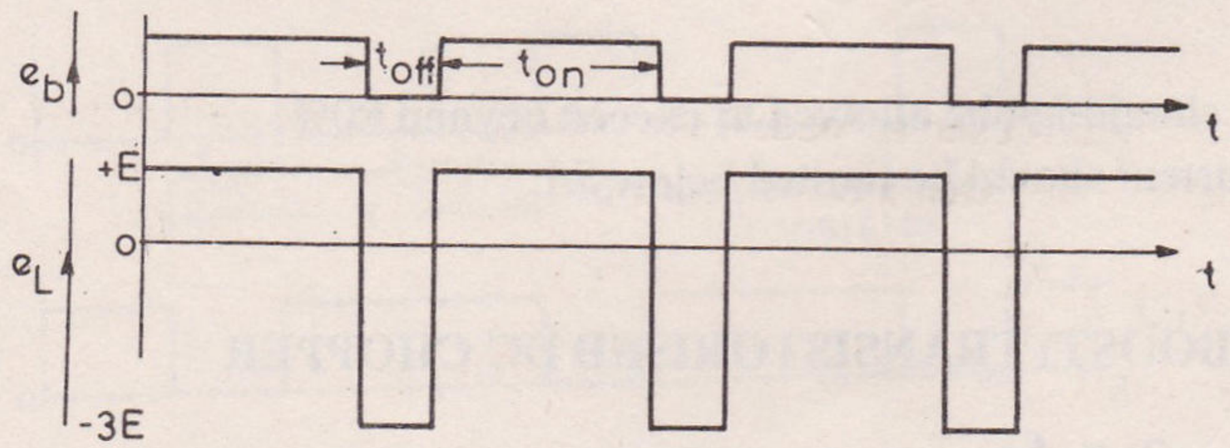


FIG.4.44:TRANSISTORISED STEP-UP CHOPPER



(a) δ (Duty cycle) = 0·25 ($3 \cdot t_{on} = t_{off}$)



(b) δ = 0·75 ($t_{on} = 3 \cdot t_{off}$) i.e. E_c = 4E

FIG.4.45:STEADY STATE WAVEFORMS OF THE CIRCUIT SHOWN IN FIG.4.44

$e_L = V_C - V$. Under steady-state operation, the voltage across the capacitor (V_C) is assumed constant due to a large value of capacitance. And also for steady operation there must be zero average voltage across L during the time period T ($T = t_{on} + t_{off}$). Therefore,

$$\frac{(V_C - V)t_{off} - Vt_{on}}{T} = 0 \qquad (4.15)$$

or $$V_C = \frac{V(t_{on} + t_{off})}{t_{off}} = \frac{V.T.}{t_{off}} \qquad (4.16)$$

And duty cycle, $\delta = \frac{t_{on}}{T}$ (4.17)

or $$\delta = \frac{T - t_{off}}{T} = 1 - \frac{t_{off}}{T}$$

or $$\frac{T}{t_{off}} = \frac{1}{1 - \delta} \qquad (4.18)$$

From eqns. (4.16) and (4.18)

$$V_C = \frac{V}{1 - \delta} \qquad (4.19)$$

If (duty cycle) approaches zero ($t_{on} \simeq 0$) then from eqn. (4.19)

$$V_c = V$$

And when δ approaches unity ($t_{on} \simeq T$)

then $$V_c = \frac{V}{0} = \infty \text{ (infinity).}$$

Thus, theoretically the output voltage can be varied from V to ∞ as δ is changed from 0 to 1. Generally δ is varied from 0 to 0.7.

A step-up power transistor chopper is shown in Fig. 4.44. The waveforms across different components are shown in Fig. 4.45. Diode D_2 protects the transistor against the negative surge voltage and the capacitor C protects it against a positive voltage surge. So no additional protection circuit (snubber circuit) is required for operating power transistor as a switch in the step-up chopper.

The power delivered by the source is equal to the power consumed in the load and control circuit of the transistor (T_r). Neglecting losses in the circuit,

$$VI_s = e_o I_o + VI_c \qquad (4.20)$$

A 100W, 250V bulb is used as load. If the voltage across the bulb is now 100V, then the power consumed by the load can be calculated as follows :

Resistance of lamp $(R_L) = \frac{V^2}{W} = \frac{250^2}{100} = 625$ ohms.

For a load voltage of 100V,

Power consumed $W_s = \frac{100^2}{625} = 16$ Watts

Neglecting chopper losses,

$$I_s = \frac{W_s}{V_s} = \frac{16 \ Watts}{12 \ Volts} \simeq 1.34 \text{ Amps.}$$

Since the same supply gives power (about $\simeq$ 2A) to the base of the transistor, the total current drawn from the power supply is around 3.5 amps.

Note that the chopper is operated at the highest possible frequency in order to minimise the size of the filter.

Procedure

Make the step-up chopper power circuit as shown in Fig. 4.44. Keep $e_o < \beta V_{ceo}$ of the transistor.

The output voltage e_o can be controlled by controlling the duty cycle δ. Use the same control circuit as used in Experiment 9.1. See the waveforms at different points without load, with an *R*-load and an *R-L* load. See the effect of changing t_{on} and t_{off} periods of the power transistor (at a particular frequency). Note the load voltage and current. Change the frequency and repeat the experiment.

Precautions

1. Duty cycle should not exceed beyond 85%.
2. The total current drawn from the power supply must be monitored and should be within the current rating of the power supply.

QUESTIONS

9.1 Why can a transistorised chopper work at higher frequencies than a thyristorised chopper ?

9.2 Draw and explain the snubber-circuit for a power transistor. And also explain the working of the very low value inductor (L) whch is generally connected in series with the power transistor.

9.3 Draw and explain the triggering pulses for a transistorised and thyristorised choppers. Why are negative pulses used in the triggering circuit of the transistorised chopper ?

9.4 Explain the working of the transistorised step-up chopper shown in Fig. 4.44. Write the capacitor voltage for the following turning conditions of the transistor when input voltage of the circuit is 50 volts.

(i) t_{off} and t_{on} periods are equal.
(ii) t_{on}–period is approximate zero.
(iii) t_{on}–period is approximate infinite.

Experiment No. 10

Objective : To study DS Step-Down MOSFET and GTO Choppers.

10.1 : MOSFET Chopper

10.2 : GTO Chopper

Apparatus Required

Power MOSFET and Diode lab. module, Oscilloscope, Fabricated control circuit for MOSFET Chopper, Low voltage power supply for control circuit, GTO Thyristor and Diode lab. module, Firing circuit for GTO chopper and Loads (*R*-load, *R-L* load and dc motor).

10.1 DC STEP-DOWN MOSFET (METAL-OXIDE SEMI-CONDUCTOR FIELD EFFECT TRANSISTOR) CHOPPER

Description

The chopper circuits produce ripple in the output. The ripple can be reduced by operating the chopper at a high frequency. The thyristor is commonly used device in a chopper circuit due to the higher current gain and good power handling capability. But its switching frequency range is low. For low power applications transistors or MOSFETs can be used. The power transistor operates at a higher frequency than a thyristor, however, a large amount of base drive (current) is needed for its operation. On the other hand, MOSFET, which is essentially a voltage controlled device, requires very low gate power and has a higher switcthing frequency compared to a transistor.

The gate current is drawn of the order of few μA to mA. A suitable gate voltage (V_{GS}) is required for a MOSFET to work as a switch. The input capacitance (stray capacitance, C_{iss}, between gate and source) of the device limits the input voltage below the safe limit, because the device may fail to operate due to overcharging of the C_{iss}. The protection such as zener diode should be connected across Gate and Source of the MOSFET for keeping the gate voltage below the safe limit. Also a path should be provided in the gate circuit for discharging of the input capacitor (C_{iss}).

The MOSFET can be driven directly from an operational amplifier. The FET Op-amp (i.e., CAO81E) is used in the control circuit to achieve higher frequency of operation. The gate drive circuit for the MOSFET is shown in Fig. 4.46(a). The waveforms at some important locations in the circuit are shown in Fig. 4.47. And Fig. 4.46(b) shows the oscillogram for the waveforms at some important locations of the MOSFET chopper circuit shown in Fig. 4.46(a). The triangular waveform is obtained at the output of LM566 chip. The 10*K* pot (P_1) sets the frequency of triangular wave. And the frequency of oscillation is given by the following equation.

$$f = \frac{2(V_{cc}^{+} - V_5)}{RC\ V_{cc}^{+}}$$

where f: Frequency of the output (square and triangular) waves

V_{cc}^{+} : Positive supply voltage

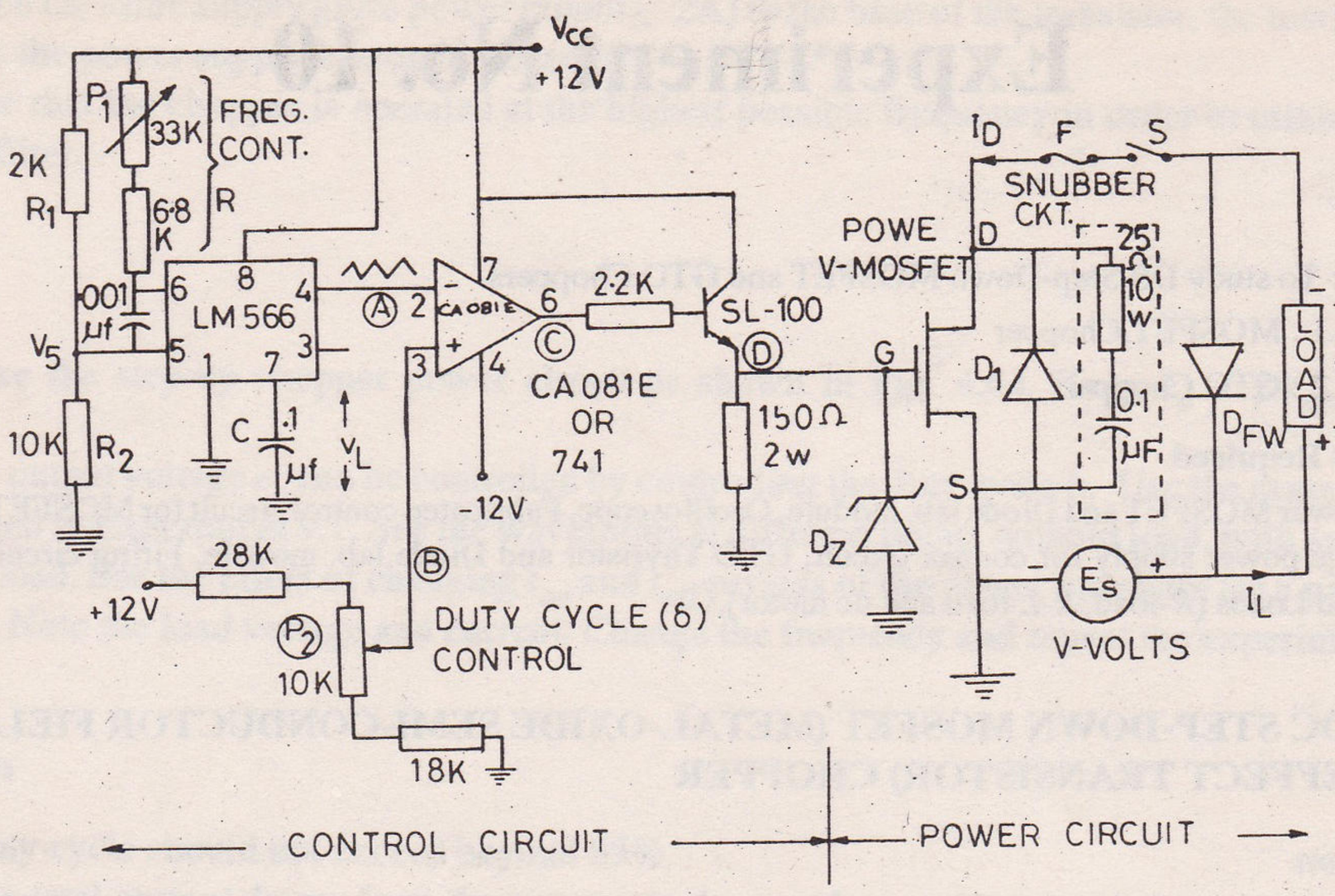


FIG.4-46(a) : CIRCUIT DIAGRAM OF THE STEP DOWN MOSFET CHOPPER

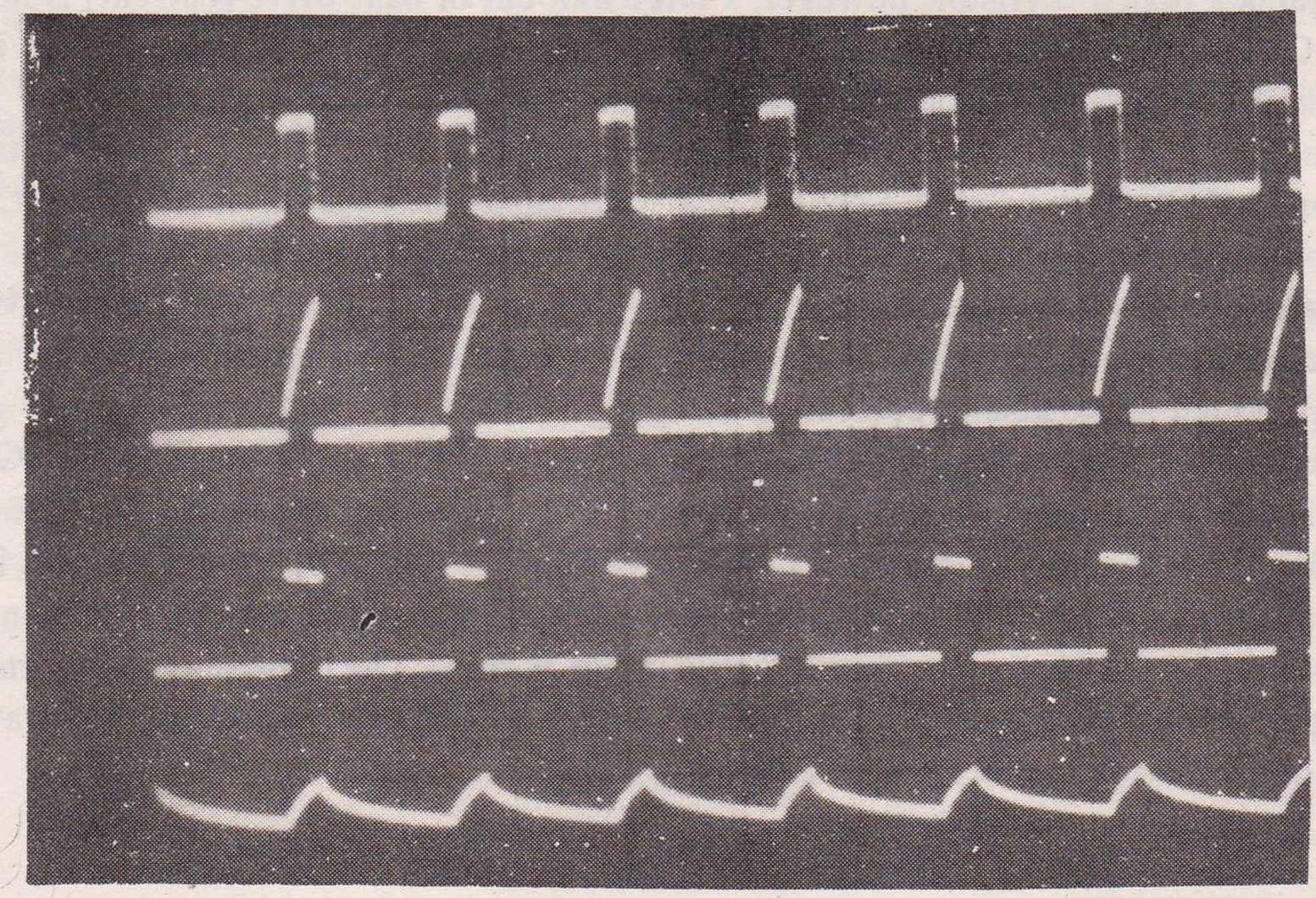


FIG. 4.46(*b*) : OSCILLOGRAM FOR WAVEFORMS OF MOSFET CHOPPER WITH R-L LOAD (R = 40 Ω AND L = 42.5 mH) AND A FREE-WHEELING DIODE
MOSFET CHOPPER'S TRACES : GATE PULSES, INPUT LINE CURRENT, LOAD VOLTAGE AND LOAD CURRENT

V_5 : Applied voltage at Pin No. 5 of LM566.

According to the circuit of Fig. 4.46

$$V_5 = \frac{V_{cc}^{+} \cdot R_2}{R_2 + R_1} = \frac{12 \cdot 10K}{10K + 2K} = 10 \text{ Volts}$$

so $$f = \frac{2(12 - 10)}{RC \cdot 12} = \frac{1}{3RC}$$

If $C = 0.1\ \mu F$ is used in the circuit, then

$$f = \frac{10^6}{0.3R}$$

The value of resistor R for 500 Hz is

$$R_{min} = \frac{10^6}{0.3 \times 500} \simeq 6.67\,K$$

and the value of resistor R for 100 Hz is

$$R_{max} = \frac{10^6}{0.3 \times 100} \simeq 33\,K$$

The FET-Op-amp CAO81E or 741, is used as a comparator and its output is fed to the gate of the power V-MOSFET. A 24 volt zener diode (FZ24) is used for limiting the gate to source voltage (V_{GS}) of the MOSFET and a small resistor of 150 ohm, 2W is used in the gate circuit for quick discharge of the input stray capacitance (C_{iss}) of the device.

A snubber is used across the MOSFET to limit the dV/dt value. The values of R and C of the snubber circuit can be obtained from monographs of the device (supplied by the manufacturer). A diode D_1 is connected across the MOSFET to protect against the reverse breakdown. If load is inductive, then a feedback diode (D_{FW}) should be put across the load.

The specification of V-MOSFET IVN600KVNR are :

Peak Drain-source voltage V_{DSmax}	= 330 Volts.
Peak Gate-source voltage V_{DSmax}	= ± 30 Volts.
Drain Current (I_{DS}) continuous	= 2.5 amps
Drain-Source breakdown voltage (BV_{DS}) with zero Gate-Source (V_{GS}) voltage	= 350 Volts
Body leakage current I_{GSS}	= 10 nA
Rise time	≃ 5 ns
Fall time	≃ 5 ns
Drain-Source voltage rate of rise (dV_{DS}/dt) with V_{GS}	=0 is 100V/nsec.
At V_{DS} = 100V & f = 60 MHz :	
Input capacitance C_{iss} = 220 pf	
Output capacitance C_{oss} = 22 pf	

Procedure

Make the V-MOSFET chopper circuit and its control circuit as shown in Fig. 4.46. And check control circuit to ensure that it is working as expected. Apply the control pulses to the gate of the V-MOSFET and examine whether the circuit works as expected. Note down the waveforms across MOSFET and load for R and R-L loads.

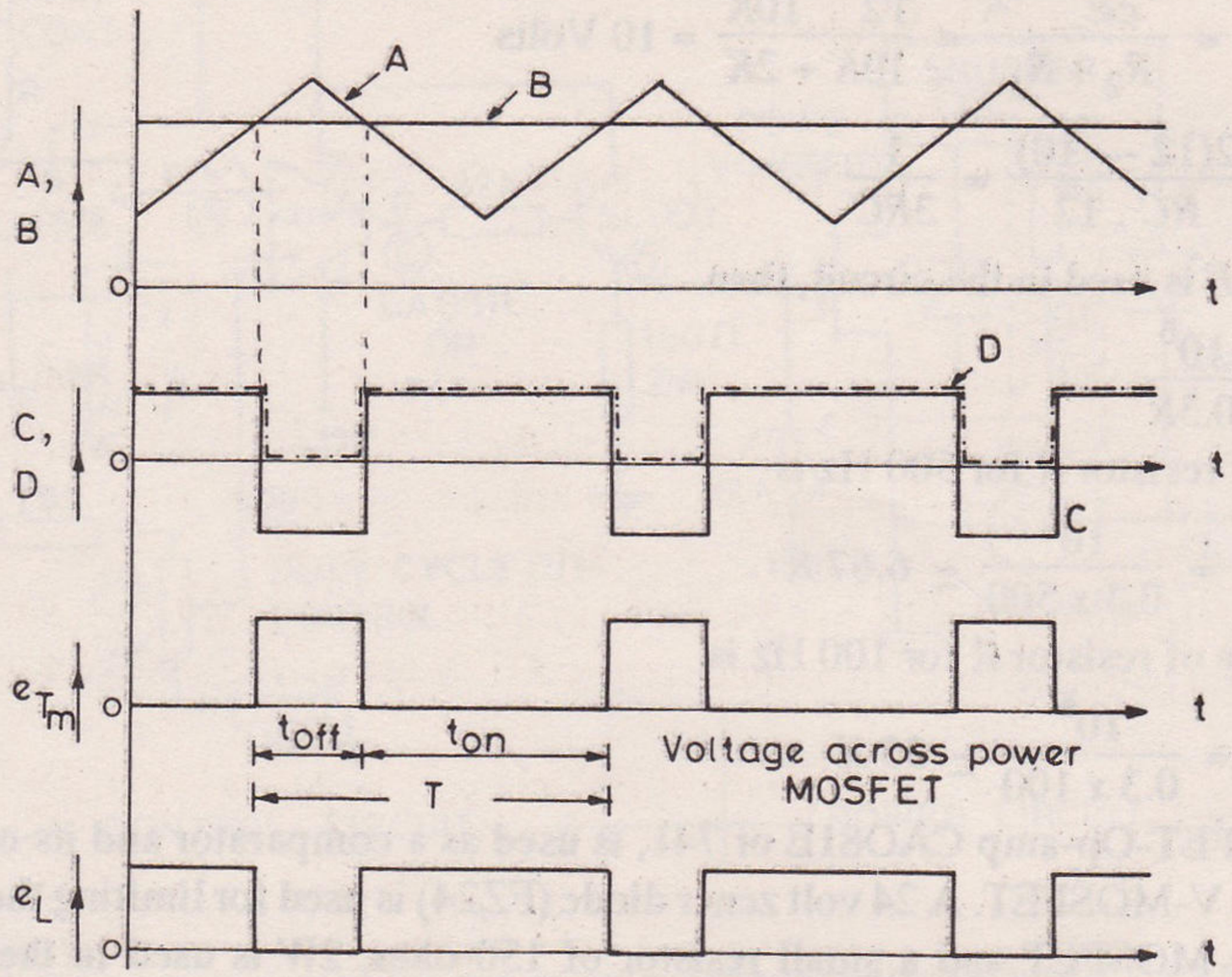


FIG. 4·47 : WAVEFORMS AT DIFFERENT POINTS OF THE CIRCUITS SHOWN IN FIG. 4·46

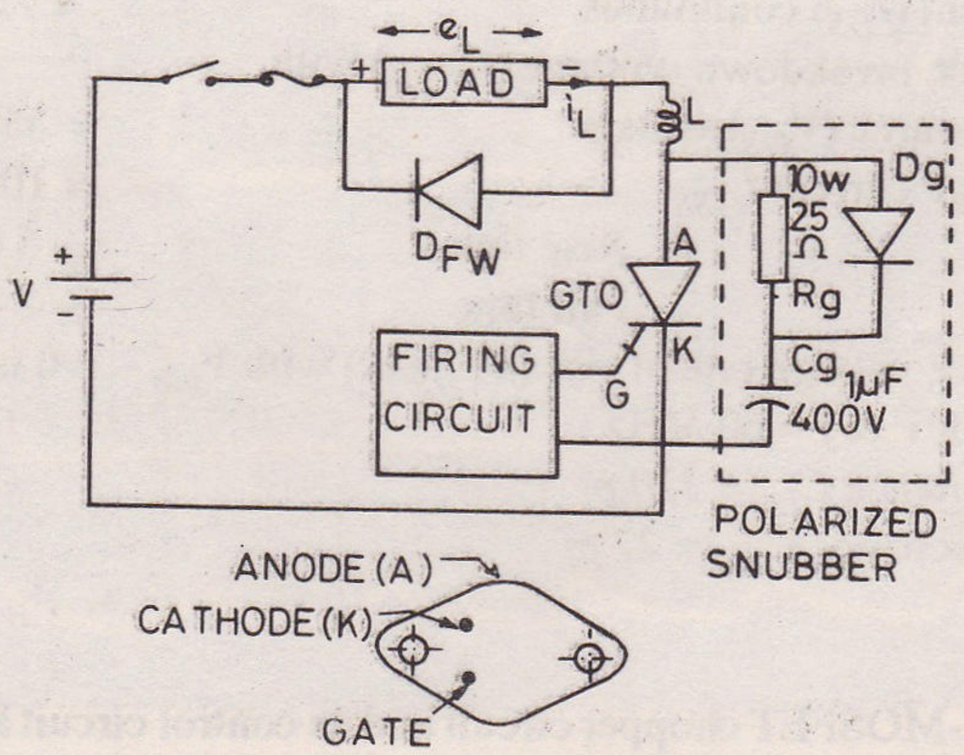


FIG.4·48 : DC STEP-DOWN GTO CHOPPER

Precautions

1. Load current (I_L or I_D) should not be allowed to exceed beyond 2 amps.
2. The duty-cycle (t_{on}/T) should not exceed beyond 80%.

10.2 DC STEP-DOWN GTO (GATE TURN-OFF) THYRISTORISED CHOPPER

Description

GTO is a device which can be turned-on in the same way as a thyristor by applying a small positive gate current pulse. But it can also be turned-off by applying a negative gate current pulse of a few microseconds duration (the negative pulse amplitude is higher than the positive pulse used for turn-on). The GTO can be operated at somewhat higher frequency than the conventional thyristor. The switching frequency limits are however smaller as compared to transistors or MOSFETs. However, power handling capacity is much larger. GTOs are now available upto 4500 Volts and 3000 Amps. rating.

The power circuit of a dc step-down GTO-chopper is shown in Fig. 4.48. A polarized snubber circuit is used across the GTO thyristor to limit dV/dt.

The firing and driver circuit for a GTO chopper is shown in Fig. 4.49. It generates two sets of pulses. One for turn-on and another for turn-off of the GTO. The duty-cycle (δ) of the chopper can be controlled by pot P_2. The frequency of the chopper can be controlled by P_1 connected in the LM566 circuit. Opto-Isolator 6M135 provides isolation between the firing circuit and the driver

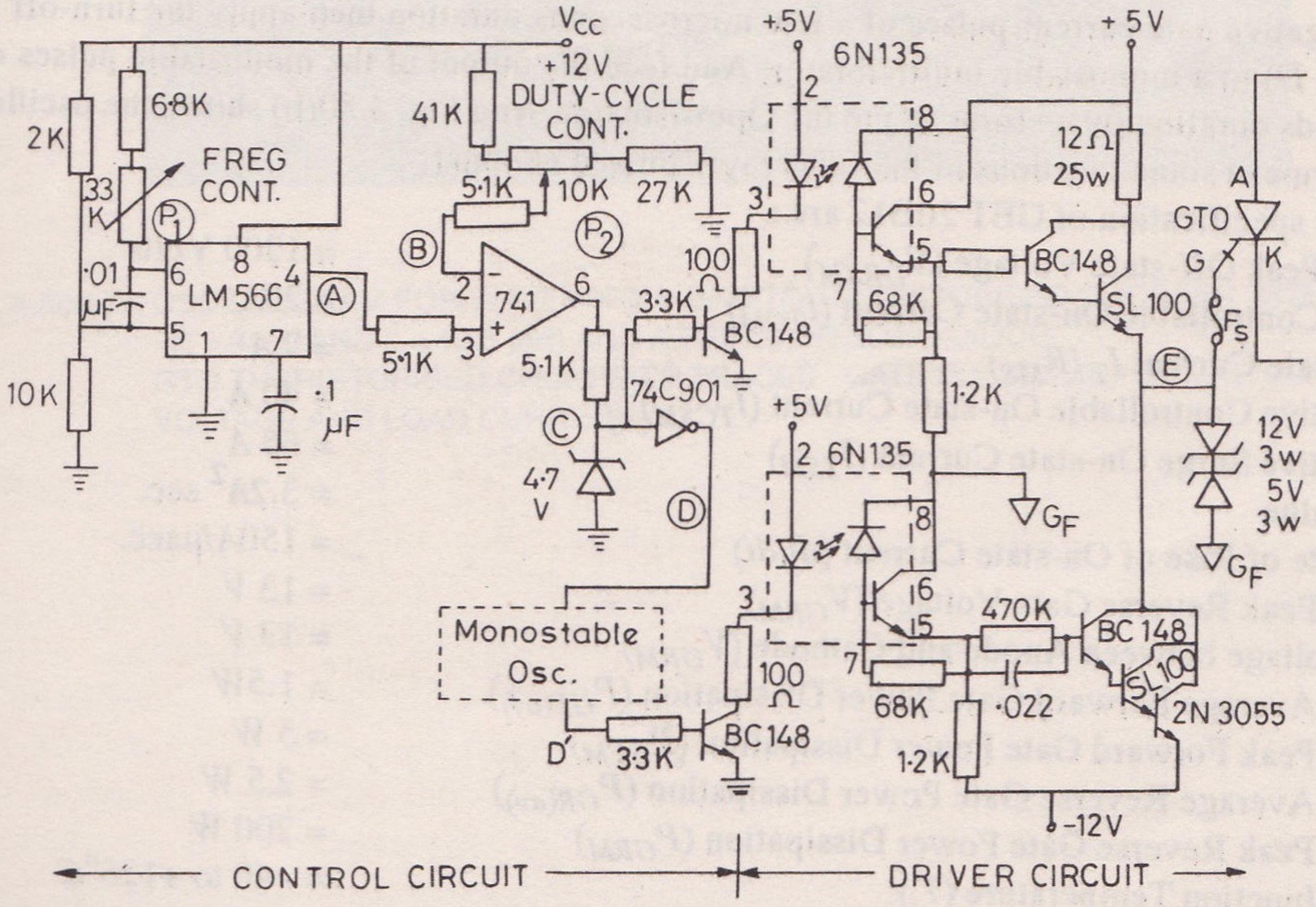


FIG.4·49: FIRING CIRCUIT FOR GTO THYRISTORS

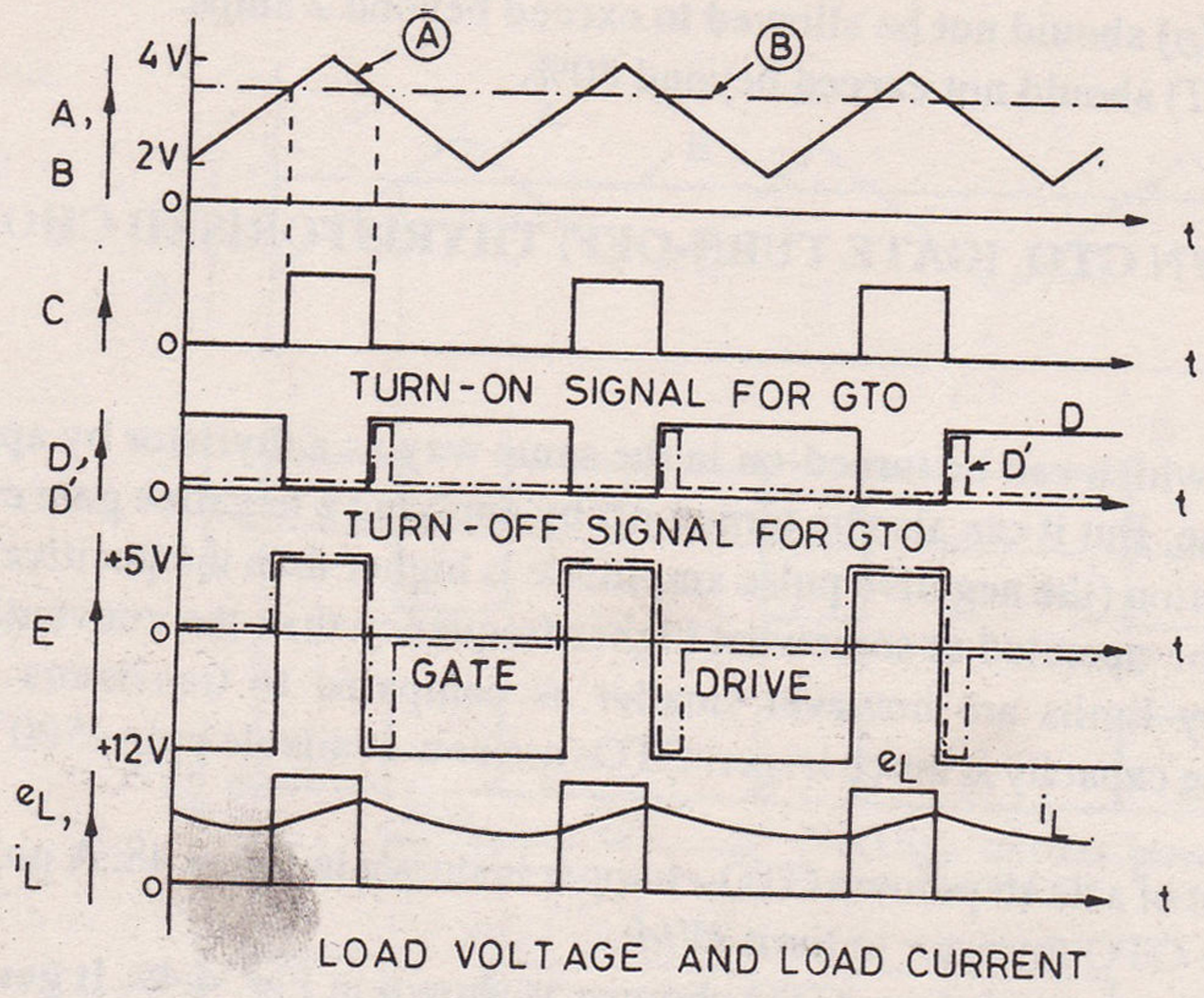


FIG. 4-50 : WAVEFORMS AT VARIOUS LOCATIONS OF FIRING CIRCUIT AND POWER CIRCUIT OF FIGS. 4.48 AND 4.49

circuit. The waveforms at some important location in the circuit are shown in Fig. 4.50. If want to obtain a negative gate current-pulses of a few microseconds duration then apply the turn-off signal (Waveform *D*) to a monostable multivibrator. And feed the output of the monostable pulses of few microseconds duration (waveform *D'*) to the Opto-Isolator. And Fig. 4.50(b) shows the oscillogram for waveforms at some locations of the GTO thyristorised chopper.

The specification of GET 20B12 are :

Repetitive Peak Off-state Voltage (V_{DRXM})	= 1200 Volts
Repetitive Controllable On-state Current (I_{TCM})	= 20*A*
RMS On-state Current I_T (R_{MS})	= 7 *A*
Non-repetitive Controllable On-state Current (I_{TCSM})	= 40 *A*
Non-repetitive Surge On-state Current (I_{TSM})	= 65 *A*
$I^2 t$ limit value	= $3.2A^2$ sec.
Critical Rate of Rise of On-state Current (di/dt)	= 150*A*/μsec.
Repetitive Peak Reverse Gate Voltage (V_{GRM})	= 13 *V*
Reverse Voltage between Anode and Cathode (V_{GRM})	= 13 *V*
Repetitive Average Forward Gate Power Dissipation ($P_{GF(av)}$)	= 1.5*W*
Repetitive Peak Forward Gate Power Dissipation (P_{GFM})	= 5 *W*
Repetitive Average Reverse Gate Power Dissipation ($P_{GR(av)}$)	= 2.5 *W*
Repetitive Peak Reverse Gate Power Dissipation (P_{GRM})	= 200 *W*
Operating Junction Temperature (T_j)	= –40 to +125°*C*
Critical Rate of Rise of Off-state Voltage (dv/dt)	= 1000 *V*/μsec.
Holding Current (I_h)	= 200 *mA*
Latching Current (I_l)	= 700 *mA*

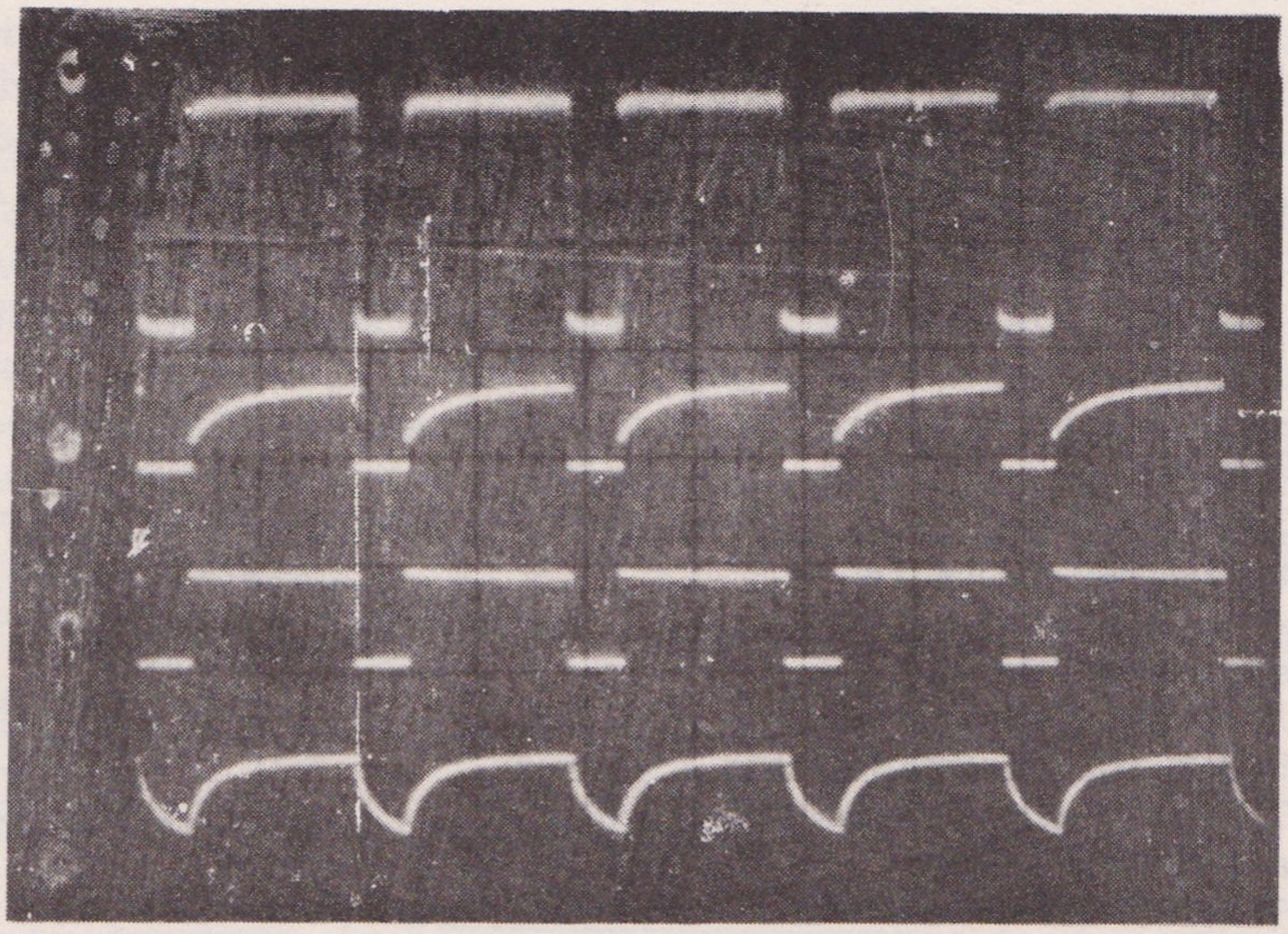


FIG. 4.50(b) : OSCILLOGRAM FOR WAVEFORMS OF GTO THYRISTORISED CHOPPER WITH R-L LOAD (R = 40 Ω AND L = 42.5 mH) AND A FREE-WHEELING DIODE
GTO THYRISTORISED CHOPPER'S TRACES : GATE PULSES, INPUT LINE CURRENT, LOAD VOLTAGE AND LOAD CURRENT

Turn–On-time (t_{dr})	= 3 μsec. (typ.)
Rise-time (t_r)	= 2 μsec. (typ.)
Gate Turn-off-time (t_{qq})	= 4.5.μsec. (typ.)
Gate Storage-time (t_s)	= 4 μsec. (typ.)
Gate Fall-time (t_f)	= 0.5 μsec. (typ.)
Turn-off Gate Charge (Q_{Gq})	= 20 μC (typ.)
Minimum DC Gate Trigger Current (I_{GT})	= 150 mA
Minimum DC Gate Trigger Voltage (V_{GT})	= 1.5 V

Procedure

Make power circuit as shown in Fig. 4.48. Make the firing circuit and driver circuit as shown in Fig. 4.49. See the waveforms at points shown in Fig. 4.50. If it is working properly, connect the firing pulse to the GTO of the chopper-power circuit. See the waveforms of the load voltage, load current and source current at different frequencies and duty cycles with an *R*-load, an *R-L* load and a dc separately excited motor.

QUESTIONS

10.1 Fill in the Blanks :

(i) The MOSFET is a _____ controlled semiconductor device while a transistor, thyristor and GTO thyristors are_____ semiconductor devices.

(ii) A MOSFET has a _____switching frequency compared to the other power semiconductor devices.

(iii) A transistor can be operated at _____switching frequency than the GTO thyristor and conventional thyristor.

(iv) The GTO thyristor can be operated at _____ switching frequency than the conventional thyristor.

(v) The MOSFET requires_____ gate power.

(vi) A GTO thyristor can be turned-off by applying a _____ pulse at the_____.

(vii) A polarized snubber circuit is used across the GTO thyristor to limit _____.

(viii) The transistors and MOSFETs can be used for_____ power applications compared to thyristors.

(ix) The power transistors, MOSFETs, Thyristors and GTOs are available upto the ratings_____, _____, _____ and _____ respectively.

(x) The turn-off time (t_{off}) of the Transistor, MOSFET, Thyristor and GTO are of the order of _____ _____, _____ and_____respectively.

(xi) The gate looses control after a _____ has been triggered into conduction while a _____ can be commutated by applying a negative pulse of the narrow time period at the gate.

10.2 Draw and explain the circuit of the step-up chopper using the MOSFET device. Also write merits and demerits of the MOSFET chopper compared to transistor chopper, thyristor chopper and GTO chopper.

10.3 Draw and explai n the transconductance characteristic and drain characteristic of a MOSFET semiconductor device. What is the threshold voltage of a MOSFET? Write the typical threshold voltage of a Power MOSFET.

10.4 Draw and explain the snubber circuits for a Power MOSFET and a GTO Thyristor.

10.5 Design and explain the triggering circuits for GTO chopper and MOSFET chopper.

Experiment No. 11

Objective : To study the Single-Phase Modified Series Inverter.

Apparatus Required

Oscilloscope, Inverter grade Thyristor lab. module, Two capacitors ($\simeq$ 15 μF, 230 *V* each), Centre taped Inductor ($\simeq$ 2 *mH, 5A)* Rheostat (10 Ω), Fabricated triggering circuit and two pulse-transformers.

Theory

The circuit which converts dc power into ac power, is called inverter. If the thyristor commutation circuit of the inverter is in series with the Load, then the inverter is called "Series-Inverter". Power circuit of a Modified Series Inverter is shown in Fig. 4.51(a). The commutating inductor L is divided into two equal inductances L_1 and L_2, which are tightly coupled. In this circuit, it is possible to turn-on thyristor T_p before the current through thyristor T_n has become zero and vice-versa. Therefore, the Modified Series Inverter can be operated beyond the resonance frequency (f_r) of the circuit. Inverter is operated at the resonance frequency (f_r) if the load current waveform has low frequency and should not have zero current interval. The inverter's resonance frequency depends on the values of L, R and C in the circuit.

The resonance frequency (f_r) of the R–L–C series circuit can be calculated by the formula:

$$f_r = \frac{1}{2\pi}\sqrt{\frac{1}{LC} - \frac{R^2}{4L^2}}$$

According to the circuit 4.51(a); L=1 *mH*, C=15 μ*F* and R=10 Ω.
Therefore,

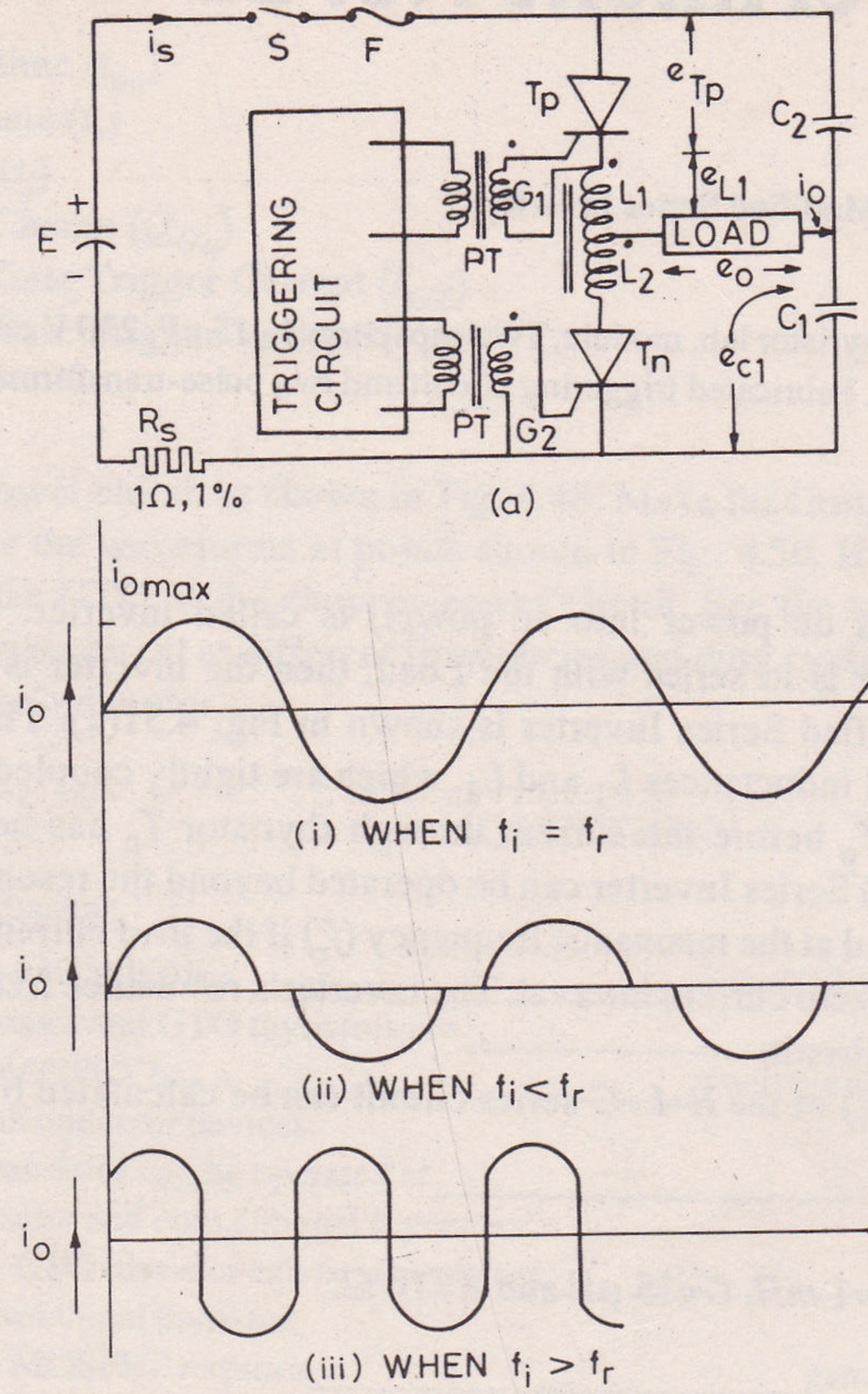
$$f_r = \frac{10^4}{2\pi}\sqrt{\frac{10}{15} - \frac{1}{4}} \simeq 1027 \text{ Hz.}$$

and Time-period (T) at the resonance-frequency = $\frac{1}{f_r} \simeq$ 0.97 *ms*.

The load current waveform for the following three ranges of the inverter frequency (f_i) are shown in Fig. 4.51(b).

(i) $f_i = f_r$, (ii) $f_i < f_r$, (iii) $f_i > f_r$

Operation of the power circuit is explained with the basic three modes shown in Fig. 4.52. The modes are discussed for the inverter-frequency (f_i) higher than the resonance frequency (f_r) and the corresponding waveforms are shown in Fig. 4.53. Let thyristor T_n be already 'ON' (with capacitor polarities as shown by dotted lines in Fig. 4.52) and load current i_o be decreasing in the negative half-cycle as shown in Mode I of this figure and point 'a_1' in the load current (i_o) waveform in Fig. 4.53. Let at point 'a', the triggering pulse is applied to thyristor T_p. Thyristor T_p is turned-ON at this instant, the voltage (e_{c2}) across the capacitor C_2 will be slightly less than $+E_c$ volts (maximum capacitors voltage) but more than supply voltage E and the load current (i_o) and load voltage (e_o) will be close to zero. Therefore, a voltage ($e_{C2}+e_o$) will appear across inductor L_1 through thyristor T_p.



SPECIFICATIONS OF USED COMPONENTS IN OUR LAB

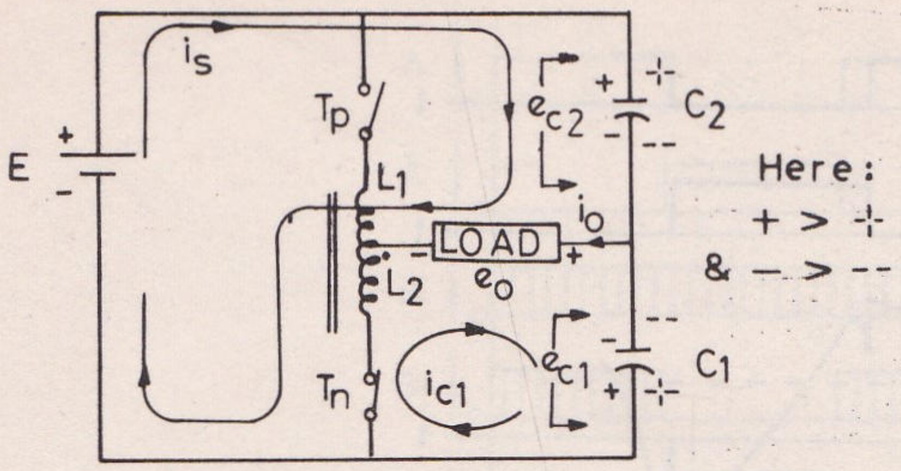
$C_1 = C_2 = 15\ \mu F$
$L_1 = L_2 = 1mH$
LOAD = 10 Ω, 10w
E = 24V

T_p & T_n : Inverter grade Thyristors
PT : Pulse Transformer

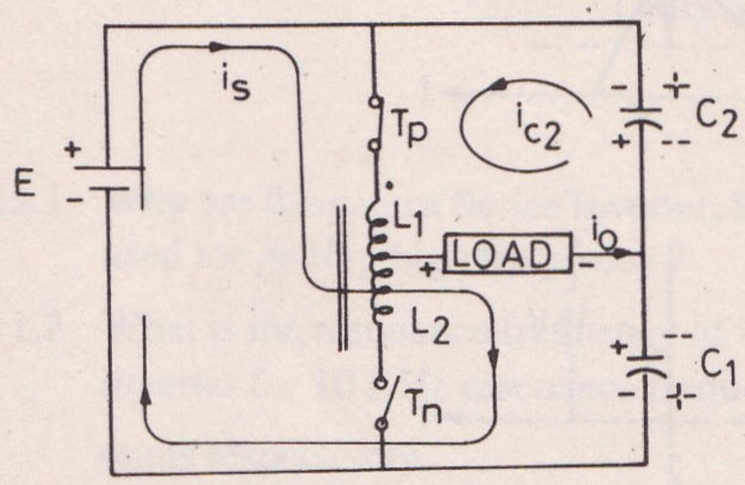
Where:
f_i → Inverter freq.
f_r → Ringing freq. of the circuit

FIG.4.51: (a) POWER CIRCUIT OF A MODIFIED SERIES-INVERTER
(b) LOAD-CURRENT WAVEFORMS FOR THREE RANGES OF THE INVERTER FREQUENCY

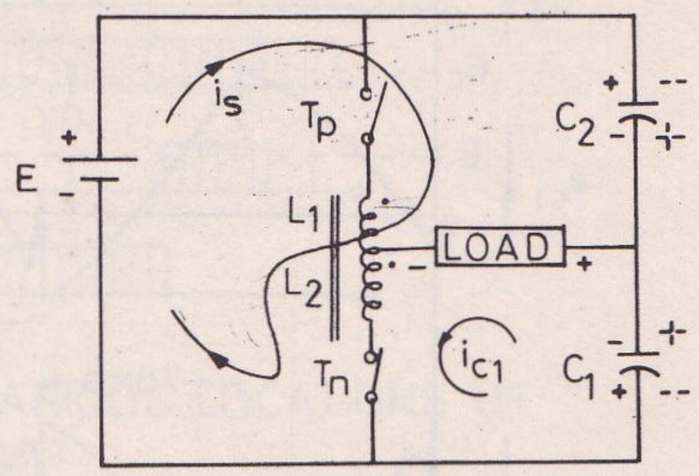
The same voltage $(e_{C2}+e_o)$ will appear across L_2 because inductors L_1 and L_2 are coupled tightly. So, a resultant reverse biased voltage will appear across the thyristor T_n. The load current (i_o) is transferred from thyristor T_n to thyristor T_p with positive polarity. Consequently, thyristor T_n is turned-off (Mode II). The supply current (i_s) now follows through source E, T_p, L_1. Load, C_1, E, and current i_{C2} flows through C_2, T_p, L_1, Load, C_2. Therefore, when T_p is conducting, part of the load current is supplied from the source (E) while the rest is supplied by the discharging capacitor C_2. The polarities of C_1 and C_2 change as shown in Mode II when load current i_o decreases from its positive peak. Now, triggering pulse is applied to thyristor T_n before load current i_o has become zero and the circuit works as shown in Mode III. Load current (i_o) is transferred from T_p to T_n. The supply current now flows through E, C_2 Load, L_2, T_n, E while the current i_{C1} flows through C_1, Load, L_2, T_n, C_1. The modes repeat cyclically. The voltage and current waveform are shown in Fig. 4.53.



Mode I: When $0 < i_o < i_{omax}$ and i_o decreasing from i_{omax}



Mode II: When thyristor T_p is turned-on



Mode III: When thyristor T_n is turned-on

Where: + & – : Show polarity of components at the end of mode

÷ &--- : Show polarity of components at the start of the mode

FIG.4.52: OPERATING MODES OF THE MODIFIED SERIES INVERTER SHOWN IN FIG. 4.51(a)

Firing Circuit

Fig. 4.54 shows the diagram of a triggering circuit for the Modified Series-Inverter. An astable multivibrator of variable frequency decides the triggering frequency (also the inverter- frequency, f_i) of inverter's thyristors and it can be varied from 50 Hz to 2 KHz with the help of variable resistance pot 47K (P). The carrier frequency (about 16 KHz) is generated from another astable multivibrator. These pulses are applied to logic control circuit and driver circuit. The generated pulses are gated to thyristors of the inverter through pulse transformers.

Test Procedure

Make the necessary connections between the firing circuit of Fig. 4.54 and the power circuit shown in Fig. 4.51(a). Release the gate pulses to thyristors T_p and T_n from the triggering circuit.

Observations

1. Observe the load voltage (e_o) and source current (i_s) waveforms for the following frequency ranges :
   (i) $f_i < f_r$, (ii) $f_i = f_r$, (iii) $f_i > f_r$
2. Measure the resonance frequency by noting down the time duration for one-cycle. And note the difference between the calculated and measured values of the resonance frequency.
3. Determine the maximum possible inverter frequency obtainable without commutation failure.

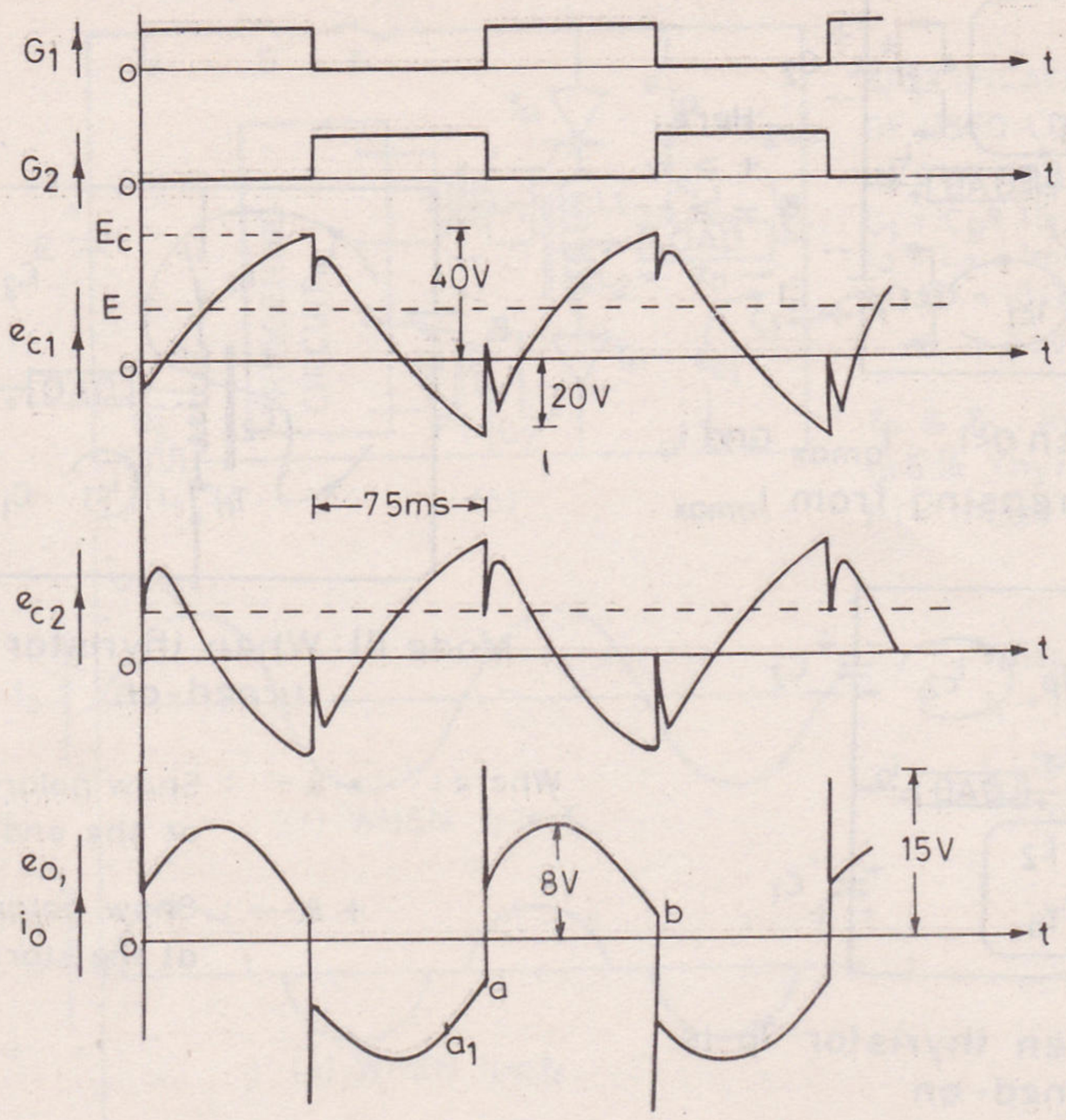
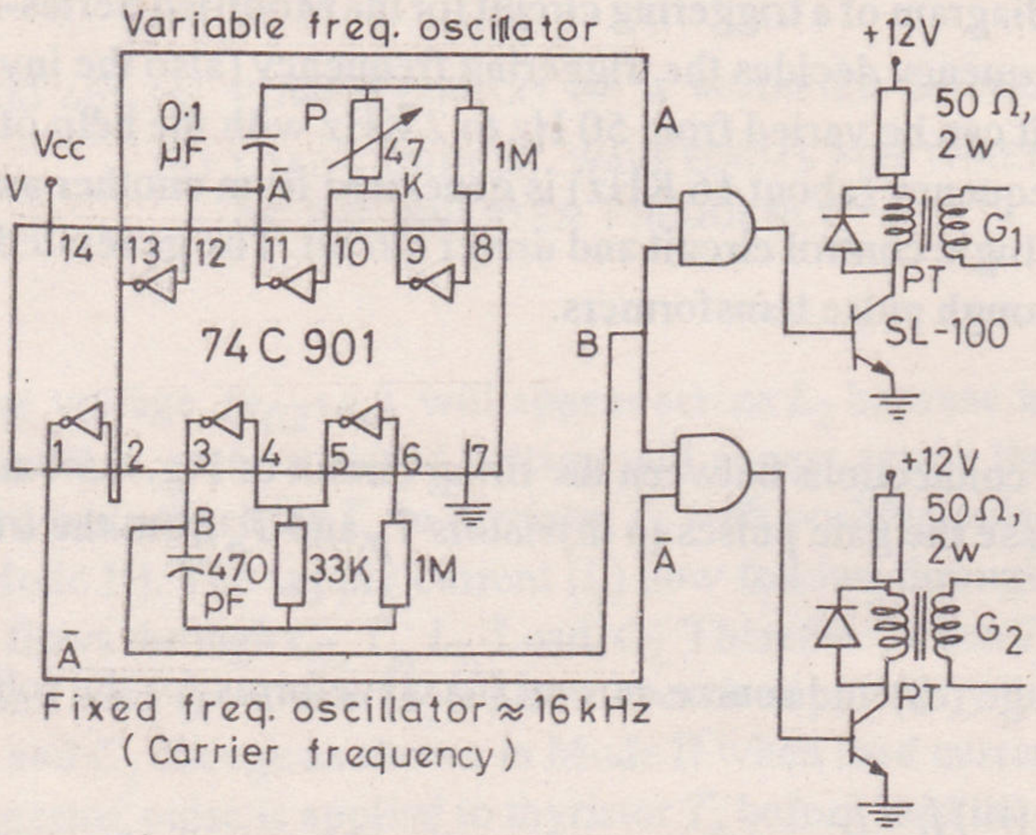


FIG. 4·53 WAVEFORMS AT VARIOUS LOCATIONS OF THE SERIES INVERTER WHEN $f_i > f_r$



FIG·4·54: TRIGGERING CIRCUIT FOR SERIES INVERTER

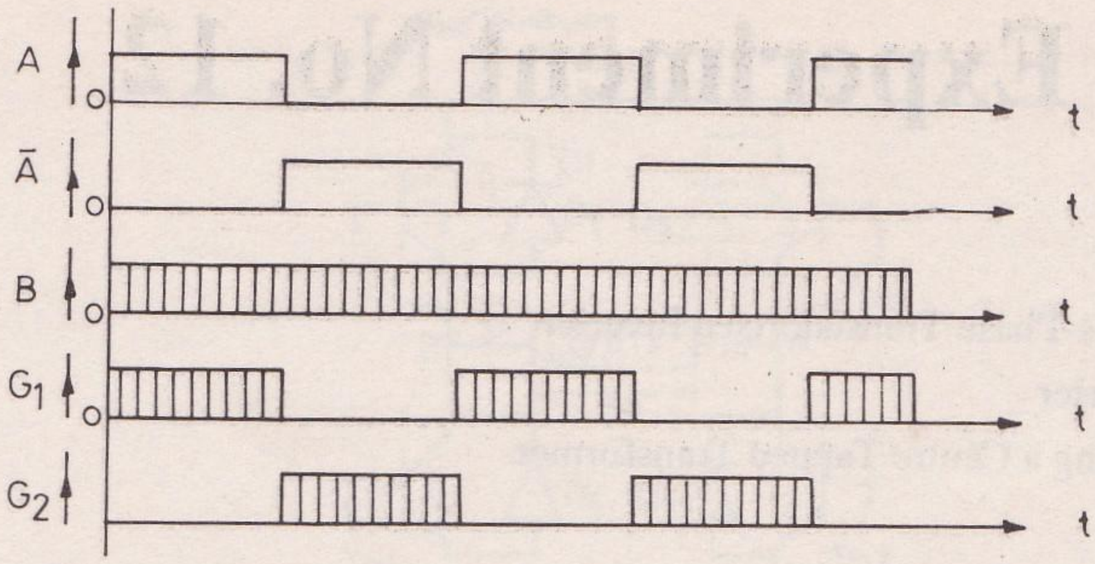


FIG.4.55: WAVEFORMS AT VARIOUS LOCATIONS OF TRIGGERING CIRCUIT

QUESTIONS

11.1 Why are the names Series Inverter, Parallel Inverter and Bridge Inverter used ? What type of inverter is used for getting high frequency ?

11.2 What is the resonance frequency of the inverter ? Calculate the value of the capacitor in the *R-L-C* series inverter for 10 KHz resonance frequency, when the value of the inductor (L) and Load are 2 mH and 15 ohms respectively.

11.3 Draw and explain series inverter (other than modified series inverters shown in Fig. 4.51(a) using two thyristors, an inductor, a capacitor and a resistive load. Can this circuit be operated beyond the resonance frequency ? Explain.

11.4 Draw the block diagram of converter for operating a 1-ϕ induction furnace of 220V, 1 KW and 500 Hz from a 3–ϕ. 440 V, 50 Hz supply.

11.5 A L-R-C series inverter has the following data :

applied dc voltage (E) = 200 V, L = 200 μH, C = 10 μF and assume that the inverter is ideal.

Calculate :

(i) The maximum value of load resistor, so that the inverter works in ideal conditions. And select the value of the load resistance, so that the sinusoidal voltage can be obtained across the load.
(ii) RMS value of the fundamental load current.
(iii) RMS value of the fundamental inductor voltage.
(iv) RMS value of the fundamental capacitor voltage.
(v) Output power (across resistor).
(vi) The maximum output frequency if thyristor's turn-off time is 20 μs.
(vii) What happens if the frequency of the triggering circuit is kept more than the calculated inverter frequency in (vi) ?

[Hint : For underdamped condition $R^2 < (4\,L/c)$; for obtaining a fairly sinusoidal voltage across load : $5 > \left(\frac{WL}{R}\right) > 2$ and RMS value of the fundamental load current $= \frac{\sqrt{2E}}{\pi Z} \angle \phi$; where Z : total impedance of the R-L-C series circuit & ϕ : phase-difference between the load voltage & load current and $\tan \phi = \frac{wL - (1/wC)}{R}$]

Experiment No. 12

Objective : To study Single-Phase Transistorised Inverter.

12.1 : Bridge Inverter

12.2 : Inverter Using a Centre Tapped Transformer

Apparatus Required

Oscilloscope, Transistor and Diode lab. module, Fabricated control circuit, Low voltage dc power supply for the control circuit, Shunts, Loads (*R*-load and *R-L* load), Centre-tapped power transformer.

12.1 BRIDGE INVERTER

Theory

Fig. 4.56 shows the power circuit of a transistorised 1–ϕ Inverter. The transistors have low turn-off times and require no commutation circuits. Consequently, the transistor inverter is well suited for PWM (Pulse Width Modulation) operation and is more compact compared to a thyristor inverter. Fig. 4.57 shows the base to emitter voltage waveforms (V_{b1}, V_{b2}, V_{b3} and V_{b4}) required by the power-transistors for the necessary operation. The figure also shows waveforms across other elements.

Let transistors T_3 and T_4 be conducting at any instant t_o and the load current (i_o) is flowing from A to B (–ve half cycle). Now the base bias is removed for the transistors T_3 and T_4 at instant t_o. Transistors T_3 and T_4 stop conducting and the remaining negative cycle of load current (i_o) is completed through E, D_2, Load, D_1, E. The base drives for transistors T_1 and T_2 are applied starting from time t_o. But transistors T_1 and T_2 do not conduct till the instant t_1, because the conduting diodes D_1 and D_2 apply a reverse bias of around 0.6 volts across them.

At instant t_1, diodes D_1 and D_2 stop conducting because the current has ceased to flow. Transistors T_1 and T_2 conduct and the load current flows from B to A. At instant t_2 the base drives of transistors T_1 and T_2 are withdrawn. Hence, diodes D_3 and D_4 conduct in the duration t_3–t_2 and the load current decreases to zero at t_3. Transistors T_3 and T_4 which have been biased from time t_2 onwards, conduct for a period t_4–t_3. At instant t_4, the next cycle starts.

Control Circuit

We cannot use a single power supply for supplying the firing pulses to all transistors T_1, T_2, T_3 and T_4, because their emitters are connected at different points. Minimum three isolated power supplies are required (Fig. 4.60). Since emitters of T_2 and T_4 are connected at the same point, so one can use the same power supply for driving the bases of T_2 and T_4.

The control circuit of a transistorised inverter is shown in Fig. 4.58. And Fig. 4.59 shows waveforms at different stages of the control circuit. For the driving stage, a push-pull amplifier configuration is used. Thus, both positive and negative voltage can be applied to the base of each power transistor. A negative voltage at the base of the power transistor w.r.t. emitter helps to turn-off fast.

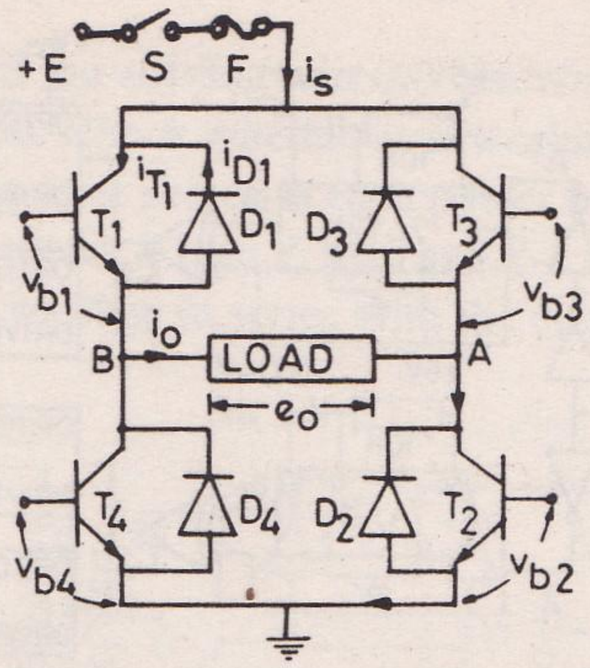


FIG.4.56: POWER CIRCUIT OF THE SINGLE PHASE BRIDGE INVERTER

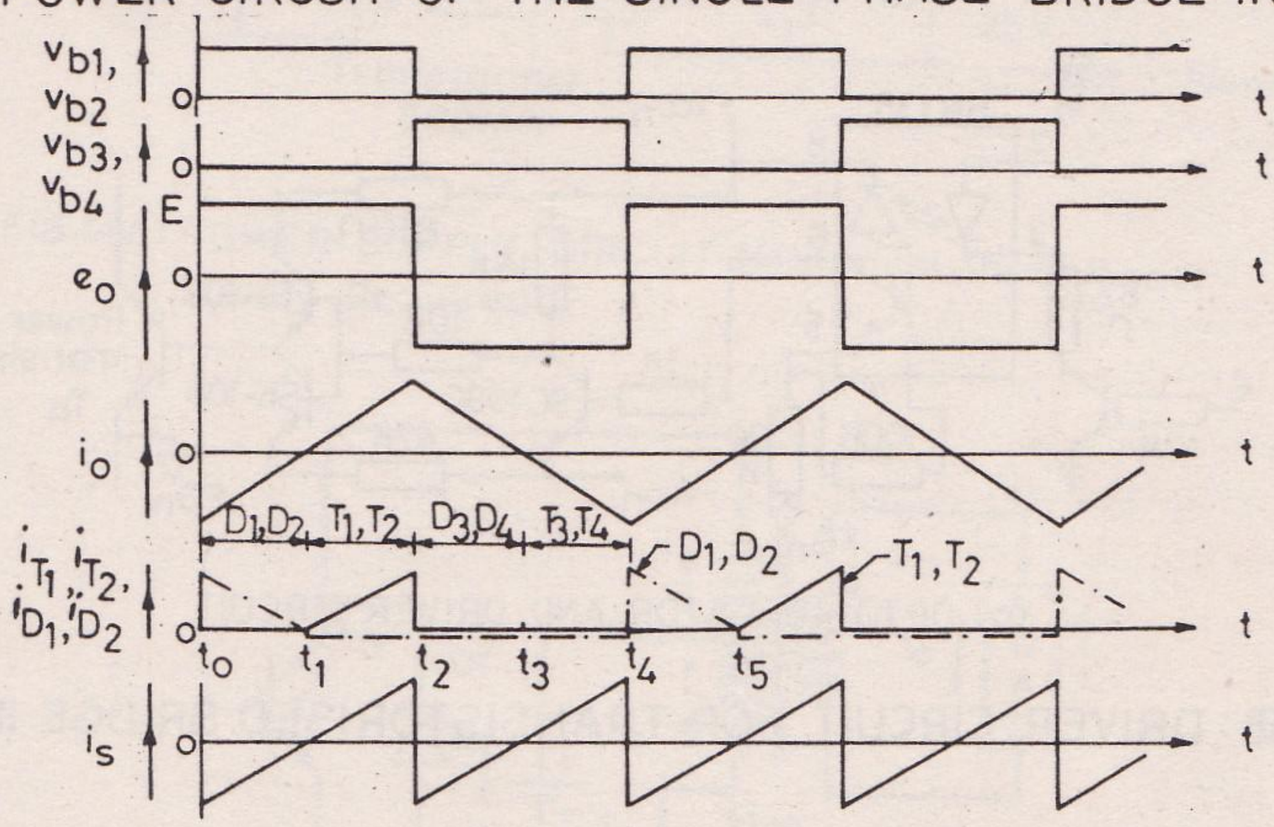


FIG.4.57 : WAVEFORMS AT VARIOUS LOCATIONS OF THE BRIDGE INVERTER FOR HIGH INDUCTIVE LOAD

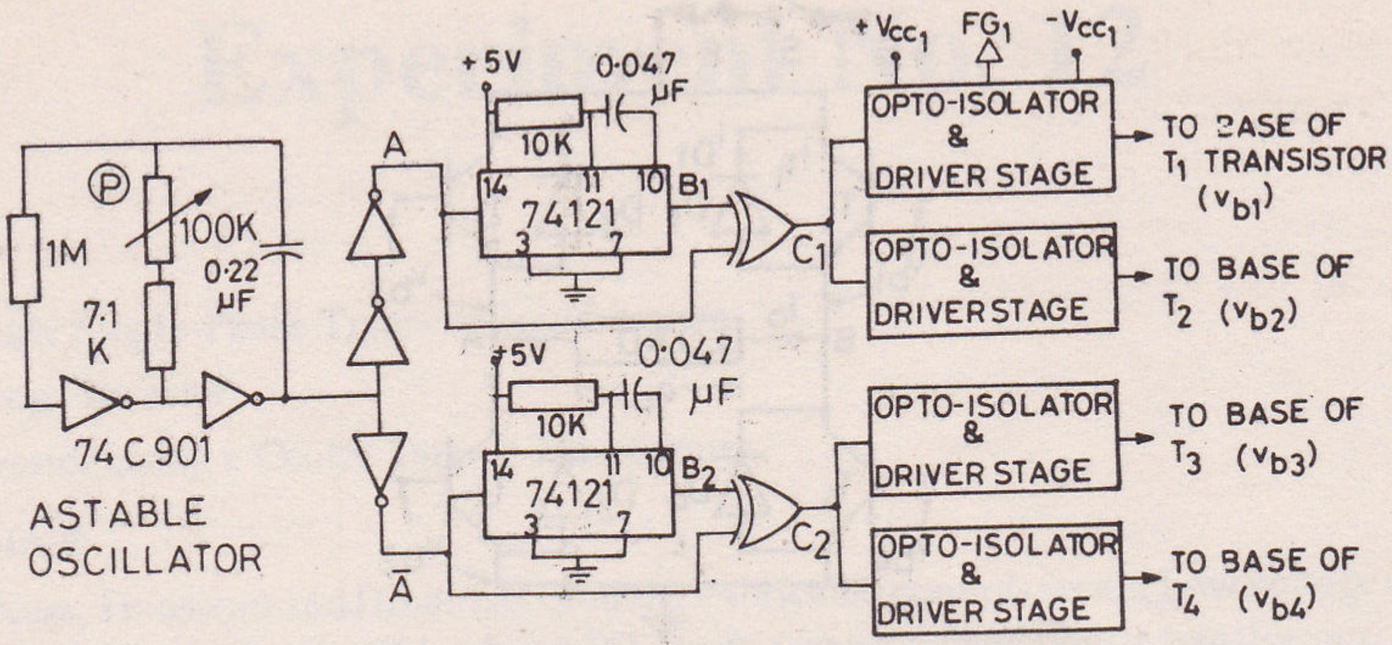
Test Procedure

Activate the driving-circuit shown in Fig. 4.58. Check whether it works as expected. If it is working as expected, connect it with the power circuit of Fig. 4.56. Release the power transistor base drives. Observe the waveforms across each element of the power circuit with *R* and *R-L* loads. Use a non-inductive resistor of less than 1Ω of necessary wattage in series with the element, whose current waveform is to be observed.

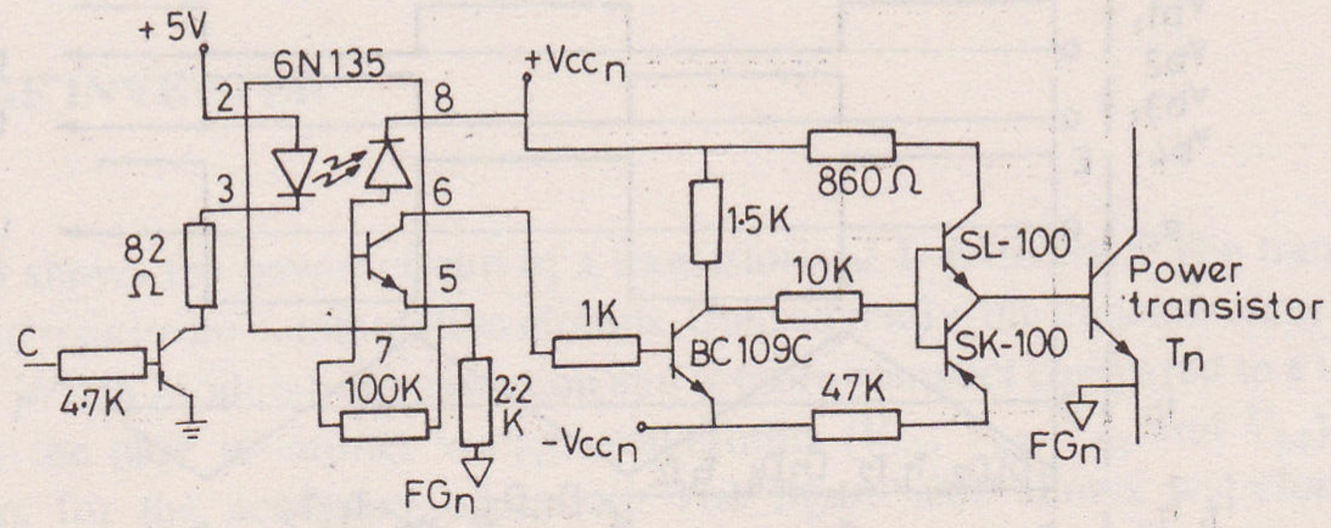
12.2 SINGLE-PHASE INVERTER USING A CENTRE TAPPED TRANSFORMER

Description

By using a centre tapped power transformer in the transistor inverter as shown in Fig. 4.61, one can save two power transistors and two power diodes, as compared to the inverter discussed earlier. This inverter is similar to the earlier one. Further, a separate power supply for each transistor is not required because the emitters of transistors T_1 and T_2 are connected together. Block-diagram of the triggering-circuit is shown in Fig. 4.62.



(a) CONTROL CIRCUIT



(b) OPTO-ISOLATOR AND DRIVER CIRCUIT

FIG.4·58: DRIVER CIRCUIT FOR TRANSISTORISED BRIDGE INVERTER

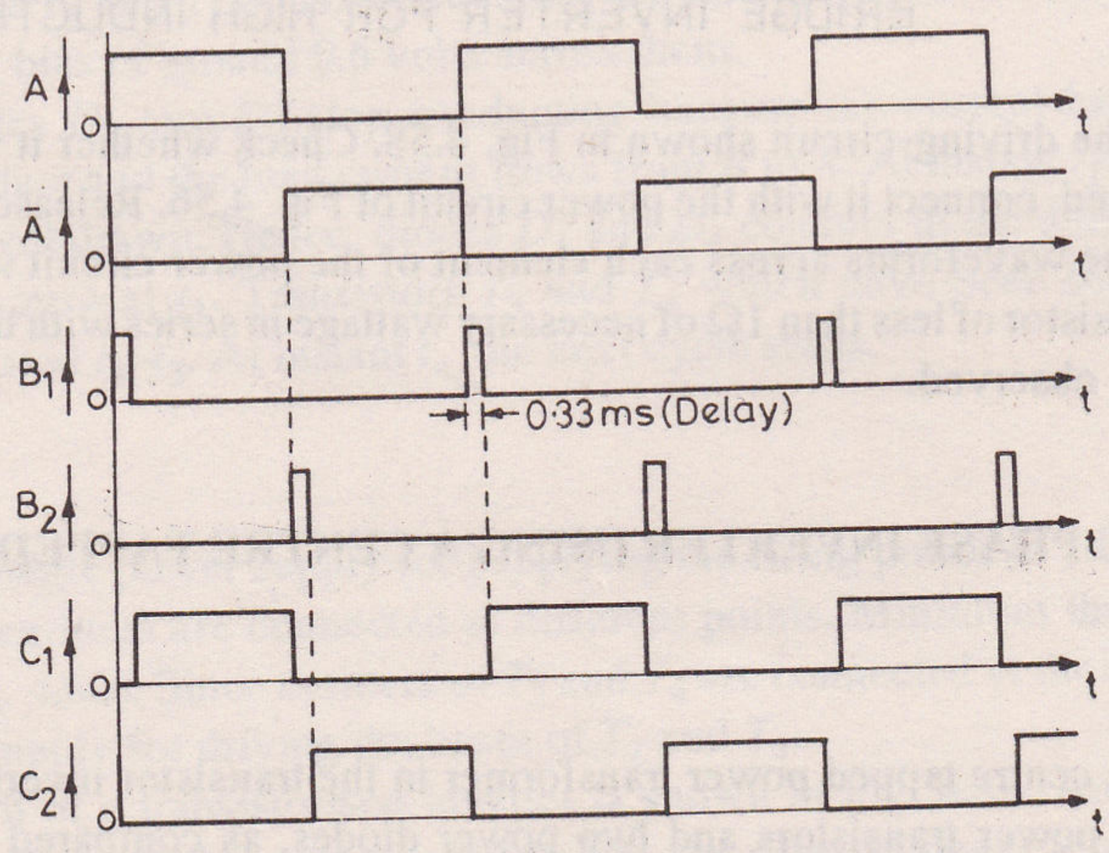


FIG.4·59: WAVEFORMS AT VARIOUS LOCATIONS OF CONTROL-CIRCUIT SHOWN IN FIG.4·58

Procedure

Activate the block diagram of the driving circuit shown in Fig. 4.62. This circuit can be built-up with the help of the Fig. 4.58. Check whether it is working as expected. Connect it to the power circuit of Fig. 4.61. Release the base drives to each power transistor. Observe the waveforms across each element of the power circuit for *R* load, *L* load and *R-L* load. Use a non-inductive resistor of value about 1Ω and of necessary wattage in series with the element whose current waveform is to be observed.

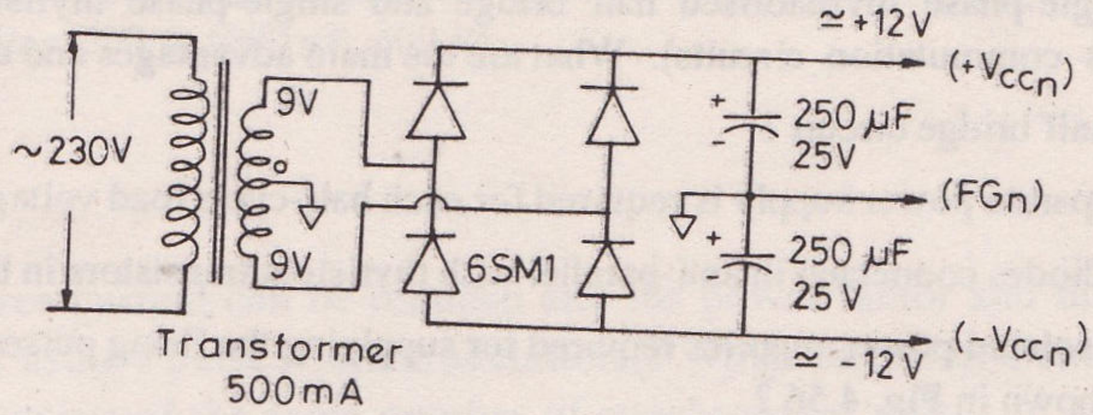


FIG.4.60: POWER SUPPLY CIRCUIT (Minimum Three Power Supply Required)

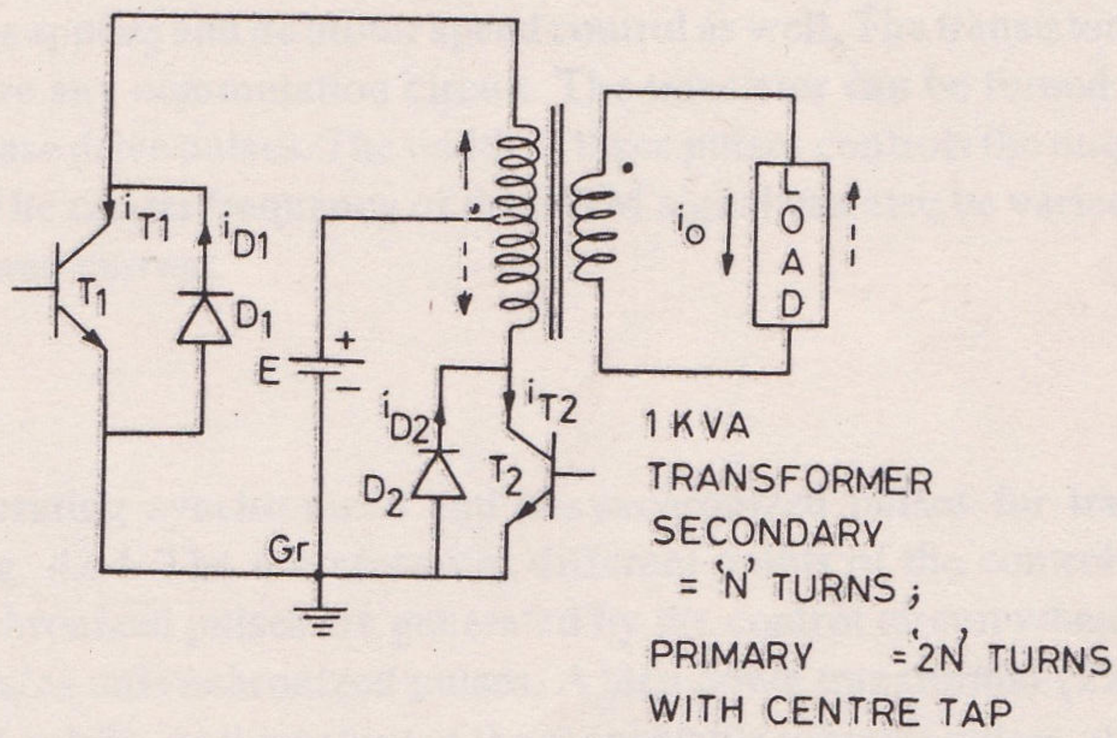


FIG.4.61: POWER CIRCUIT OF TRANSISTORISED INVERTER WITH CENTRE TAPPED POWER TRANSFORMER

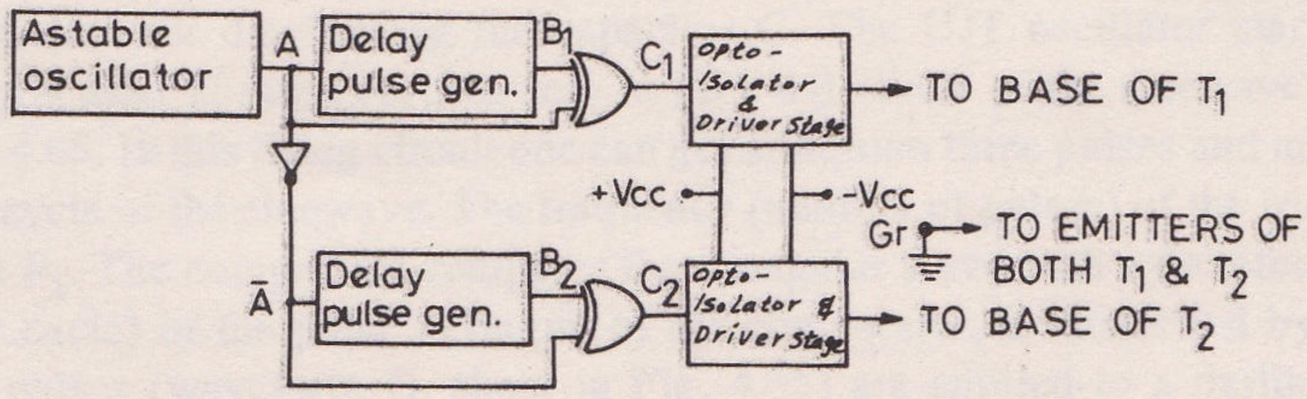


FIG.4.62: BLOCK-DIAGRAM OF THE CONTROL CIRCUIT FOR TRANSISTORISED INVERTER SHOWN IN FIG. 4.61

QUESTIONS

12.1 Generally, why is the transistorised bridge inverter preferred over a thyristorised bridge inverter ?

12.2 Draw and explain the block diagrams for controlling a 3–ϕ, 100 Hz induction motor from the following power supplies :

(i) DC power supply
(ii) Single-phase power supply of 50 Hz.
(iii) Three-phase power supply of 50 Hz.

12.3 Draw single-phase thyristorised half bridge and single-phase thyristorise d bridge inverters (without thyristor's commutation circuits). What are the main advantages and disadvantages of the bridge circuit over the half bridge circuit ?

[Hint : Separate power supply is required for each half-cycle load voltage]

12.4 Why are diodes connected in anti-parallel with thyristors/transistors in the bridge inverter circuit ?

12.5. Why are isolated power supplies required for supplying the firing pulses for all transistors of the bridge inverter shown in Fig. 4.56 ?

Experiment No. 13

Objective : To study a Transistorised Single-phase PWM Converter.

Apparatus Required

Oscilloscope, Transistor and Diode lab. module, Fabricated control circuit, Loads (*R*-load, *R-L* load and dc motor) and Electrolytic capacitor (500 to 1000 μF, 400 *V*).

Description

Harmonics in the source current can be reduced and the power factor and the load current waveform can be improved by using a pulse width modulation (PWM) converter. Generally, the load voltage of PWM converter consists of the same number of synchronized pulses of equal widths in each half cycle. However, if the number of pulses per half cycle is five or more, then the pulses need not be synchronised.

An AC to DC converter employing equal pulse width modulation (PWM) is shown in Fig. 4.63. This simple circuit is chosen, to illustrate the principle of PWM. Such PWM converters find application in variable dc power supplies and dc motor speed control as well. The transistorized PWM converter circuit does not require any commutation circuit. The transistor can be turned on and off several times by using suitable base drive pulses. The width of these pulses controls the output voltage which can be smoothly varied. The carrier frequency of the PWM signal can also be varied to control the ripple in the output voltage and current.

Control Circuit

Control circuit for generating synchronized and unsynchronized pulses for transistorised PWM converter is shown in Fig. 4.64. The waveforms at different points of the control circuit are shown in Fig. 4.65(a). The synchronized pulses are generated by the control circuit when the switch '*S*' is closed, otherwise it generates unsynchronized pulses. A step down transformer (220*V* : 6*V*) is used for obtaining synchronized pulses. At the output of the monostable vibrator pulses of about 0.03 ms duration are obtained at each zero crossing point of the sine-wave, as shown by *D*-wave in Fig. 4.65. The duration of the discharge of capacitor *C* (0.05μ*F*) of the UJT triangular wave (carrier) generator, through transistor (*SL*-100) and 100 Ω resistor is about 0.005 *ms*. Thus, a pulse of 0.03 ms duration is sufficient for discharging the capacitor *C*. The UJT oscillator starts generating triangular pulses again after *D*-pulse reaches zero in each half-cycle of the sinewave as shown by waveform *E* in Fig. 4.65. In this firing circuit one can get minimum three pulses and maximum nine pulses in each half-cycle of the sinewave. The frequency (number of pulses) of the triangular wave is controlled by Pot P_1. The comparator compares the triangular wave with a dc reference voltage. The width (or duty cycle) of the pulse at output of the comparator, is controlled by pot P_2. The comparator output pulses (waveform G, show in Fig. 4.65) are applied to a darlington pair for amplification and the amplified pulses are applied to the base of the power transistor in the PWM

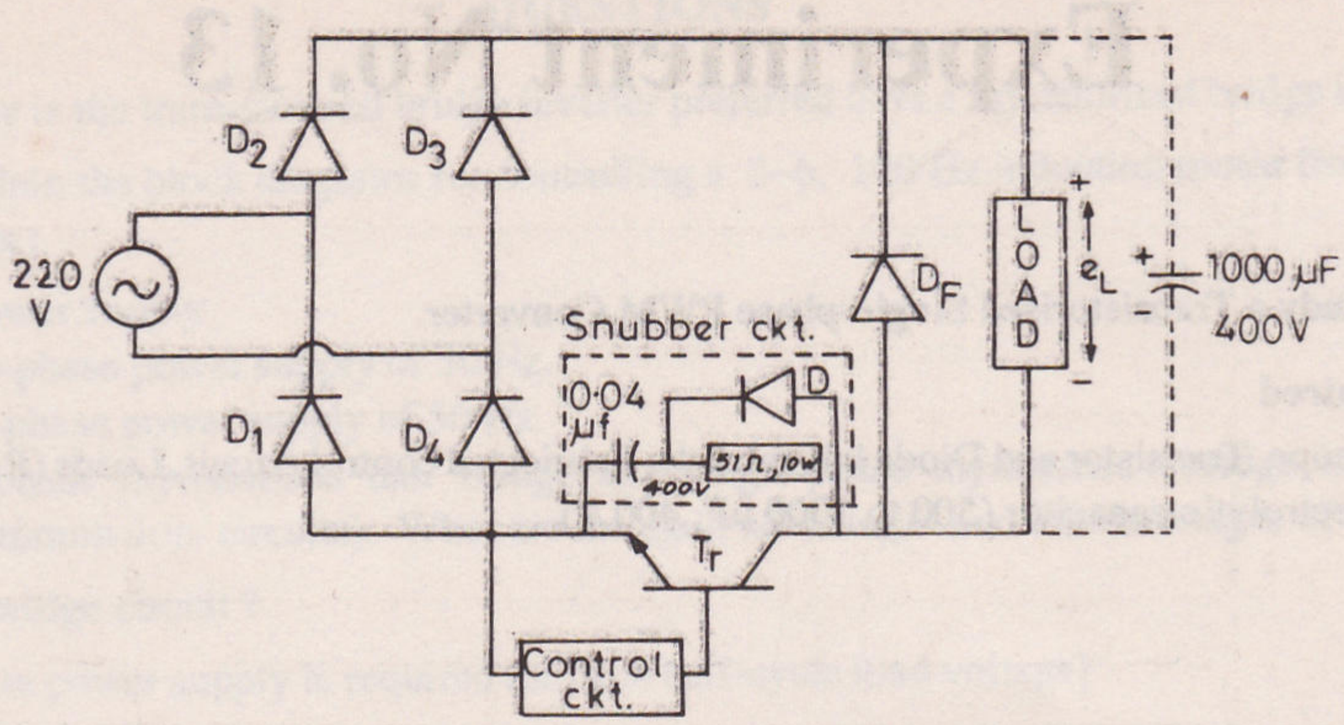


FIG.4·63: POWER CIRCUIT OF SINGLE PHASE PWM CONVERTER EMPLOYING A TRANSISTOR

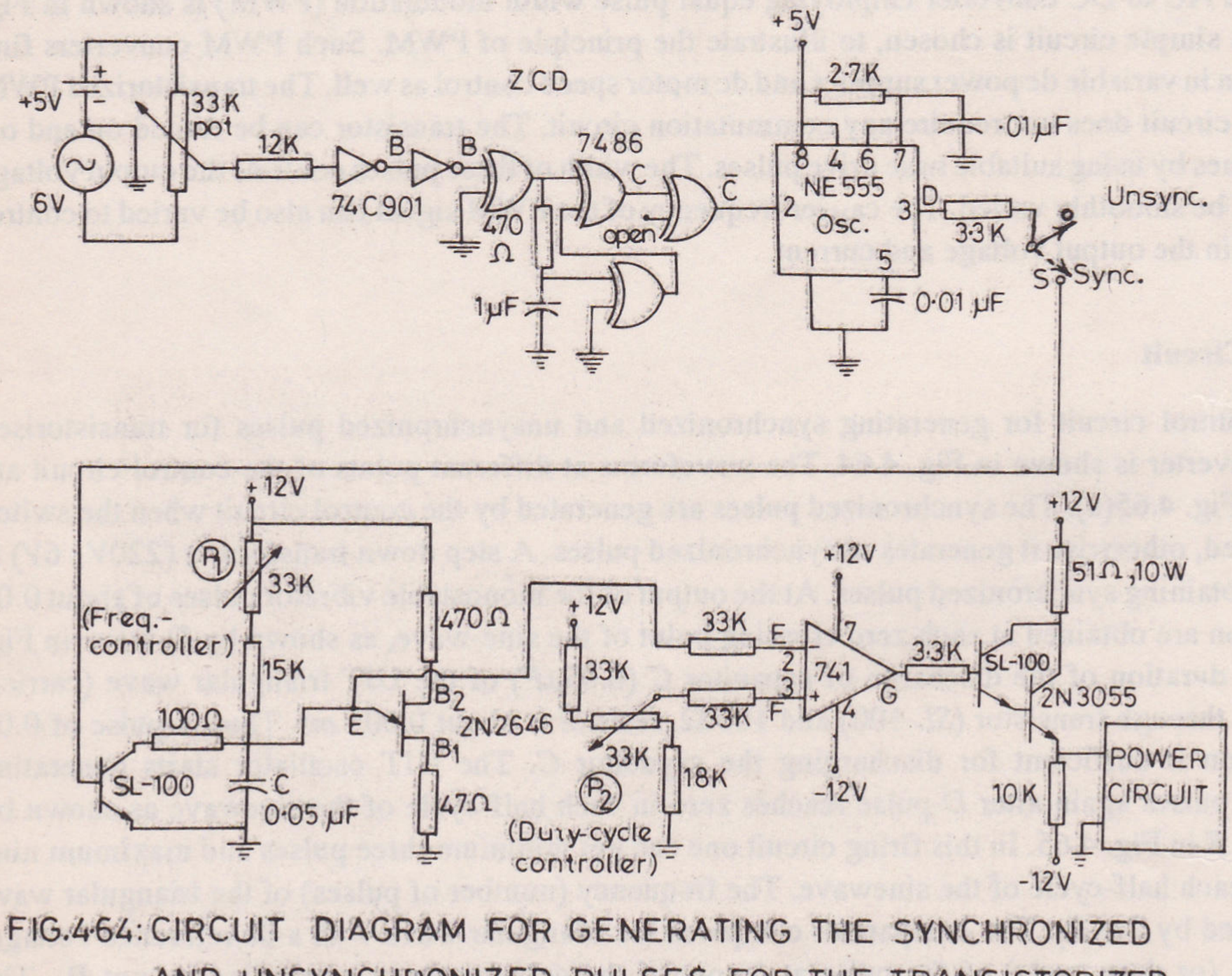


FIG.4·64: CIRCUIT DIAGRAM FOR GENERATING THE SYNCHRONIZED AND UNSYNCHRONIZED PULSES FOR THE TRANSISTORIZED PWM CONVERTER

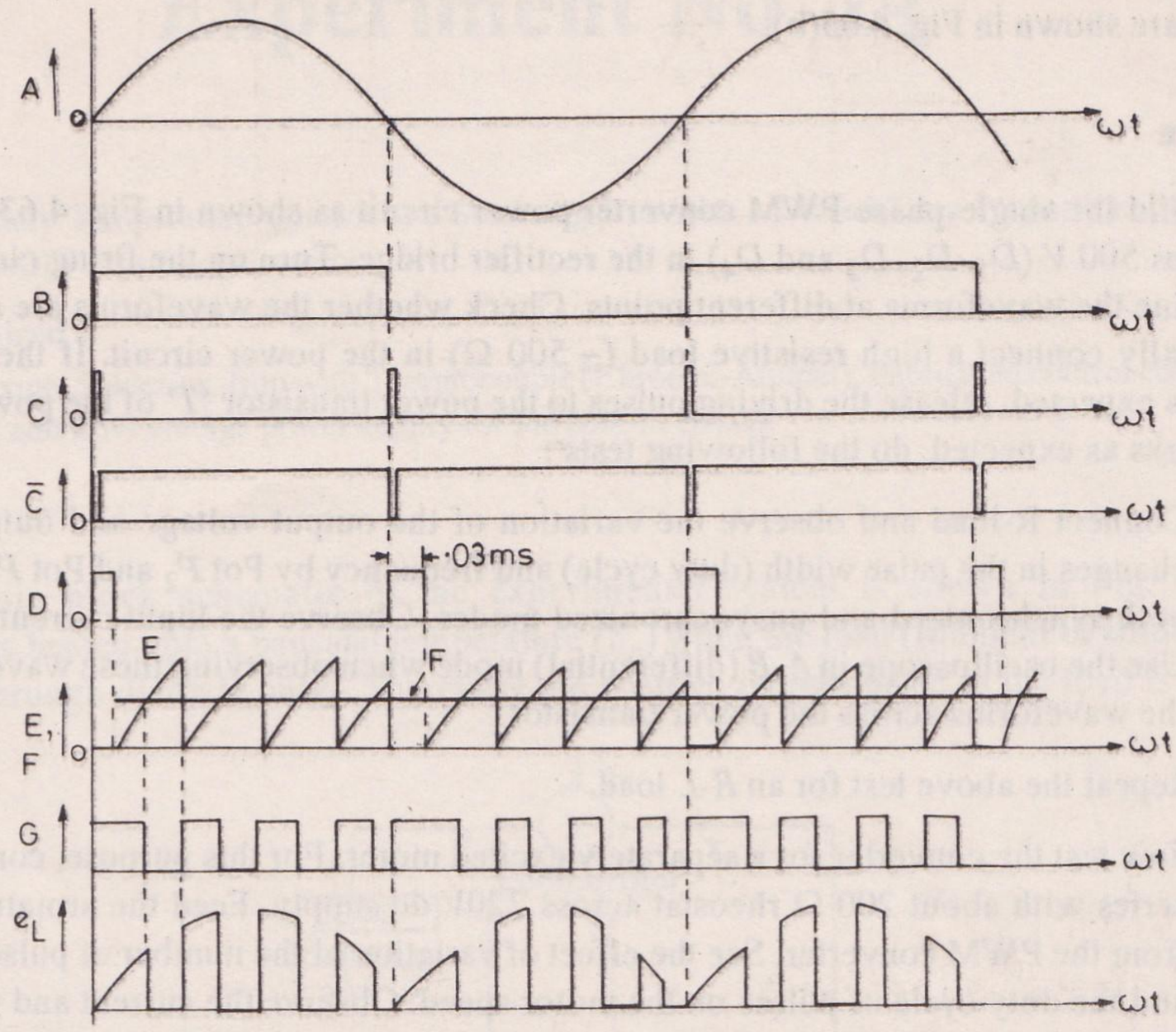


FIG. 4·65(a) : WAVE FORMS AT VARIOUS LOCATICNS OF THE FIRING CIRCUIT

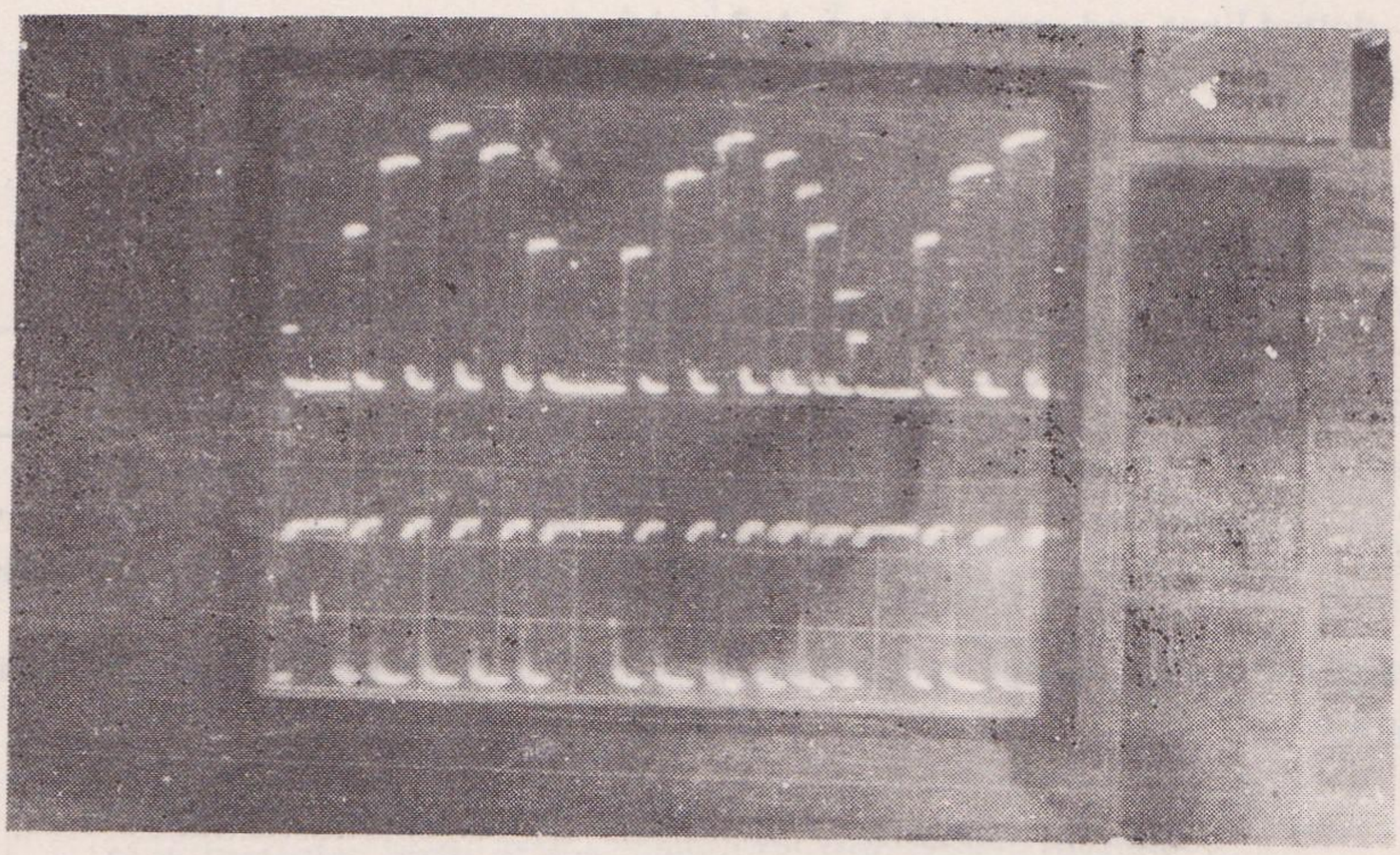


FIG. 4.65(b) : OSCILLOGRAM OF A TRANSISTORISED SINGLE-PHASE PWM CONVERTER
TOP : LOAD VOLTAGE
BOTTOM : BASE DRIVE PULSES TO POWER TRANSISTOR

converter power circuit (Fig. 4.63). Oscillograms of load voltage and base-drive pulses to power transistor are shown in Fig. 4.65(b).

Procedure

Build the single-phase PWM converter power circuit as shown in Fig. 4.63. Use the diodes of 10 Amps 500 *V* (D_1, D_2, D_3 and D_4) in the rectifier bridge. Turn on the firing circuit of Fig. 4.64 and examine the waveforms at different points. Check whether the waveforms are as shown in Fig. 4.65. Initially connect a high resistive load ($\simeq$ 500 Ω) in the power circuit. If the firing circuit is working as expected, release the driving pulses to the power transistor '*T*' of the power circuit. If the circuit works as expected, do the following tests :

Test 1 : Connect R-load and observe the variation of the output voltage and output current with changes in the pulse width (duty cycle) and frequency by Pot P_2 and Pot P_1 respectively in both synchronized and unsynchronized modes. Observe the input current waveform also. Use the oscilloscope in *A-B* (differential) mode when observing these waveforms. Also see the waveforms across the power transistor.

Test 2 : Repeat the above test for an *R-L* load.

Test 3 : Now test the converter for a separately excited motor. For this purpose, connect the field in series with about 200 Ω rheostat across 220*V* dc supply. Feed the armature of the motor from the PWM converter. See the effect of variation of the number of pulses per half-cycle and the duty cycle of pulses on the motor speed. Observe the current and terminal voltage waveforms of the motor armature. Also observe the source current of the PWM converter.

Test 4 : Connect a capacitor at the output terminals of the PWM converter as shown in Fig. 4.63 by dotted lines and carry out tests 1, 2 and 3.

QUESTIONS

13.1 Fill in the blanks :

(i) The PWM converter shown in Fig. 4.63 are used to control _____ of dc power supply and_____ of the dc motor (voltage/speed).

(ii) The PWM converters improve_____ and _____ waveforms.

(iii) The PWM converters reduce_____in the source current.

(iv) The dc motor_____can be controlled by the PWM converter.

(v) The diode (D_1, D_2, D_3 and D_4) bridge converter shown in Fig. 4.63, converts ac supply to _____ _____ .

13.2 Design and explain a simple synchronised triggering circuit for transistorised PWM converter shown in Fig. 4.63.

Experiment No. 14

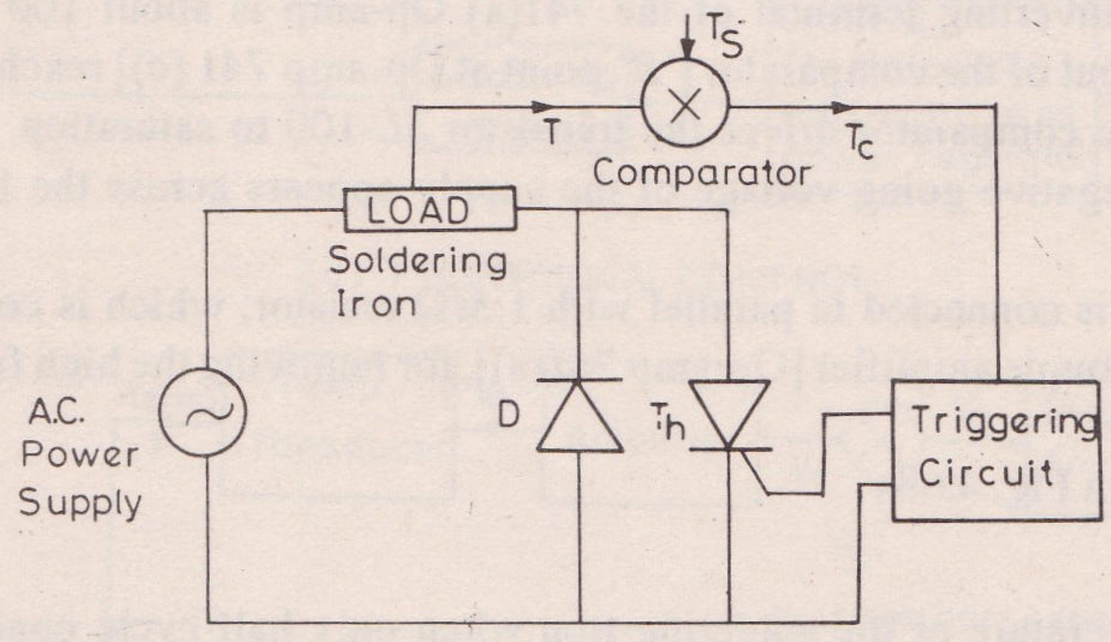
Objective : To study Temperature Control of a Soldering-Iron with a Closed Loop Proportional Control and ON-OFF Hysteresis Control.

Apparatus Required

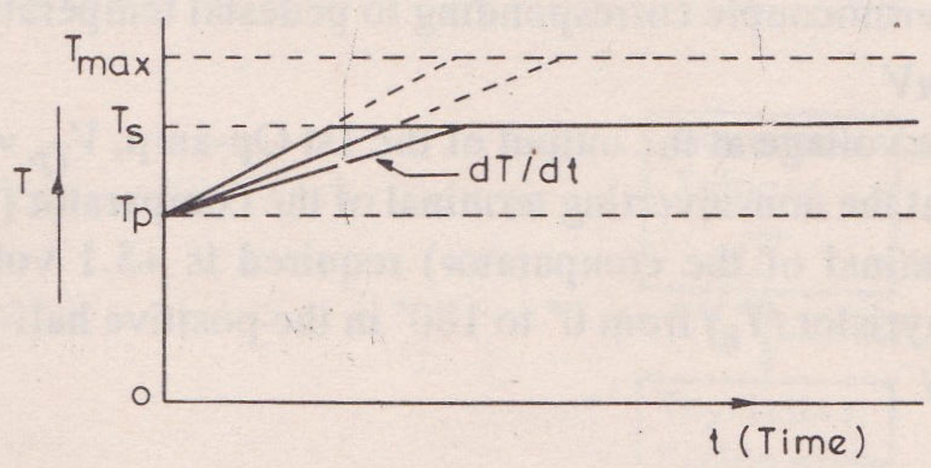
Oscilloscope, Soldering-Iron with Thermocouple (Chromel-Alumel), Fabricated control circuit, Transformer 230*V* : 6*V* and Low voltage power supply for the control circuit.

Description

The basic block schematic of the experimental system is shown in Fig. 4.66. The soldering-iron is heated upto a pedestal temperature (T_p) when the load (filament of soldering-iron) current flows through dicde *D* only. Thereafter the positive current pulse to the load is controlled



(a) BLOCK DIAGRAM



(b) TEMPERATURE OF SOLDERING-IRON w.r.t. TIME

Where:

T = Temp.of Soldering Iron

T_S = Temp. Setling of the Soldering-Iron

T_p = Pedestal Temp. of the Soldering-Iron (When Thyristor T_h is off and load current flows through Diode D only)

T_{max}=Max. Temp. of the Soldering-Iron (When Thyristor T_h is on all the time)

FIG. 4.66 : TEMPERATURE CONTROL SCHEME

with the help of the thyristor while uncontrolled negative current pulse through the diode is maintained as it is. The soldering-iron, thus, can be heated up to a set temperature (T_s; $T_p < T_s < T_{max}$). The temperature of the soldering-iron can be controlled between T_p and T_{max} by controlling the thyristor (T_h) conduction angle. The conduction angle control can be implemented either by the hysteresis band control (ON-OFF control) or the closed loop proportional control. The comparator compares the actual temperature (T) of soldering-iron with the set temperature (T_s). The output of the comparator (T_c) generates the triggering signals for the thyristor in the power circuit.

Fig. 4.67 shows the block diagrams of the two methods, i.e., closed loop proportional control and ON-OFF control. Fig. 4.68 shows corresponding circuit diagrams. The temperature of the soldering-iron is measured by a thermocouple (Chromel-Alumel) which generates 40 μV (micro volts) per ^oC or 22 μV per ^oF.

The voltage V_o generated by the thermocouple depends on the temperaure (T) of the soldering-iron. It is amplified by a non-inverting amplifier [op-amp 741 (a)] with a gain of 1000. For limiting the maximum temperature of the soldering-iron below the safe limit when the thermocouple is opened, resistors 100K, 2K and thermocouple (resistance of thermocouple << 2K) are connected in the 741 (a) Op-amp amplifier circuit as shown in Fig. 4.68. If the thermocouple opens, the input voltage applied at the non-inverting terminal of the 741(a) Op-amp is about 100 mV, hence, it saturates. Therefore, the output of the comparator ['B' point at Op-amp 741 (c)] reaches the positive saturation. The output of the comparator drives the transistor SL-100 to saturation, thyristor (T_h), turns-off and hence, only negative going voltage of the supply appears across the filament of the soldering-iron.

A 1000 pf capacitor is connected in parallel with 1 $M\Omega$ resistor, which is connected in the feedback path of the thermocouple amplifier [Op-amp 741(a)], for removing the high frequency noise in the output of the amplifier.

Consider the circuit in Fig. 4.68.

Suppose $T_p = 100^oC$

where $T_p \rightarrow$ Pedestal Temperature of the soldering-iron when only half-cycle conduction occurs through the diode.

The voltage generated by the thermocouple corresponding to pedestal temperature,

$$V_{op} = 40 \times 100\ \mu V = 4\ mV$$

With the given gain of 1000, the voltage at the output of the 1st Op-amp, $V_{Tp} = 4V$. Since the ramp voltage decays from +5V to 0V at the non-inverting terminal of the comparator [741 (c) op-amp], the voltage V_A at the inverting-terminal of the comparator) required is +5.1 volts to –0.1 volts for controlling the firing angle of thyristor (T_h) from 0° to 180° in the positive half-cycle of the supply. Since the voltage V_D is given by

$$V_D = -\frac{V_A}{1.3}$$

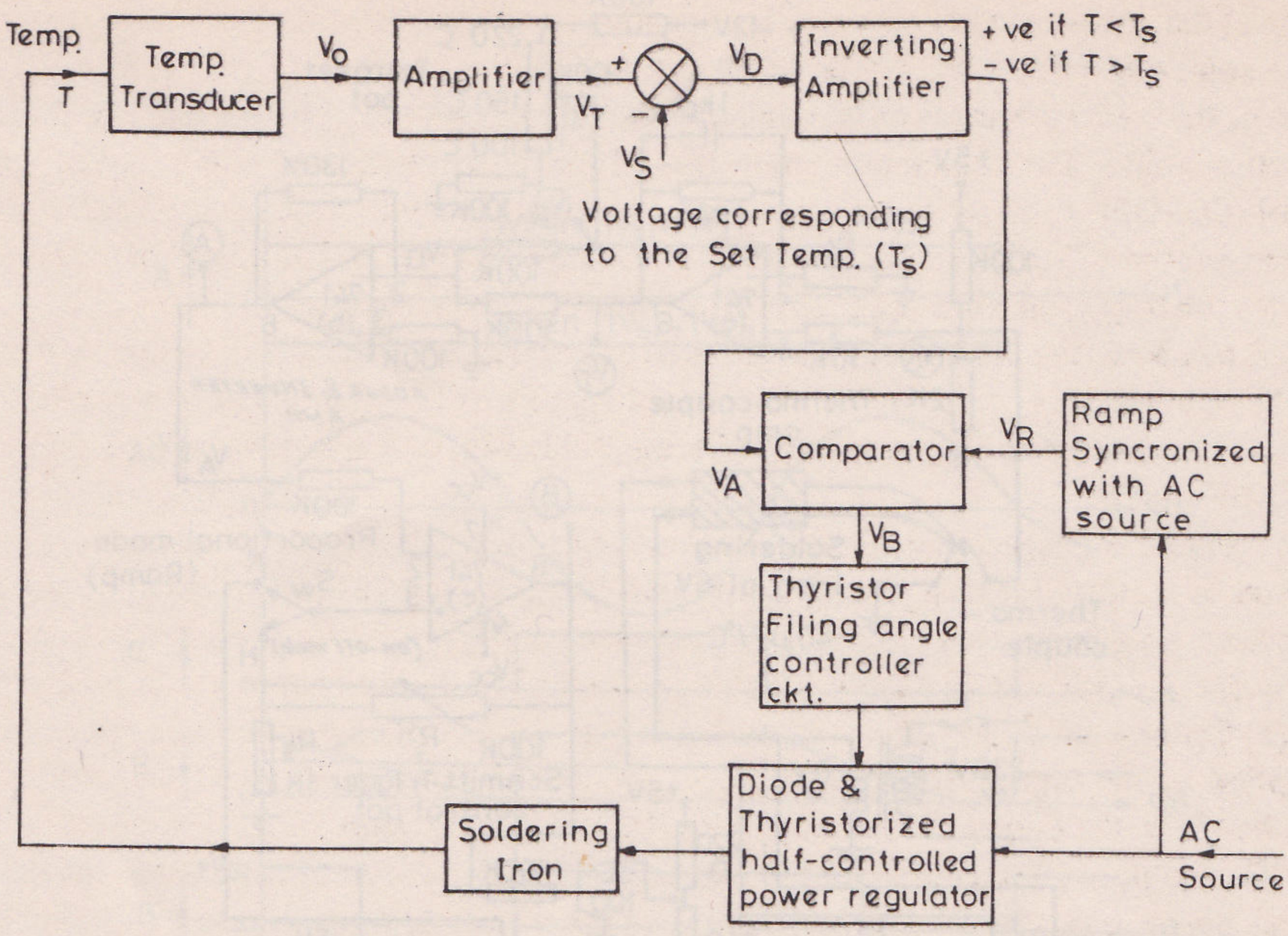
it must vary from 0 to – 4V.

Also $V_D = V_T + V_S$

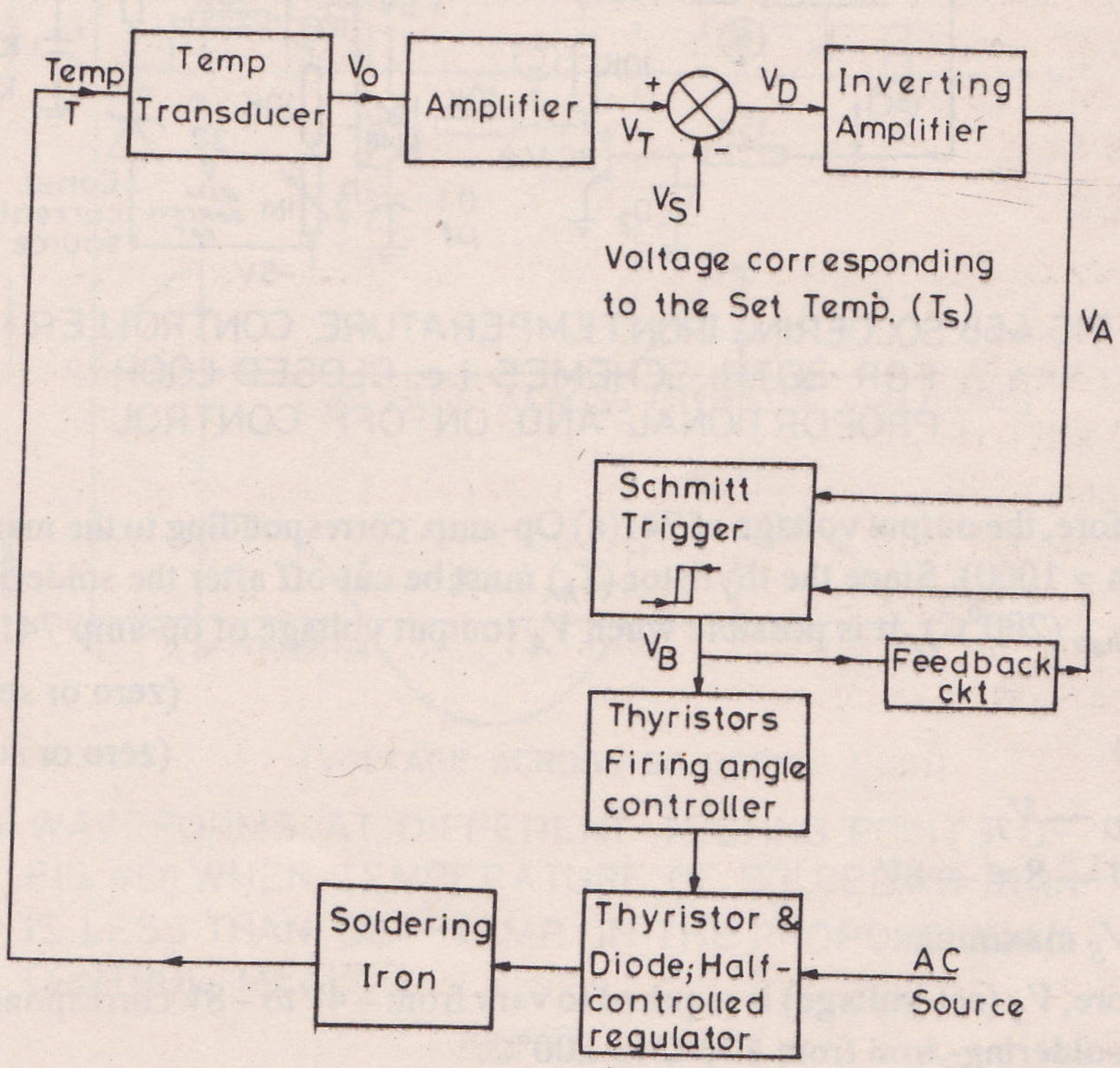
where V_T = Voltage corresponding to actual temperature of the soldering-iron.

V_S = Voltage corresponding to set temperature.

Let the maximum temperature of the soldering-iron be $T_{max} = 200^oC$. Therefore, the voltage generated by the thermocouple corresponding to the maximum temperature of the soldering-iron = 40×200μV



(a) PROPORTIONAL CONTROL



(b) ON-OFF (HYSTERESIS BAND) CONTROL

FIG.467: BLOCK DIAGRAM SHOWS TWO METHODS OF TEMP. CONTROL OF SOLDERING IRON

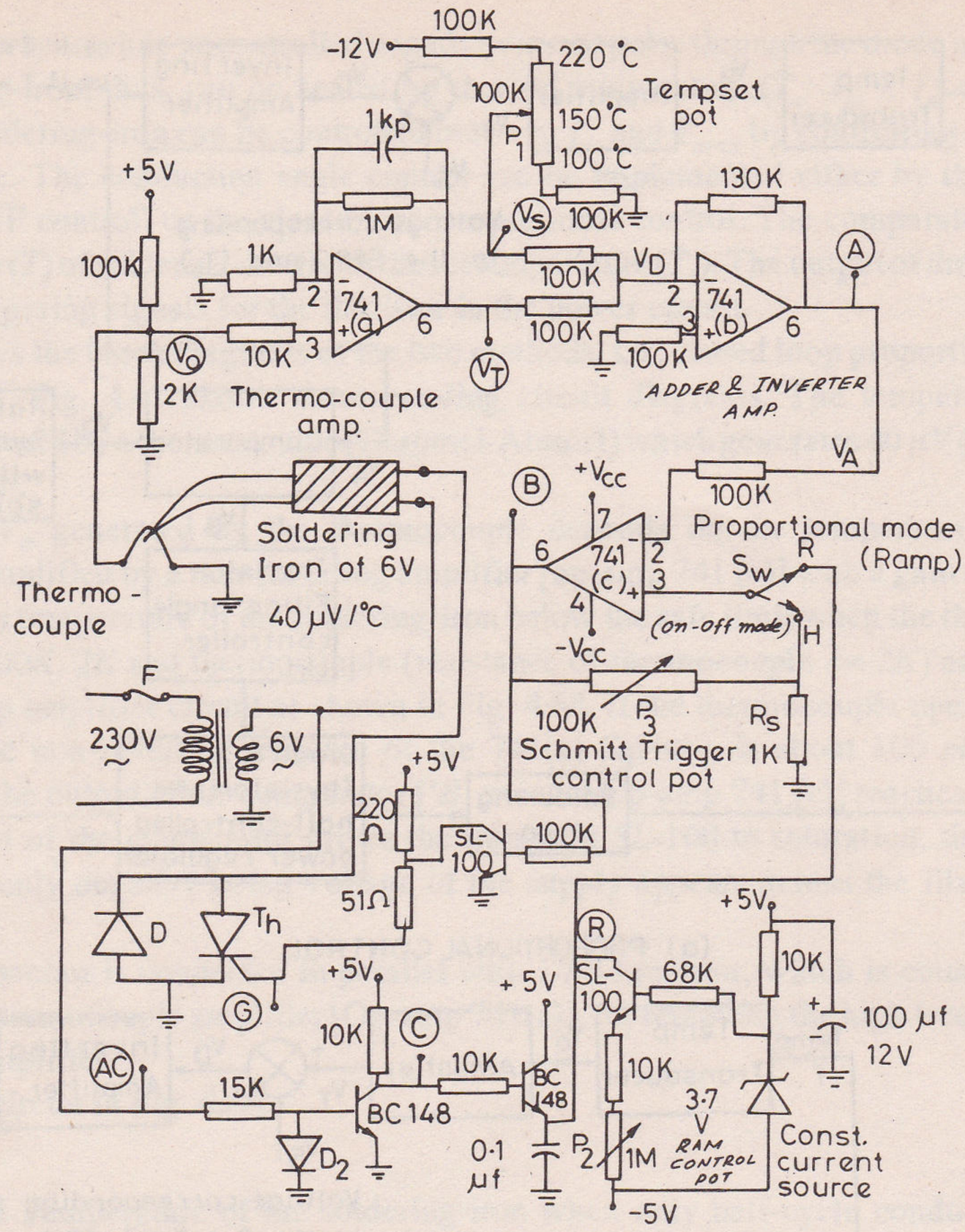


FIG.4·68 SOLDERING IRON TEMPERATURE CONTROLLER FOR BOTH SCHEMES i.e. CLOSED LOOP PROPORTIONAL AND ON-OFF CONTROL

$= 8\,mV$. Therefore, the output voltage of 741(a) Op-amp. corresponding to the maximum temperature $V_{Tm} = 8V$ (gain = 1000). Since the thyristor (T_h) must be cut-off after the soldering-iron reaches the temperature T_{max} (200^oC). It is possible when V_A [output voltage of op-amp 741 (b)] ≤ 0

(zero or some negative value)

So $V_D \geq 0$

(zero or some positive value)

Since $V_S = V_D - V_T$

$V_{sm} = 0 - 8 = -8V$

where $V_{Sm} = V_S$ maximum.

Therefore, V_S (set-voltage) is required to vary from $-4V$ to $-8V$ corresponding to temperature settings of the soldering- iron from 100^oC to 200^oC.

Consider now the soldering-iron to be at 125^oC. We would like to change this temperature of the soldering-iron to 150^oC [by setting the temperature Set-Pot (P_1) to 150^oC]. Thus,

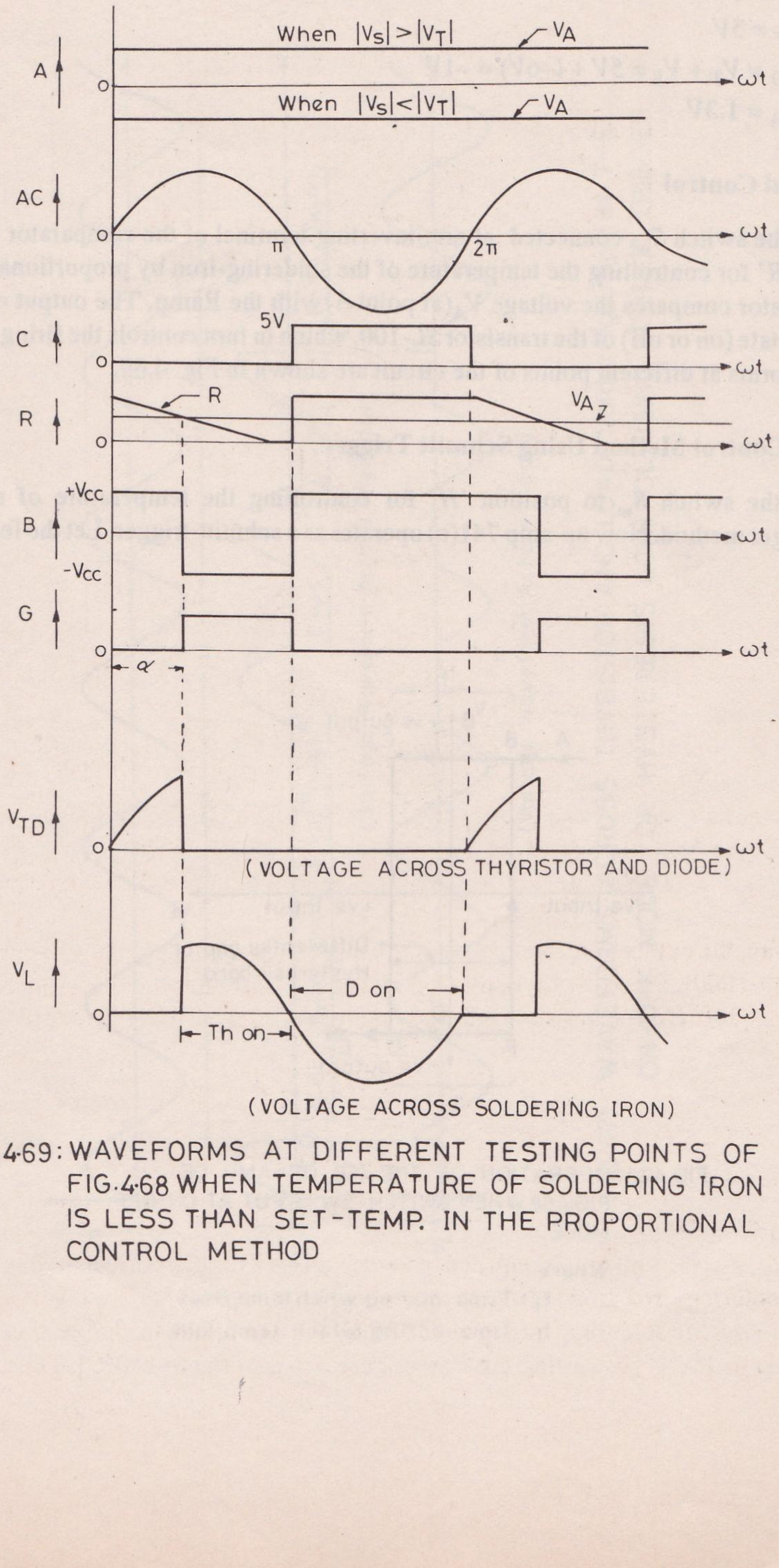


FIG.4·69: WAVEFORMS AT DIFFERENT TESTING POINTS OF FIG.4·68 WHEN TEMPERATURE OF SOLDERING IRON IS LESS THAN SET-TEMP. IN THE PROPORTIONAL CONTROL METHOD

$$V_S = -6V$$

and $V_{oi} = 40 \times 125\ \mu V = 5\ mV$

where V_{oi} → the initial voltage generated by the thermocouple corresponding to the temperature of $125^{\circ}C$.

$$\therefore V_T = 5V$$

$$\therefore V_D = V_T + V_S = 5V + (-6V) = -1V$$

or $V_A = 1.3V$

Proportional Control

Put the switch S_w, connected at non-inverting terminal of the comparator [741(c) op-amp], to position '*R*' for controlling the temperature of the soldering-iron by proportional control method. The comparator compares the voltage V_A(at point *A*) with the Ramp. The output of the comparator decides the state (on or off) of the transistor *SL*-100, which in turn controls the firing angle of thyristor (T_h). Waveforms at different points of the circuit are shown in Fig. 4.69.

Hysteresis Control Method Using Schmitt Trigger

Put the switch S_w to position '*H*' for controlling the temperature of soldering-iron by schmitt-trigger method. Now op-amp 741(c) operates as a schmitt-trigger. Let the feedback resistance

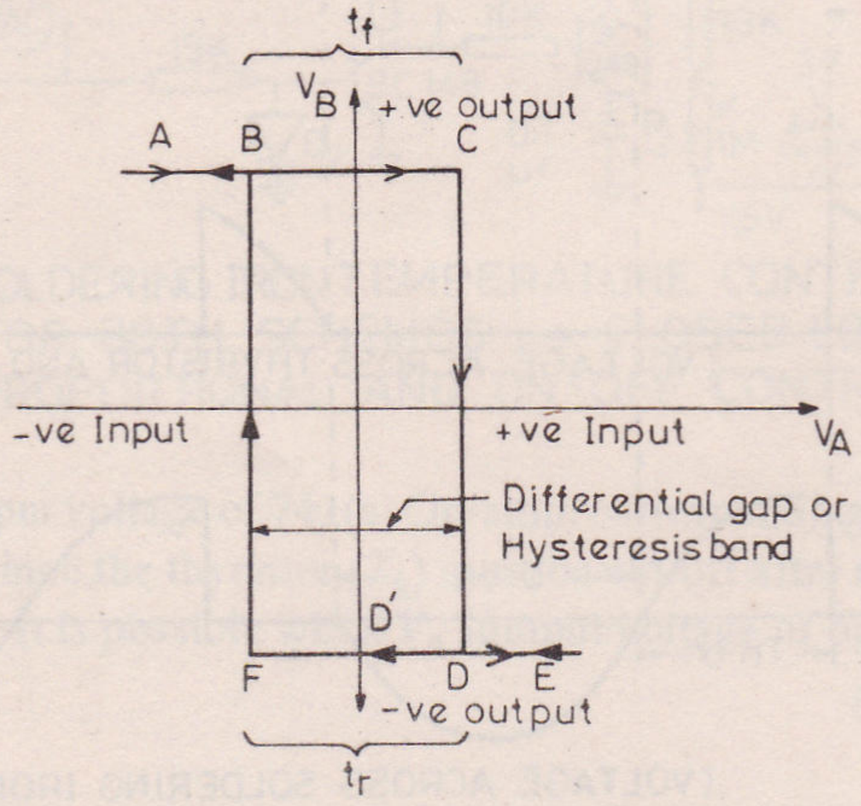


FIG. 4·70: OPERATION OF THE (C) OP-AMP. OF FIG. 4·68 WHEN SWITCH Sw IS PUT AT ON-OFF MODE

Where:

t_r: Time during which temp. rises

t_f: Time during which temp. falls

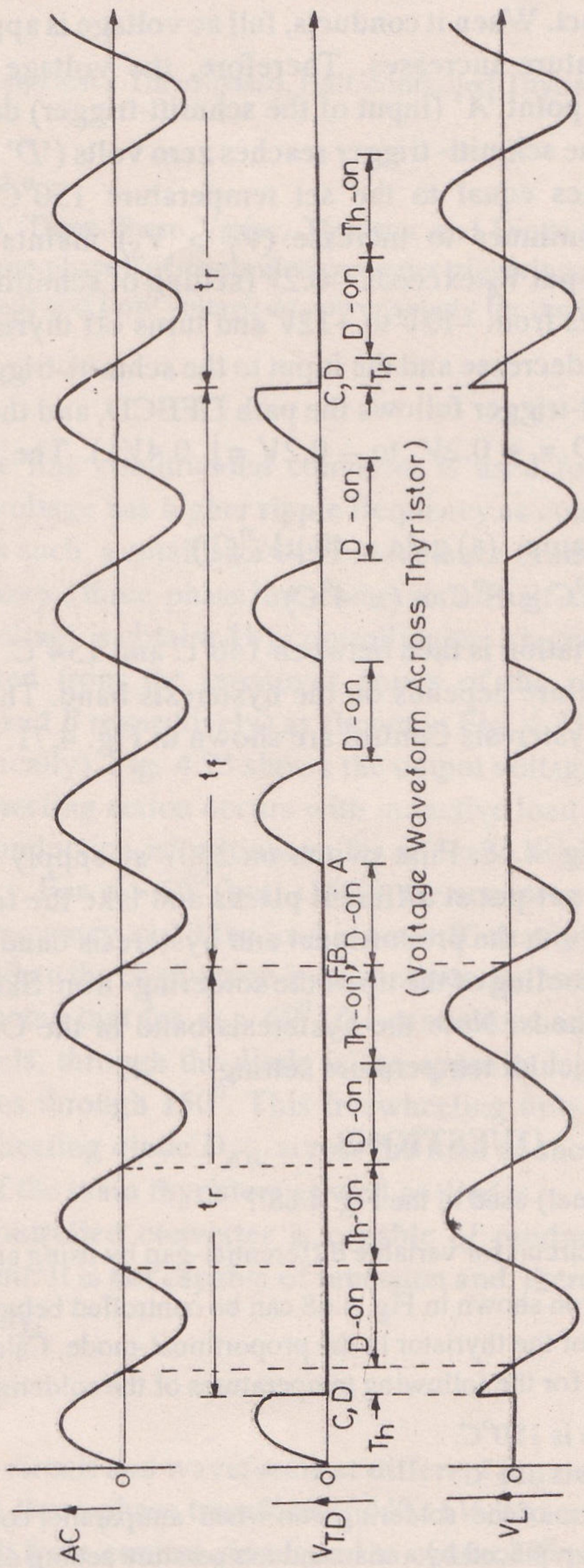


FIG.4.71 : WAVEFORMS ACROSS THYRISTOR AND LOAD (Soldering Iron) IN THE ON-OFF MODE OR HYSTERESIS CONTROL USING SCHMITT TRIGGER

(decoded by the position of pot P_3) be $60K$. Then the voltage across resistance R_s $(= 1K) = \pm \frac{1k \,.\, 12V}{61K} \simeq \pm\ 0.2V$. But the voltage at point 'A' is $+ 1.3V$. The output of Schmitt-Trigger (point B) will be $-12V$ and, hence, the voltage across R_S will be $-0.2V$.

The application of $-12V$ at point 'B' turns off the transistor SL–100. Then $+5V$ is applied to the gate of the thyristor to make it conduct. When it conducts, full ac voltage is applied to the filament of the soldering-iron and its temperature increases. Therefore, the voltage V_T also increases corresponding to V_o and the voltage at point 'A' (input of the schmitt-trigger) decreases (path EDF given in Fig. 4.70). When the input of the schmitt- trigger reaches zero volts ('D' point in Fig. 4.70), the soldering-iron temperature becomes equal to the set temperature $150^{\circ}C$ $(V_T = V_S = 6V)$. Temperature of the soldering-iron continues to increase $(V_T > V_S)$ maintaining input of the schmitt-trigger as negative. When the input V_A exceeds $-0.2V$ (setting of schmitt-trigger by P_3 pot), the output of the schmitt-trigger changes from $-12V$ to $+12V$ and turns off thyristor T_h. This causes the temperature of the soldering-iron to decrease and the input to the schmitt-trigger follows the path BC in Fig. 4.70. In this way, the schmitt-trigger follows the path DFBCD, and the hysteresis band is equal to FD or BC (in this setting $FD = + 0.2V$ to $- 0.2V = |\ 0.4V|$). The temperature of the soldering-iron varies by

$$(0.4/[\text{II op-amp. (b) gain} \times \text{I op-amp. (a) gain} \times 40\ \mu V/^{\circ}C])$$
$$= 0.4/(1.3 \times 1000 \times 40 \times 10^{-6})\ ^{\circ}C \simeq 8^{\circ}C \text{ or } (\pm\ 4^{\circ}C)$$

The consequent temperature variation is then between $146^{\circ}C$ and $154^{\circ}C$. The frequency and deviation from the steady state temperature depends on the hysteresis band. The waveform across thyristor and load (Soldering-Iron) in Hysteresis Control are shown in Fig. 4.71.

Procedure

Build the circuit according to Fig. 4.68. First switch-on $230V$ ac supply and then $\pm 12V$ and $5V$ power supplies. Set the temperature set-pot at different places and take the reading and observe the waveforms at each testing point for both the proportional and hysteresis band (ON-OFF) control methods. Wet cloth can be used for fast cooling of the tip of the soldering- iron. Sketch the waveforms at different testing points for both methods. Note the hysteresis-band in the ON-OFF mode with different settings of the pot P_3 for a particular temperature setting.

QUESTIONS

14.1 Why is a thermocouple (chromel-alumel) used in the Fig. 4.68 ?

14.2 Draw and explain "Schmitt-Trigger" circuit for variable differential-gap by using an op-amp. IC.

14.3 Let the temperature of the soldering iron shown in Fig. 4.68 can be controlled between nearly $250^{\circ}C$ and $125^{\circ}C$ by controlling the firing angle of the thyristor in the proportional-mode. Calculate the firing angles and explain the working of the circuit for the following temperatures of the soldering iron.

(i) $200^{\circ}C$ and setting temperature is $150^{\circ}C$.
(ii) $200^{\circ}C$ and setting temperature is $225^{\circ}C$.

14.4 Draw and explain the voltage waveform of the soldering iron when antiparallel connected thyristor (T_h) and Diode (D) shown in Fig. 4.68 are replaced by a triac and temperature setting of the soldering iron is $150^{\circ}C$. The temperature of the soldering iron increases by $50^{\circ}C$ when the power supply of the soldering iron is increased by $1V$ (rms).

14.5 Explain the working of the circuit shown in Fig. 4.68 for on-off control mode.

Experiment No. 15

Objective : To study and test a Three-phase, Half-controlled Thyristorized bridge Converter with its Triggering circuit.

Apparatus Required

Oscilloscope, Three-Phase Variac, Thyristor and Diode lab. module, Pulse-Transformers (3 Nos.). Shunts, Fabricated three-phase half-controlled converter triggering circuit (3–ϕ, fully-controlled converter firing circuit can also be used) and Low voltage dc power supply for the triggering circuit.

Function

Three-phase line commutated converter is used for obtaining a smooth and variable dc voltage. Its output voltage has higher ripple frequency as compared to the output voltage of a single-phase converter. As such, a small size filter inductance is adequate for filtering the output ripples.

Fig. 4.72 shows a three-phase line-commutated half-controlled thyristorised bridge converter. The controlled dc voltage is obtained by controlling the triggering angle α of thyristors. The triggering angle α is measured from the crossover points of the phase voltages (Points R_{st}, Y_{st} and B_{st} for the phases *R*, *Y* and *B* respectively) as shown in Fig. 4.73. The rectification is possible for $\alpha = 0$ to $\alpha = 150^\circ$ (theoretically). Fig. 4.73 shows the output voltage (e_L) waveform for $\alpha < 60^\circ$.

The free-wheeling action occurs with inductive load when the firing angle is more than 60°. For $\alpha < 60^\circ$, the conduction is continuous for all loads. Ripple frequency of the output is six times the supply frequency. For $\alpha > 60^\circ$ (but $<150^\circ$), the converter has output ripple frequency three times that of the supply frequency and if the load is not sufficiently inductive, the dc current waveform will be discontinuous. When the conduction is discontinuous, the thyristors and diodes conduct for $<120^\circ$.

It must be noted that for $\alpha > 60^\circ$ (for continuous as well as discontinuous conduction), the dc current freewheels, through the diode in the opposite leg of the conducting thyristor, when the phase voltage passes through 150°. This freewheeling duty of main devices can be eliminated by connecting a freewheeling diode D_{FW} across the load as shown in Fig. 4.72. This helps in reducing the current rating of the main thyristors as well as diodes.

This half-controlled converter is capable of producing only positive output voltage and unidirectional current. It is not capable of inversion and, therefore, it is used for speed control of low power dc motors only.

Control-Circuit

The control circuit and waveforms at different important points are shown in Figs. 4.74 and 4.75 respectively. A three-phase transformer 440 : 6*V* connected in Delta-Star (Δ–*Y*), is employed to isolate power circuit from control circuit and to obtain 30° phase shifted signal voltages *R*, *Y* and *B* from phase *R*, *Y* and *B* respectively. If three-phase Delta-Star (Δ–*Y*) transformer is not available, three single-phase transformers (220*V* : 6*V*) can be used. Three single-phase transformers are connected as three-phase Delta Star (Δ–*Y*) configuration as shown in Fig. 4.79.

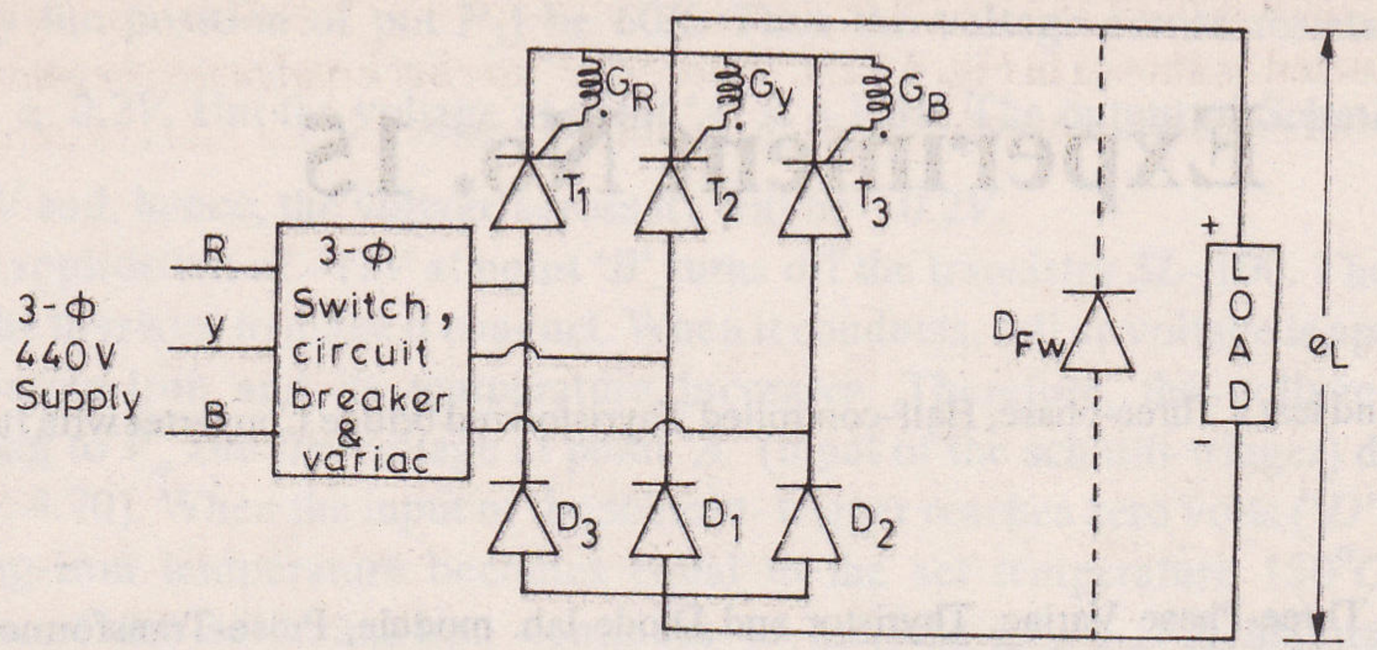


FIG.4.72 : THREE-PHASE HALF CONTROLLED BRIDGE CONVERTER

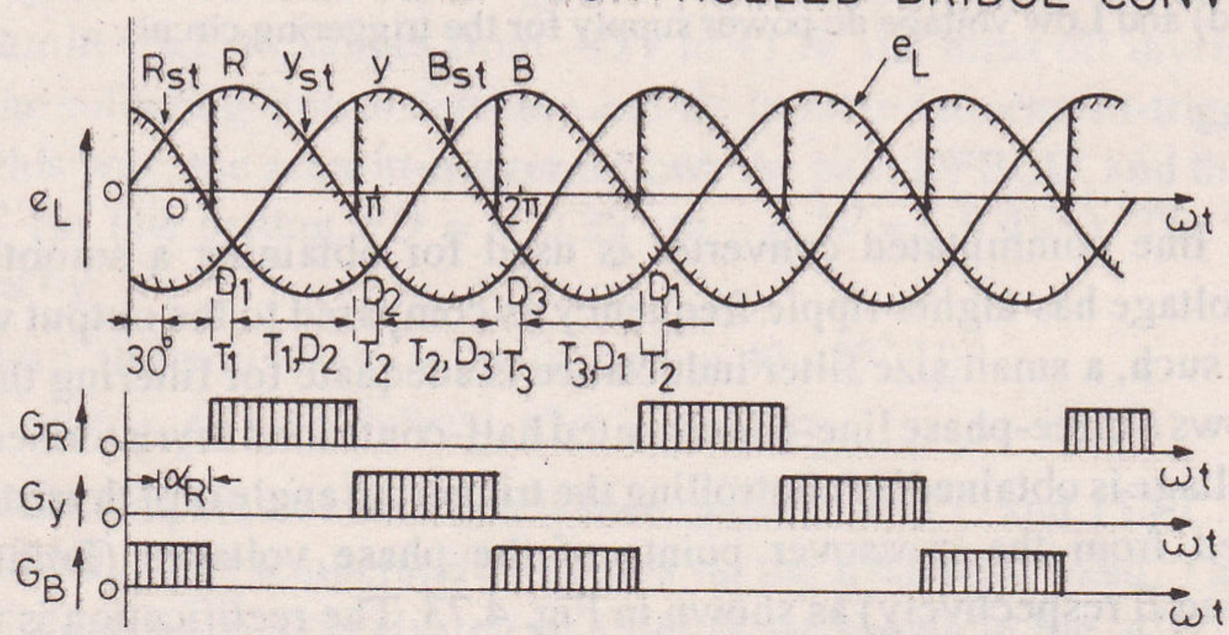


FIG.4.73 : FIRING PULSES AND LOAD-VOLTAGE

The three separate but identical cards (*R*-card, *Y*-card and *B*-card) are used for controlling the triggering angles of thyristor T_1, T_2 and T_3 respectively. These cards function as follows:

The phase-shifters (*R-C* circuits) shift phase signal voltages *R'*, *Y'* and *B'* in reverse direction (to right-side). Adjust the preset 100*K* Pots of the phase-shifters for shifting the synchronized signal voltages *R'*, *Y'* and *B*, by 60°. The output waves R_o, Y_o and B_o of the phase-shifters are used as synchronised signal voltages for *R*, *Y* and *B* phases respectively.

The zero crossover detector generates square wave pulses (R_1, Y_1 and B_1). The triangular waveforms (R_2, Y_2, and B_2) are obtained at the output of the Integrators. The comparators compare the triangular waveforms (R_2, Y_2, and B_2) with a dc voltage V_c which varies between $+V_{cc}$ to $-V_{cc}$ and is controlled by the 47*K* Pot (*P*). The outputs of the comparators (R_3, Y_3 and B_3) form inputs to the pulse generators (monostable). The monostable outputs (waveforms R_4, Y_4 and B_4) are used as clock and clear pulses for *J-K* Flip-Flops F/F_1, F/F_2 and F/F_3 as shown in the Fig. 4.74. Outputs of the *J-K* flip-flops (R_5, Y_5 and B_5) are the required 120° conduction pulses for the thyristors.

These waveforms (R_5, Y_5 and B_5) are ANDed with a high frequency carrier signal ($\simeq 10KHz$) to produce the triggering signals αR, αY and αB. The high frequency switching is essential to reduce gate power dissipation and size of pulse transformers.

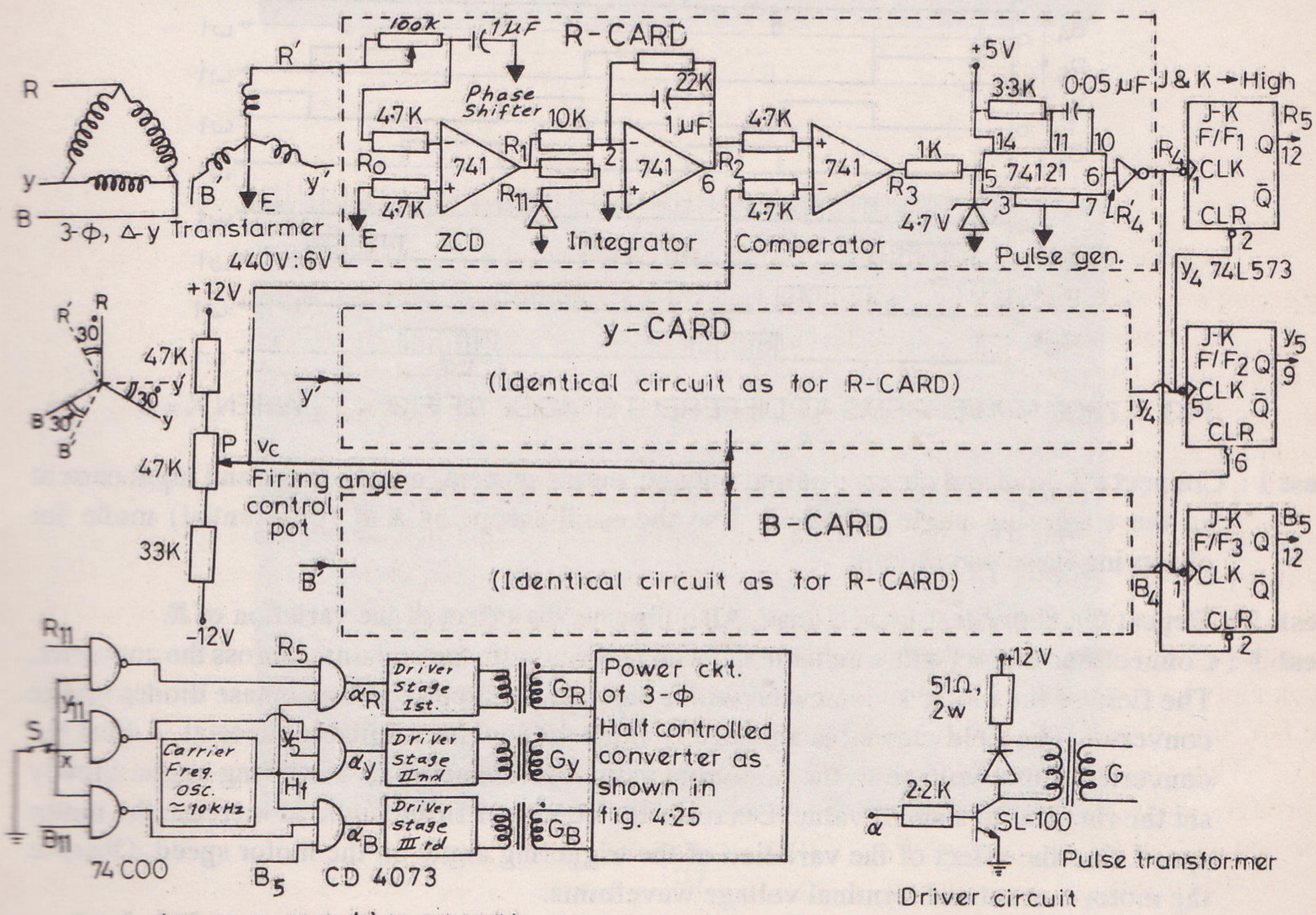
When switch '*S*' is closed ($x = 0$), the pulse widths α_R, α_Y and α_B are almost same as waveforms R_5, Y_5 and B_5 respectively. And when switch '*S*' is open ($x = 1$), the pulse widths α_R, α_Y and α_B are almost same as waveforms R_5, Y_5 and B_5 if $\alpha < 60^o$ otherwise almost equal to $\pi-\alpha$. These modulated pulse signals α_R, α_Y and α_B are applied to thyristors T_1, T_2 and T_3 respectively, through pulse transformers.

The control circuit is built and tested to give the appropriate gate pulses G_R, G_Y and G_B. The power circuit is completed as shown in Fig. 4.72. *It is necessary to check and mark the phase-sequence of the power supply and connect properly the phases with the power circuit and the control circuit.*

Test Procedure

Make control circuit as shown in Fig. 4.74. Check whether the firing circuit is working properly or not for all three phases. If it is working as expected, check the polarity and phase of the output pulses G_R, G_Y or G_B of the control circuit. Use proper thyristors and diodes and make the three-phase Half-Controlled Bridge Converter power circuit as shown in Fig. 4.72. See that the incoming power supply (*R*, *Y* and *B*) is properly connected to the bridge and the control circuit so that proper phase sequence is maintained. For safety of the power circuit, it is routed through a properly rated ICTP switch and breaker. Again check the triggering pulses G_R, G_Y and G_B for the thyristor of *R*, *Y* and *B* phases respectively before breaker is switched 'ON'. The triggering pulses G_R, G_Y and G_B are delivered to the gate of thyristors T_1, T_2 and T_3. Note the synchronisation w.r.t. the supply.

After completing the above procedure, connect required load and release the three-phase power supply (breaker to be switched 'ON') and firing pulses to thyristors T_1, T_2 and T_3. The circuit will be ready for operation as a three phase half-controlled converter. Conduct the following tests :



X = 0 (When switch 's' is closed)
X = 1 (When » 's' is open)

FIG.4·74 : FIRING CIRCUIT DIAGRAM FOR THREE PHASE HALF CONTROLLED CONVERTER

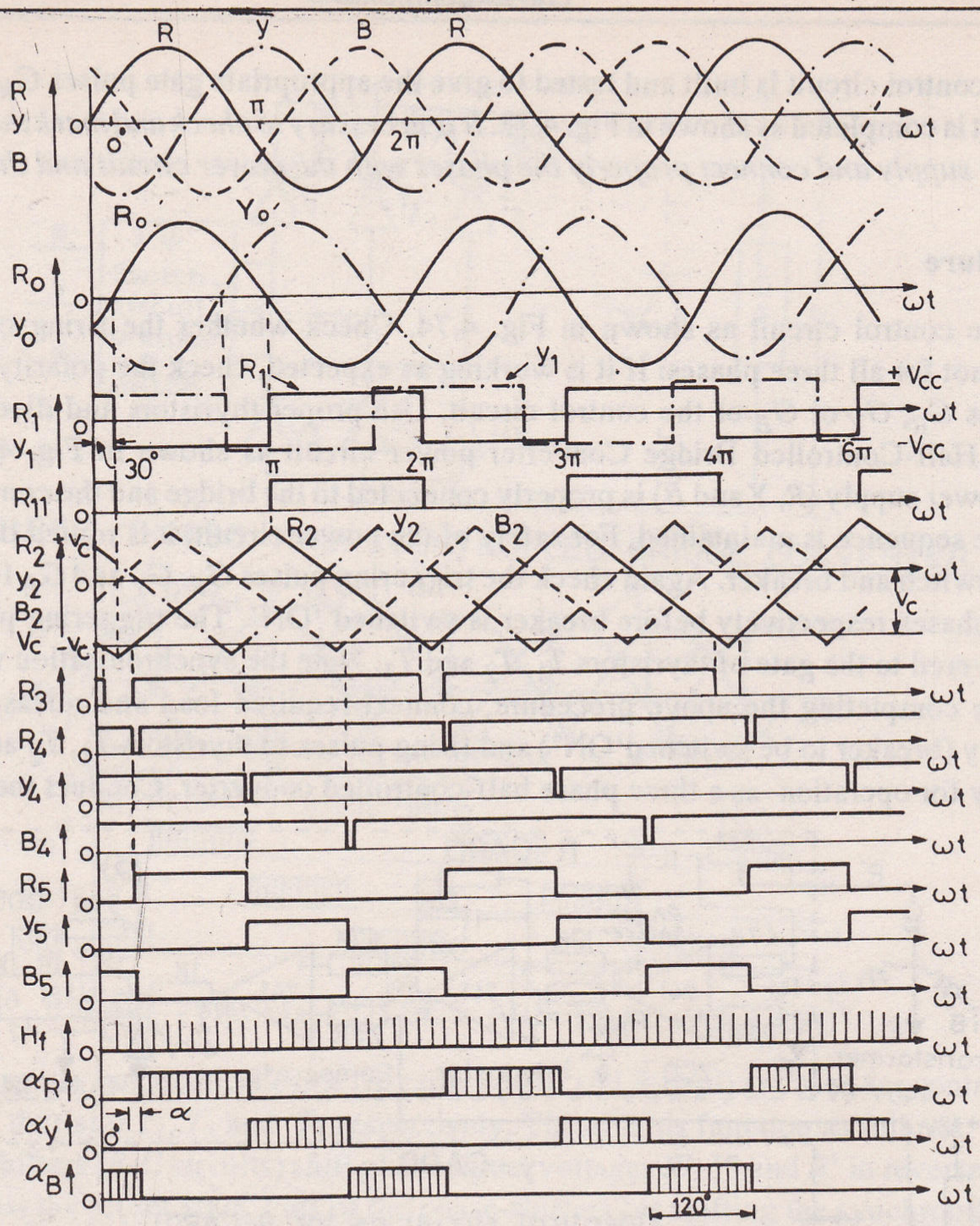


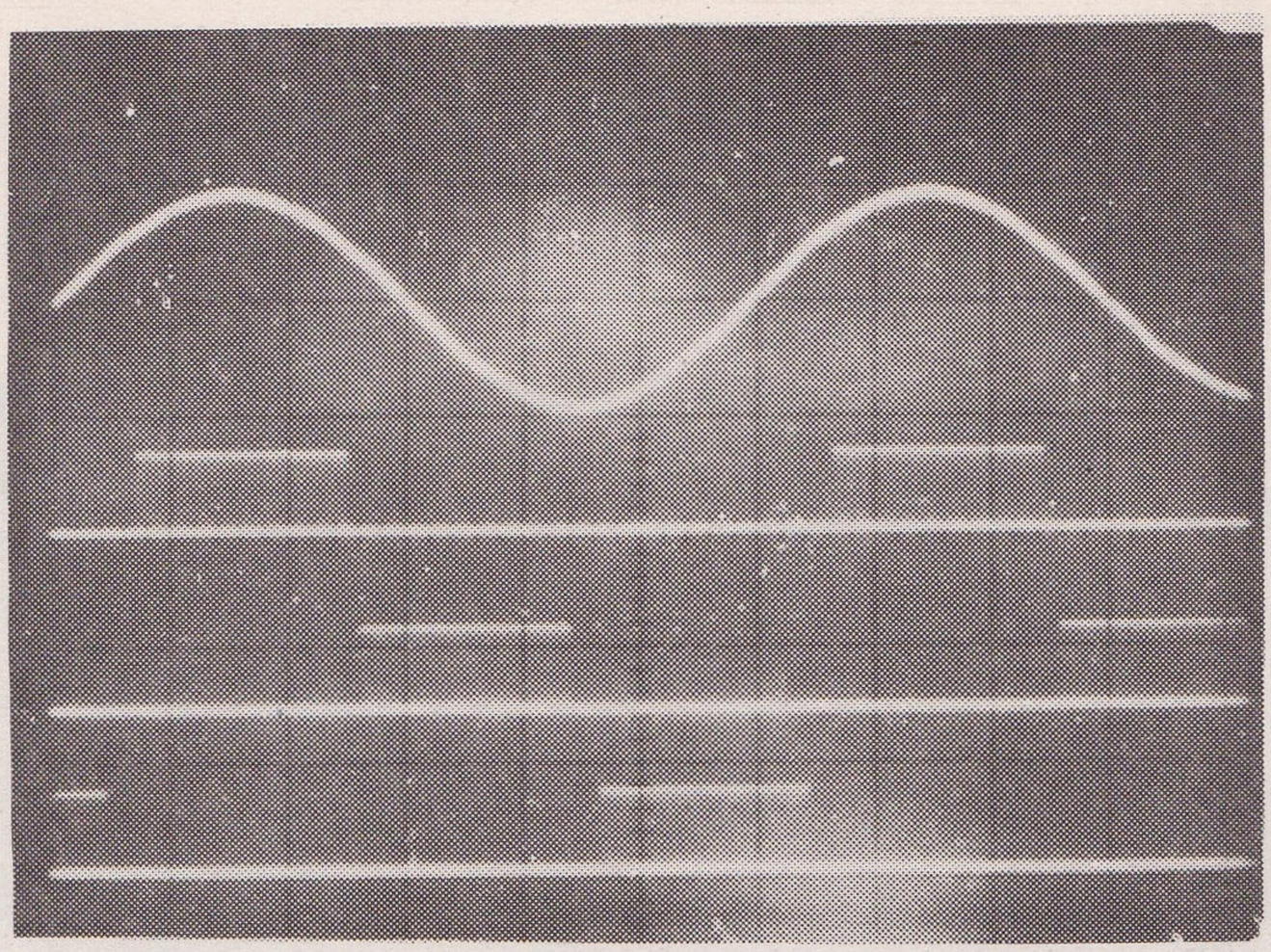
FIG. 4.75(a): WAVEFORMS AT DIFFERENT STAGES OF FIG. 4.75 WHEN X = o

Test 1 : Connect a *R*-load and observe output voltage, output current, input voltage and input current as the triggering angle is varied. Use the oscilloscope in *A-B* (differential) mode for observing these waveforms.

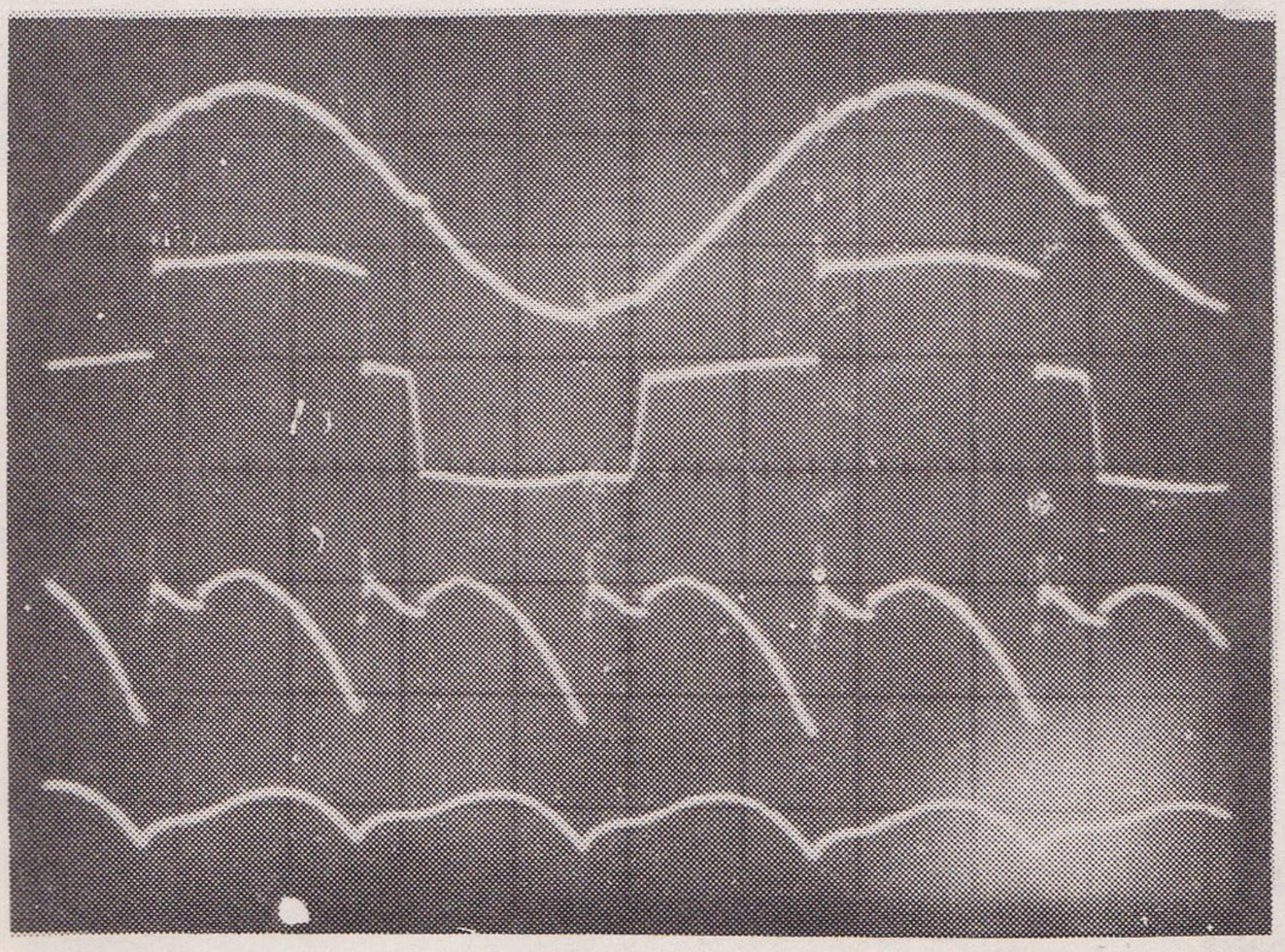
Test 2 : Repeat the above test for *R-L* load. Also observe the effect of the variation of *R*.

Test 3 : Connect a dc motor (with a suitable rheostat in series with the armature) across the converter. The field of the motor is connected with a separate dc supply or three-phase diodes bridge converter. The field current is adjusted to rated value with a suitable rheostat. Adjust the converter output voltage to the minimum value by advancing its triggering angle. Slowly set the rheostat to a small value. Decrease the converter firing angle to increase the motor speed. See the effect of the variation of the triggering angle on the motor speed. Observe the motor current and terminal voltage waveforms.

The oscilloscope traces of Fig. 4.75(b) and Fig. 4.75(c) show the triggering pulses w.r.t. V_{RB} (input voltage between phases *R* and *B*), *R*-phase input current, load voltage, load current and thyristor T_1 voltage for triggering angles (α) appropriate 45° and 100° respectively.

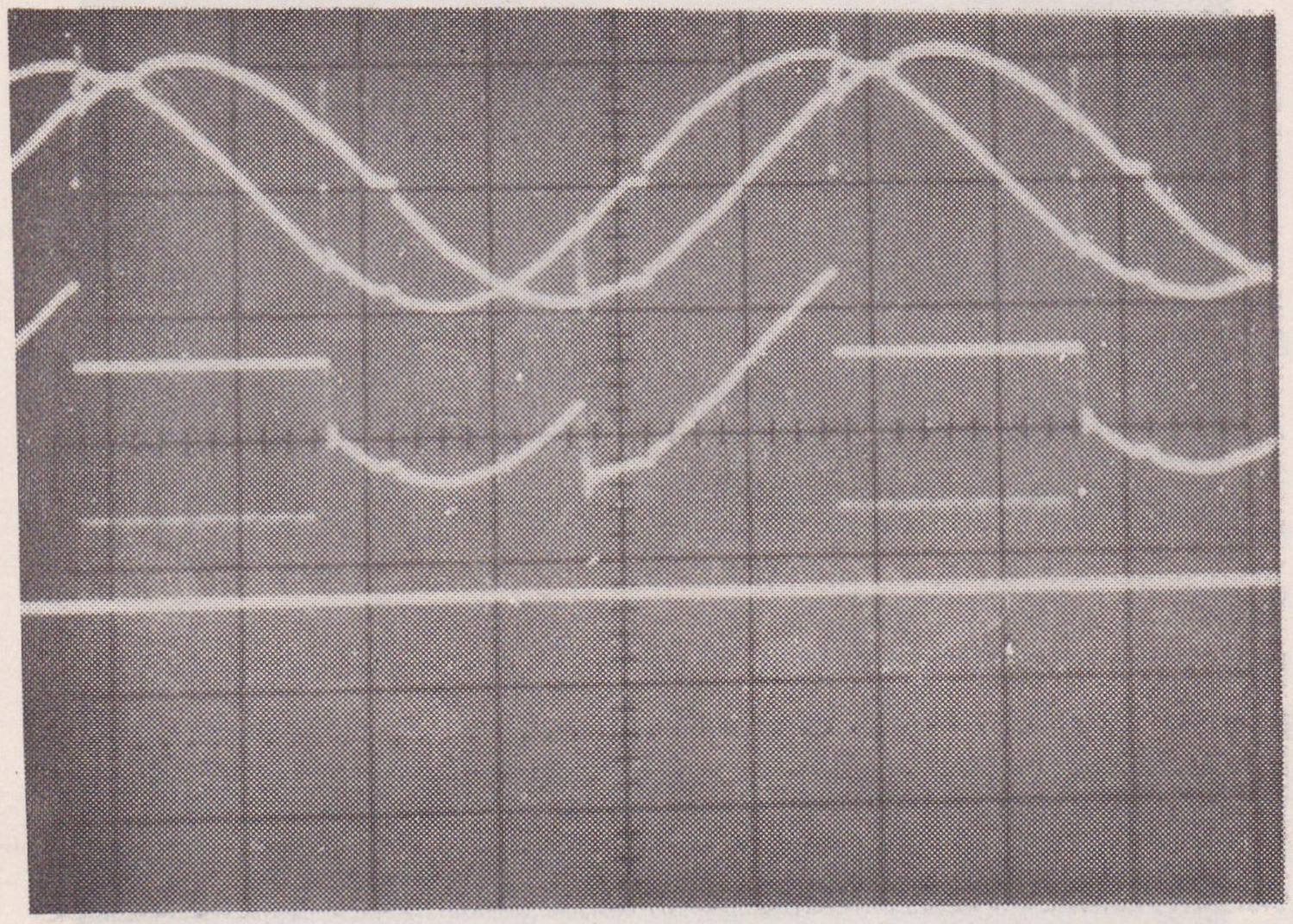


(i)



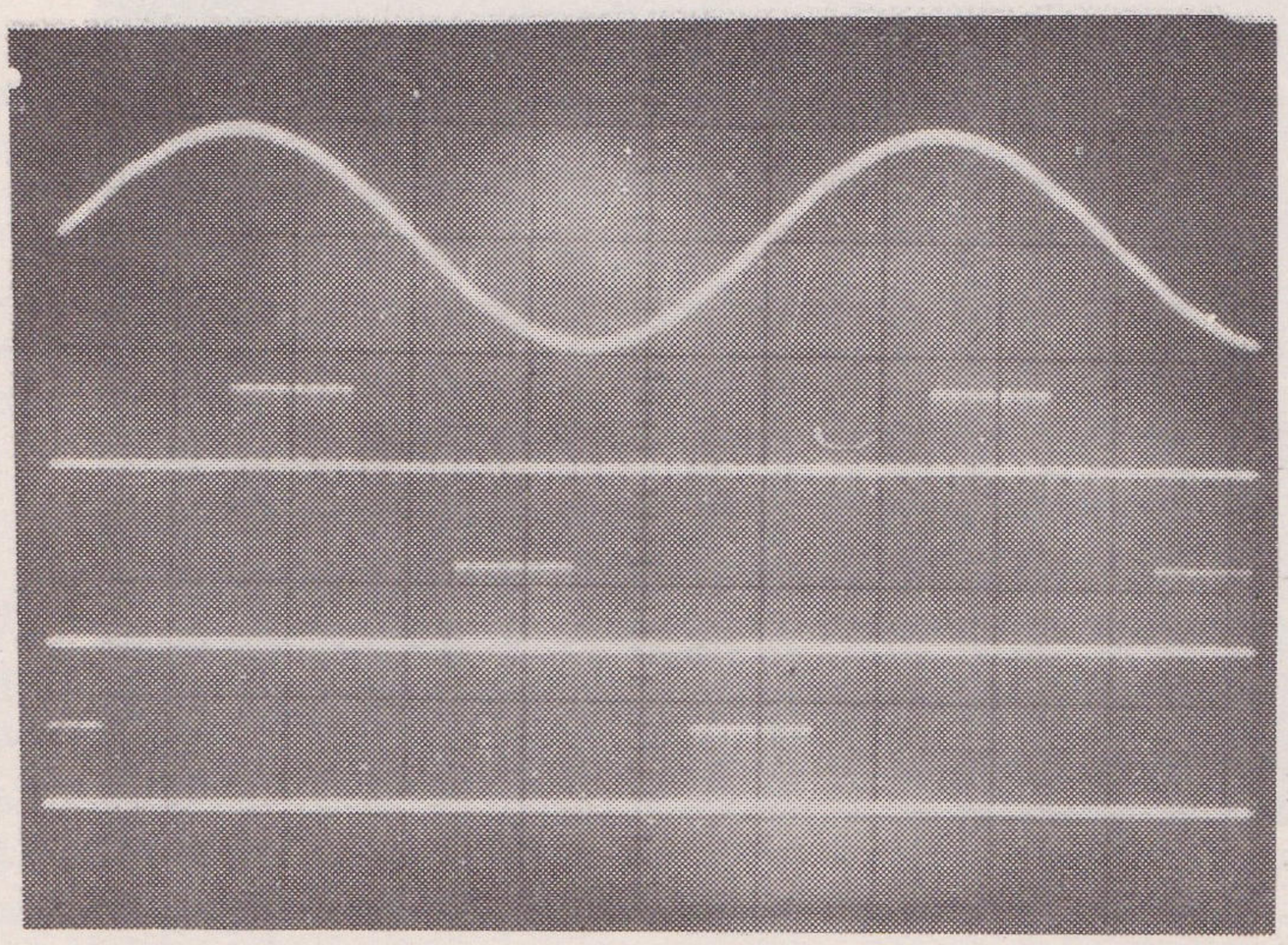
(ii)

FIG. 4.75(b) (CONT.)

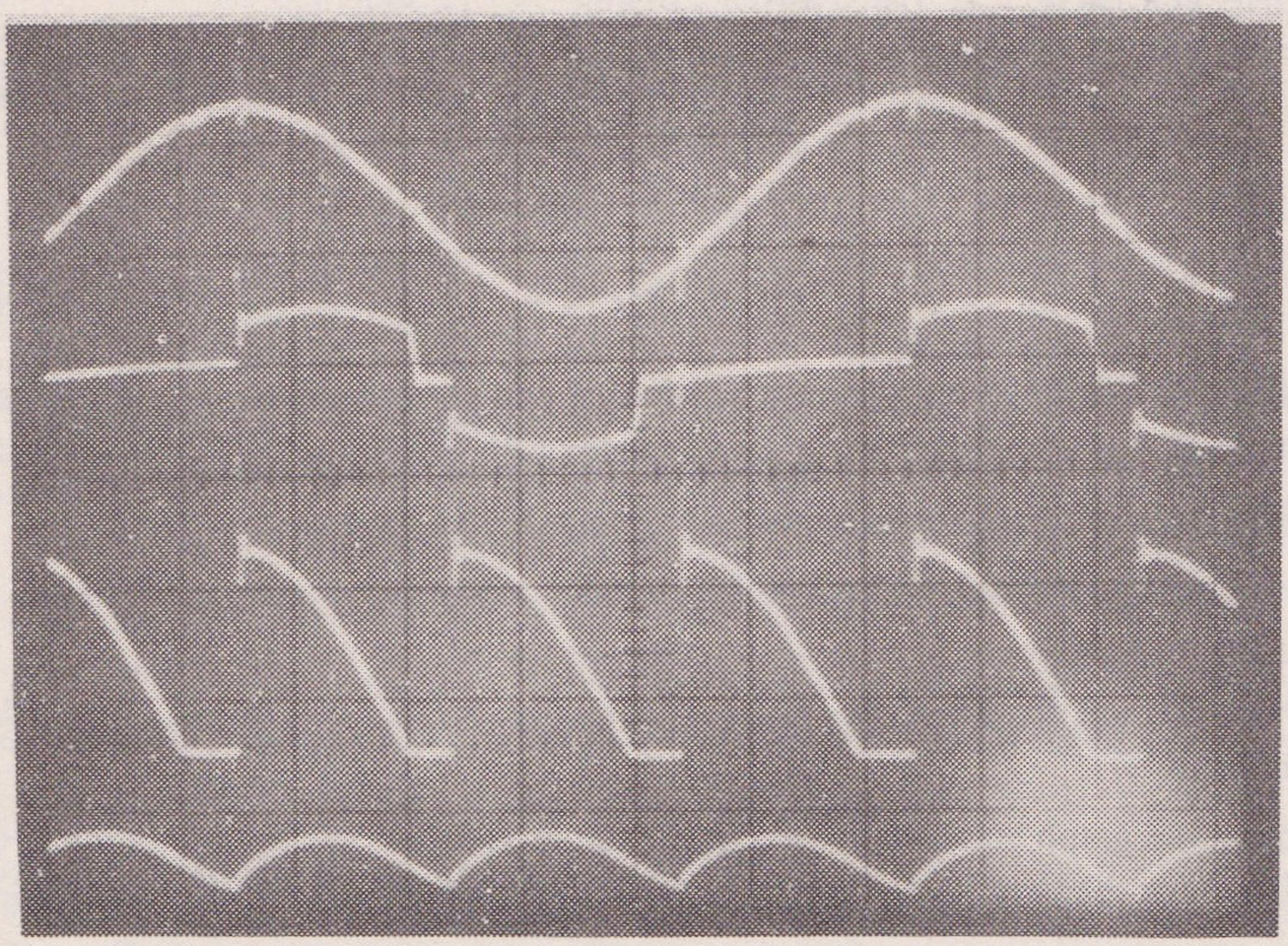


(iii)

FIG. 4.75(b) : OSCILLOGRAMS OF THREE-PHASE HALF-CONTROLLED CONVERTER WITH R-L LOAD (R = 50 Ω AND L = 240 mH) FOR α (FIRING ANGLE) ≃ 45°
(i) LINE VOLTAGE V_{RB}, TRIGGERING PULSE G_R, G_Y AND G_B
(ii) LINE VOLTAGE V_{RB}, *R*-PHASE INPUT CURRENT, LOAD VOLTAGE AND LOAD CURRENT
(iii) LINE VOLTAGES V_{RB} AND V_{RY}, THYRISTOR T_1 VOLTAGE AND TRIGGERING PULSE G_R

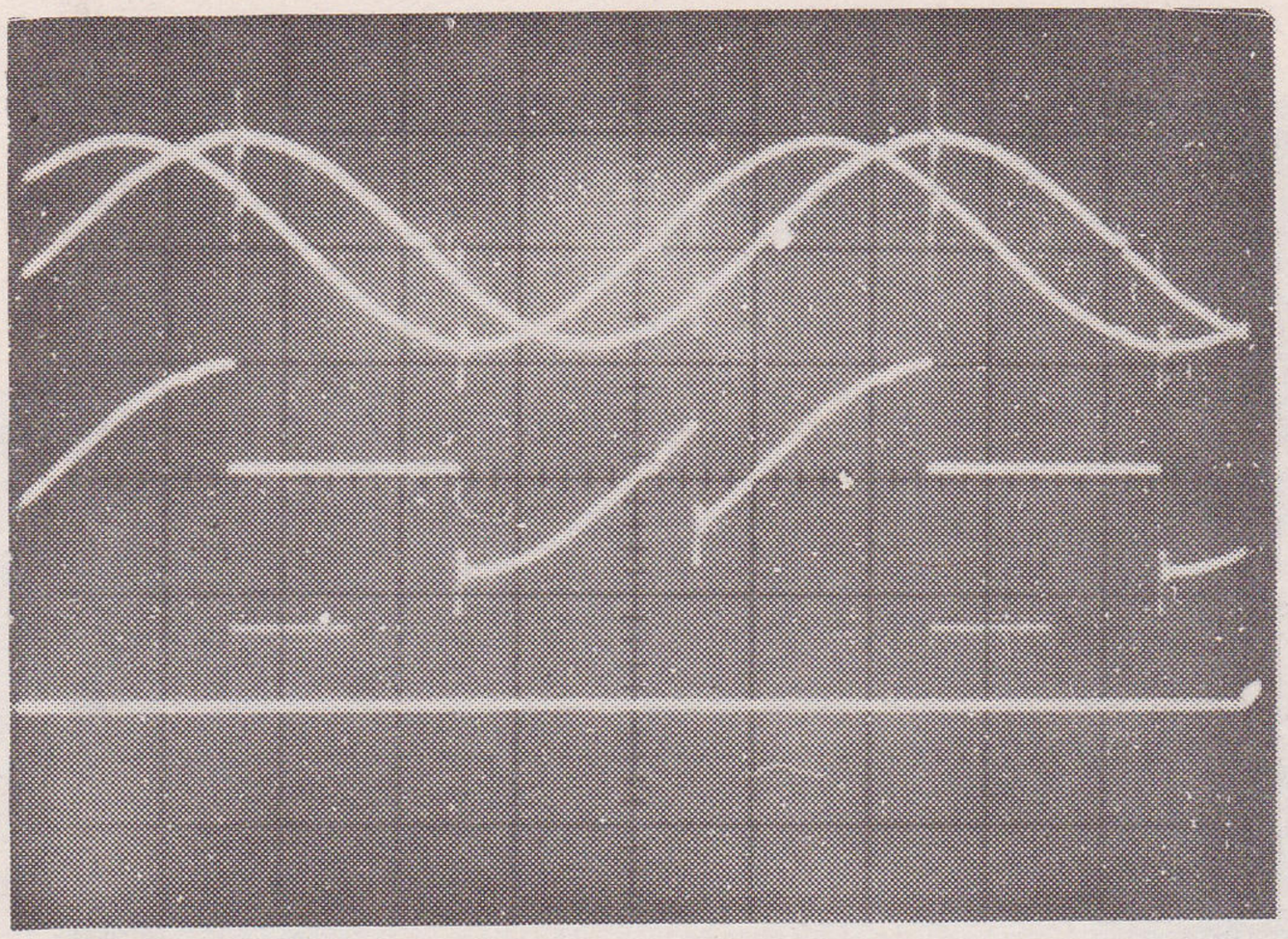


(i)



(ii)

FIG. 4.75(C) (CONTD.)



(iii)

FIG. 4.75(c) : OSCILLOGRAMS FOR THREE-PHASE HALF-CONTROLLED CONVERTER WITH R-L LOAD (R = 50 Ω AND L = 240 mH) FOR α (FIRING ANGLE) ≃ 85°
(i) LINE VOLTAGE V_{RB}, TRIGGERING PULSE G_R, G_Y AND G_B
(ii) LINE VOLTAGE V_{RB}, *R*-PHASE INPUT CURRENT, LOAD VOLTAGE AND LOAD CURRENT
(iii) LINE VOLTAGES V_{RB} AND V_{RY}, THYRISTOR T_1 VOLTAGE AND TRIGGERING PULSE G_R

QUESTIONS

15.1 Draw the 3–ϕ supply's voltage waveform w.r.t. neutral and show the *R*-load voltage for *Y*-phase only and *R-L* load voltage for *R*-phase only for triggering angle of 45° for a 3–ϕ half-controlled converter.

15.2 Why is a smaller filter required for 3–ϕ converter compared to the 1–ϕ coverter ?

15.3 Show the free-wheeling duration in the *B*-phase only for triggering angle of 75° in the 3–ϕ half-controlled converter.

15.4 Write the advantages and disadvantages of the 3–ϕ half-controlled converter compared to the 3–ϕ fully-controlled converter.

15.5 Draw and explain the graph between the triggering angle and the load voltage in the 3–ϕ half-controlled converter. Also show the load voltages at triggering angle 0°, 54°, 66°, 90° and 150° when phase to phase voltage of the input supply is 100 volts (rms).

[Hint : load voltage = $\frac{3\sqrt{6}}{2\pi}\, e\ (1+\cos\alpha)$

where *e* : supply phase voltage in rms]

Experiment No. 16

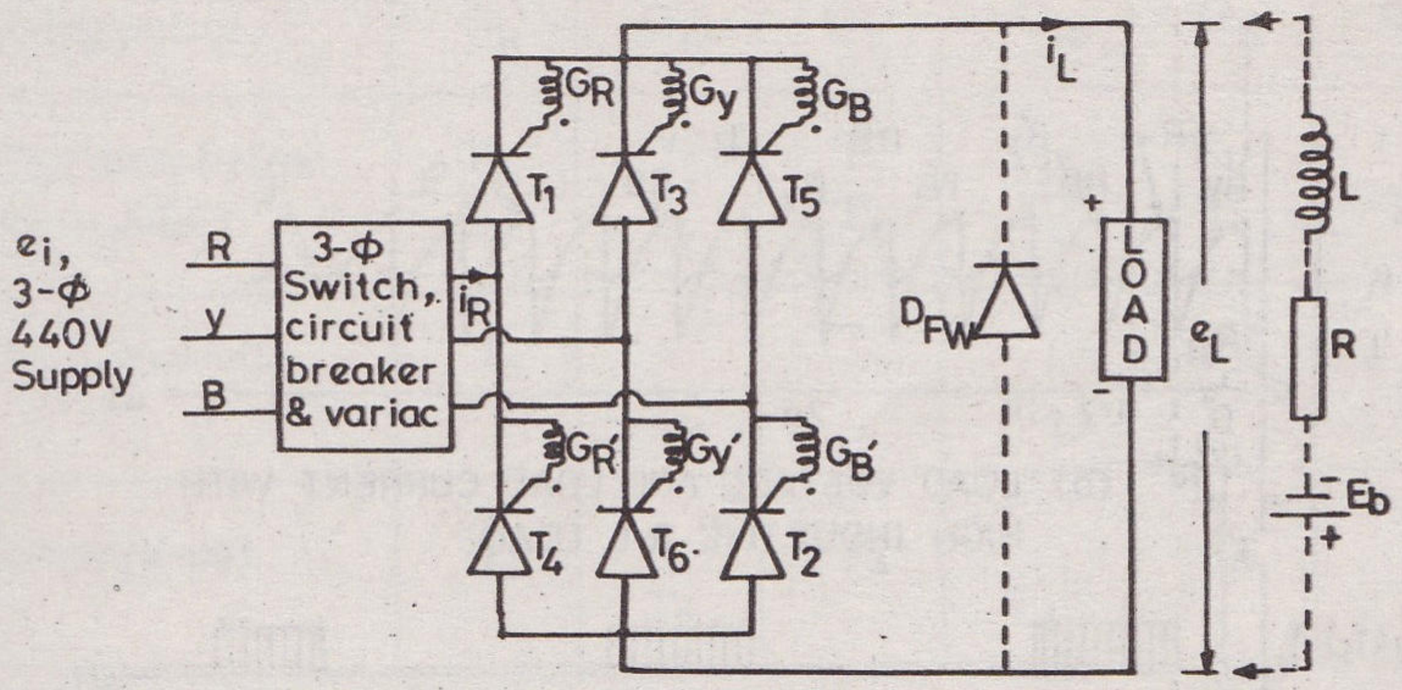
Objective : To study and test a Three-phase Fully-controlled Thyristor Bridge Converter with its Triggering Circuits.

Apparatus Required

Oscilloscope, Three-phase Variac, Thyristor and Diode lab. module, Pulse-Transformers (6 Nos.), Shunts, Fabricated three-phase fully-controlled converter triggering circuit and low voltage dc power supply for the triggering circuit.

Function

Generally, the three-phase line commutated bridge converters are used where both conversion and inversion operations are required, i.e., in HVDC power supply system, dc motor speed control with regenerative braking, battery chargers, as front-end converters in choppers, inverters and cycloconverters. Upto about 10 kilowatts power ratings, the single-phase converters are used and for more than about 10 KW power ratings, the 3–ϕ converters are used. These converters are also called two-quadrant six-pulse bridge converters (B-6) because the output voltage of the 3–ϕ fully-controlled converter has six pulses during one cycle duration of the input supply these types of converters generate sixth order of the lowest harmonic in the output power and generate harmonics of the order $6\pi+1$; where π = 1, 2, 3, 4,... in the input power supply current. The amplitudes of the harmonics decrease with an increase in the order of harmonic.



FIG·4·76(a):THREE-PHASE FULLY-CONTROLLED BRIDGE CONVERTER

Fig. 4.76(a) shows a three-phase line-commutated fully-controlled thyristorised bridge converter. The controlled dc voltage is obtained by controlling the triggering angle α of thyristors. The triggering angle α is measured from the crossover points of the phase voltages as shown R_{st}, Y_{st} and B_{st} points in Fig. 4.77(a). The average dc output voltage E_L is given by equation :

$$E_L = \frac{3\sqrt{2}}{\pi} e_i \text{ Cos } \alpha \simeq 1.35\, e_i \text{ Cos } \alpha$$

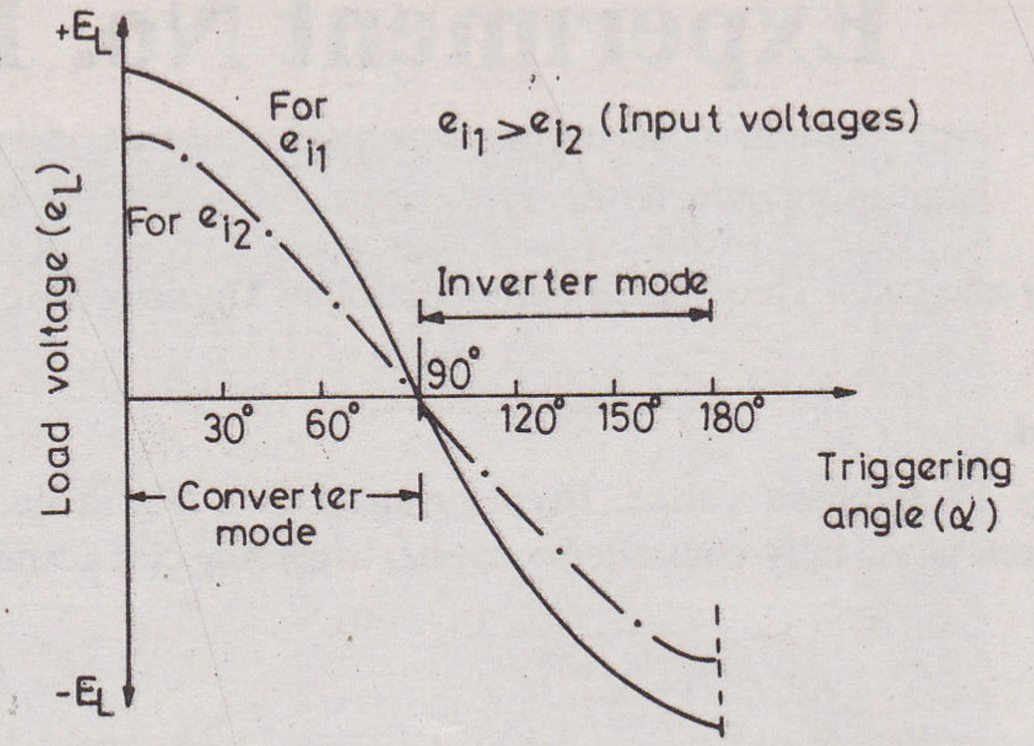


FIG.4.76(b): VARIATION IN LOAD VOLTAGE WITH THE VARIATION OF TRIGGERING ANGLE

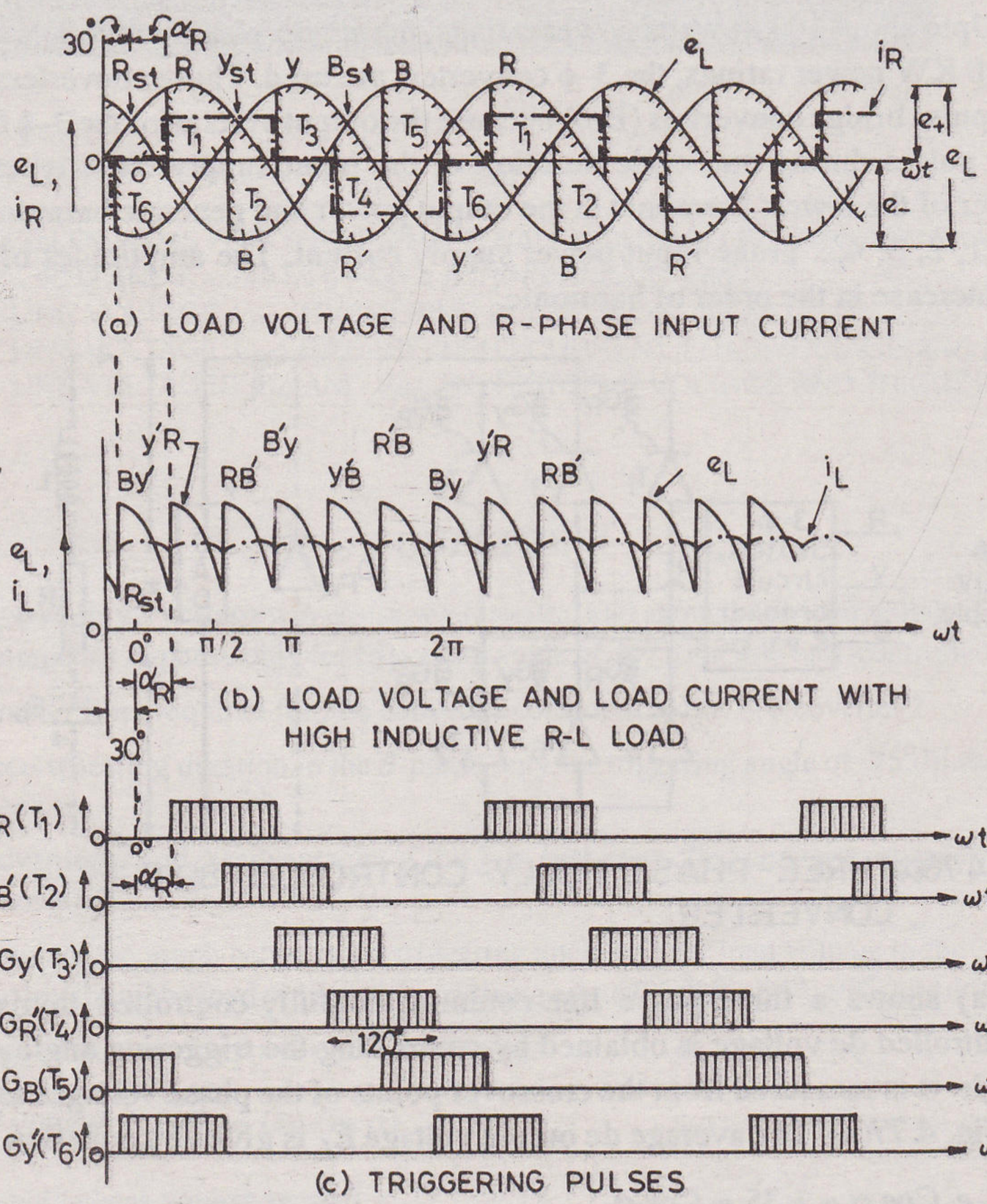


FIG.4.77: LOAD VOLTAGE, LOAD CURRENT AND TRIGGERING PULSES

where, e_i : Phase to phase voltage of the input power supply in rms.

If the triggering angle α is greater than 90^o then the output voltage E_L will be negative. So if a dc power supply with opposite polarity (shown by dotted line in Fig. 4.76(a) is connected at the output side, then it will supply power to the output circuit and the 3–ϕ ac power system. This operation is called inversion. The variation in the output voltage E_L with the variation of the triggering angle is shown in Fig. 4.76(b). Fig. 4.77 shows *R*-phase input current, load voltage, load current and triggering pulses. And Fig. 4.78 shows oscillograms for waveforms at different stages of the Fig. 4.76(a) for *R-L* load.

In Fig. 4.76(a), thyristors T_1, T_3 and T_5 are called positive group thyristors because they are turned-on when the respective phase voltages are positive. Similarly, thyristors T_2, T_4 and T_6 are called negative group thyristors. The changeover of conduction from one thyristor to other thyristor in the positive group (T_1, T_3 and T_5) will take place only, if the phase voltage of the thyristor to be turned on is more positive than that of the thyristor to be turned off. Similarly, the changeover of conduction from one thyristor to other thyristor in the negative group thyristors (T_2, T_4 and T_6) will take place only if the phase voltage of the thyristor to be turned-on is more negative than that of thyristor to be turned off. The thyristors T_1, T_2, T_3, T_4, T_5,T_6,T_1, T_2 ... are turned-on in sequence of their numbers with a phase difference of 60^o. It can be noted that the negative group thyristors T_4,T_6 and T_2 are turned-on in a sequence after 180^o from the positive group thyristors T_1, T_3 and T_5 respectively. With a high inductive load, each thyristor conducts for 120^o ($2\pi/3$). So the positive and negative current flow for 120^o in each phase of the input power supply. Table 16.1 shows conduction sequence of the thyristors.

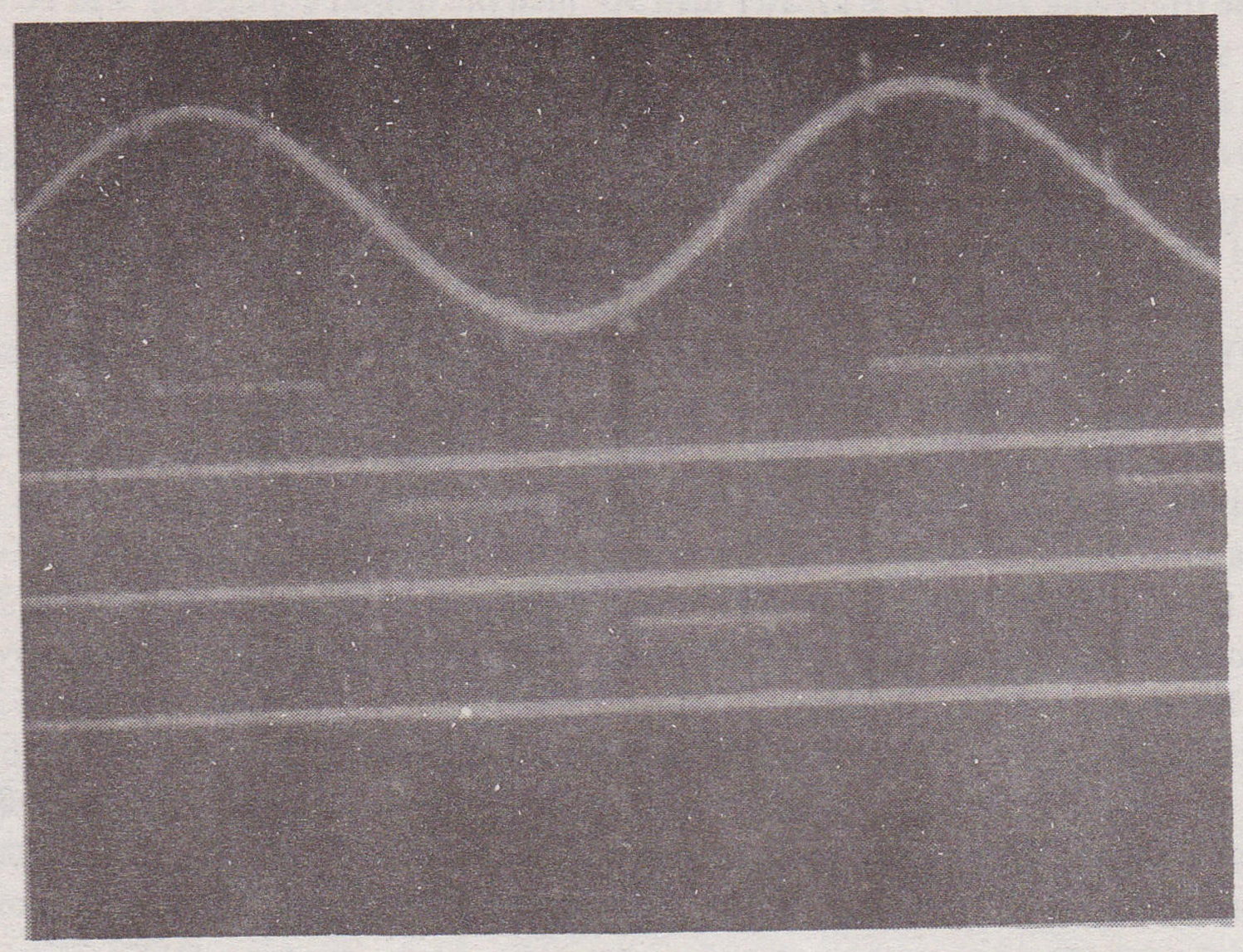
Table 16.1

Triggering Sequence of Thyristors in Fig. 4.76(a)

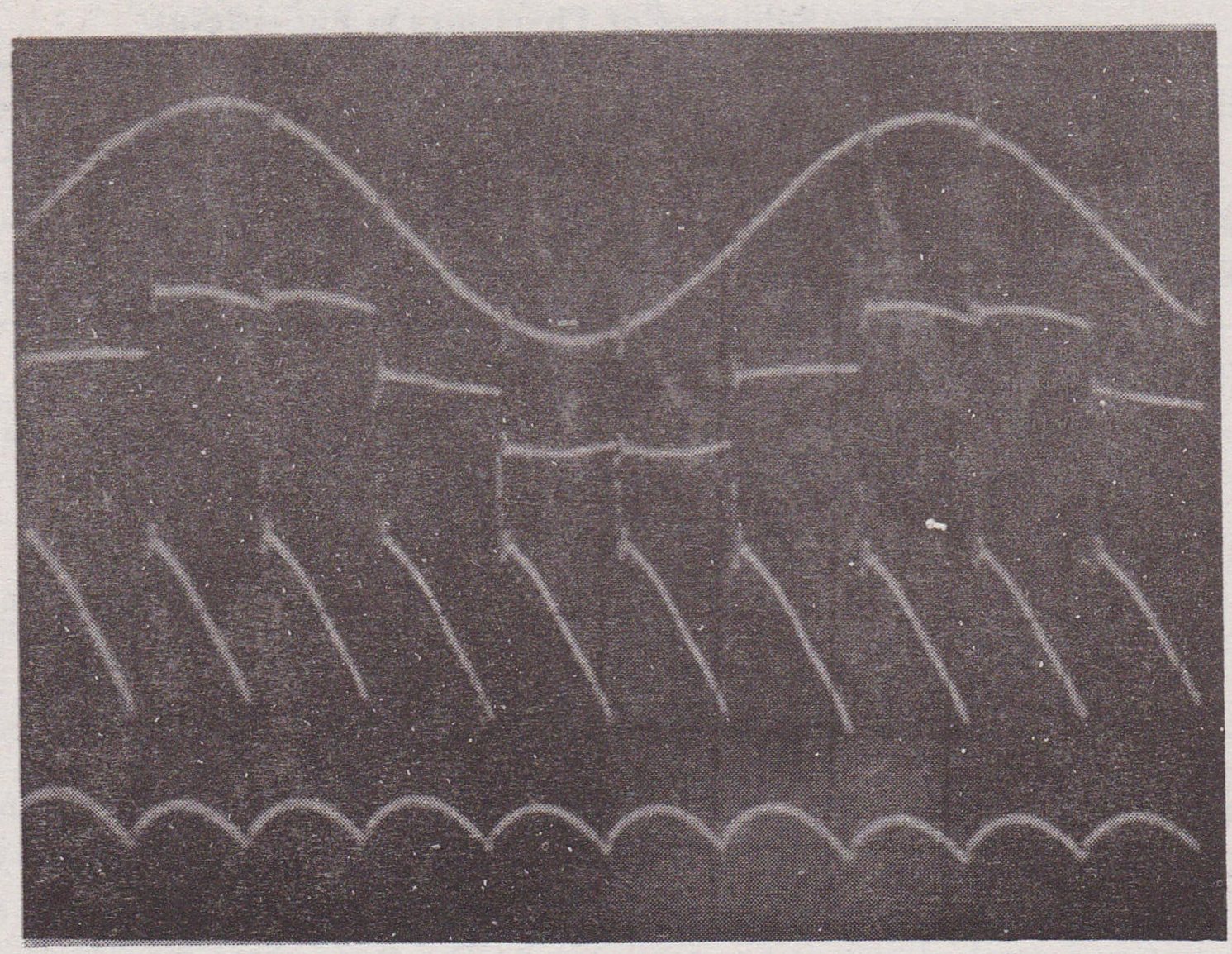
Coming triggering pulses	G_R	G_B,	G_Y	G_R,	G_B	G_Y,	G_R
Conducting Thyristors before coming triggering pulses	T_5, T_6	T_1, T_6	T_1, T_2	T_3, T_2	T_3, T_4	T_5, T_4	T_5 T_6
Outgoing (to be turned-off) Thyristor	T_5	T_6	T_1	T_2	T_3	T_4	T_5
Coming (to be turned-on) Thyristor	T_1	T_2	T_3	T_4	T_5	T_6	T_1

16.1 CONTROL-CIRCUIT WITH ISOSCELES-COMPARATOR APPROACH

The control circuit and waveforms at different important points are shown in Figs. 4.79 and 4.80 respectively. A three-phase transformer $440V : 6V$ connected in Delta-Star (Δ–Y), is employed for obtaining synchronised control triggering pulses from the control circuit, And it also provides isolation between control circuit and power circuit. The three-phase transformer connected in Delta-Star will shift secondary phase signal voltages R_o, Y_o and B_o by 30^o in the forward direction (left side) from *R*, *Y* and *B* phases respectively. So the phase signal voltages R_o, Y_o and B_o with respect to neutral are shifted total 60^o from the reference points R_{st}, Y_{st} and B_{st} (Fig. 4.77). If three-phase

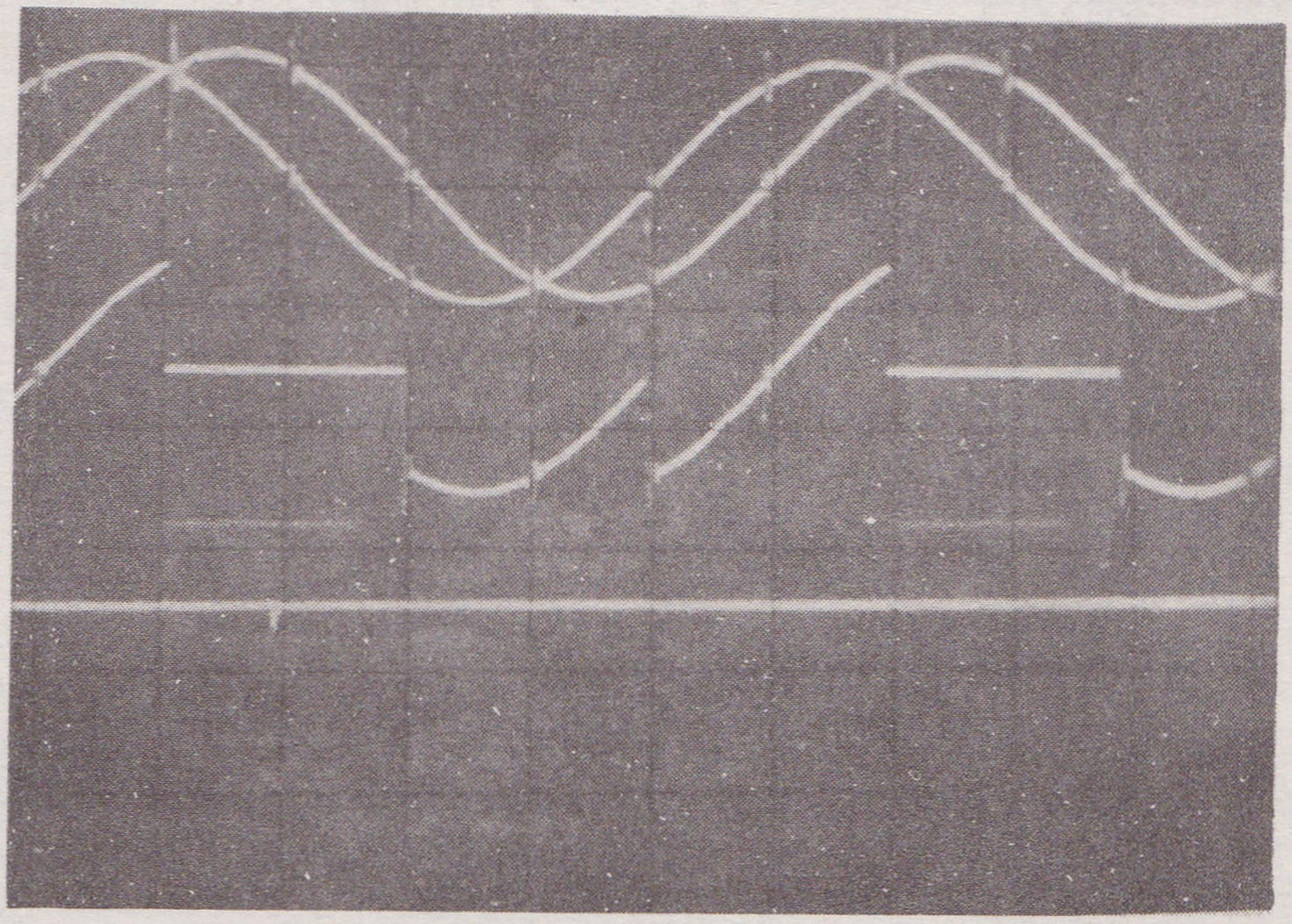


(i)



(ii)

FIG. 4.78 (CONTD.)



(iii)

FIG. 4.78 : OSCILLOGRAMS FOR THREE-PHASE FULLY-CONTROLLED CONVERTER WITH R-L LOAD (R = 50 Ω AND L = 240 mH) FOR α (FIRING ANGLE) ≃ 60°
(i) LINE VOLTAGE V_{RB}, TRIGGERING PULSE G_R, G_Y AND G_B
(ii) LINE VOLTAGE V_{RB}, *R*-PHASE INPUT CURRENT, LOAD VOLTAGE AND LOAD CURRENT
(iii) LINE VOLTAGES V_{RB} AND V_{RY}, THYRISTOR T_1 VOLTAGE AND TRIGGERING PULSE G_R

Delta-Star transformer is not available, three signal-phase transformer ($220V : 6V$) can be used as shown in the Driver Circuit (Fig. 4.79).

The three separate but identical cards (R-card, Y-card and B-card) are used for controlling the triggering angles of the positive group thyristors T_1, T_3 and T_5 respectively. These cards function as follows :

The phase shifters (R-C circuits) shift phase signal voltages R_o, Y_o and B_o in reverse direction (to right side). Adjust the preset $100K$ Pot (Pr) of the Phase-Shifters for shifting by 60^o, in the reverse direction (right side), the phase voltages R_o, Y_o and B_o. The output waves R_{o1}, Y_{o1} and B_{o1} of the Phase-Shifters are used as synchronised signal voltages for R, Y and B phases respectively.

The zero crossover detectors generate rectangular wave pulses (R_1, Y_1 and B_1). The isosceles triangular waveforms (R_2, Y_2 and B_2) are obtained at the output of the integrators. The comparators compare the triangular waveforms (R_2, Y_2 and B_2) with a dc voltage V_c which varies between $+V_{cc}$ to $-V_{cc}$ and is controlled by the $47K$ Pot (P). The outputs of the comparators (R_3, Y_3 and B_3) from inputs to the pulse generators (monostable). The monostable outputs are R_4, Y_4 and B_4. The waveforms (R_4, Y_4 and B_4) are used as clocks and clear pulses for J-K Flip-Flops F/F_1, F/F_2 and F/F_3 as shown in the Fig. 4.79. Outputs of the J-K flip/flops R_5, Y_5 and B_5 are the required $120°$ conduction pulses for the positive group thyristors (T_1, T_3 and T_5) respectively.

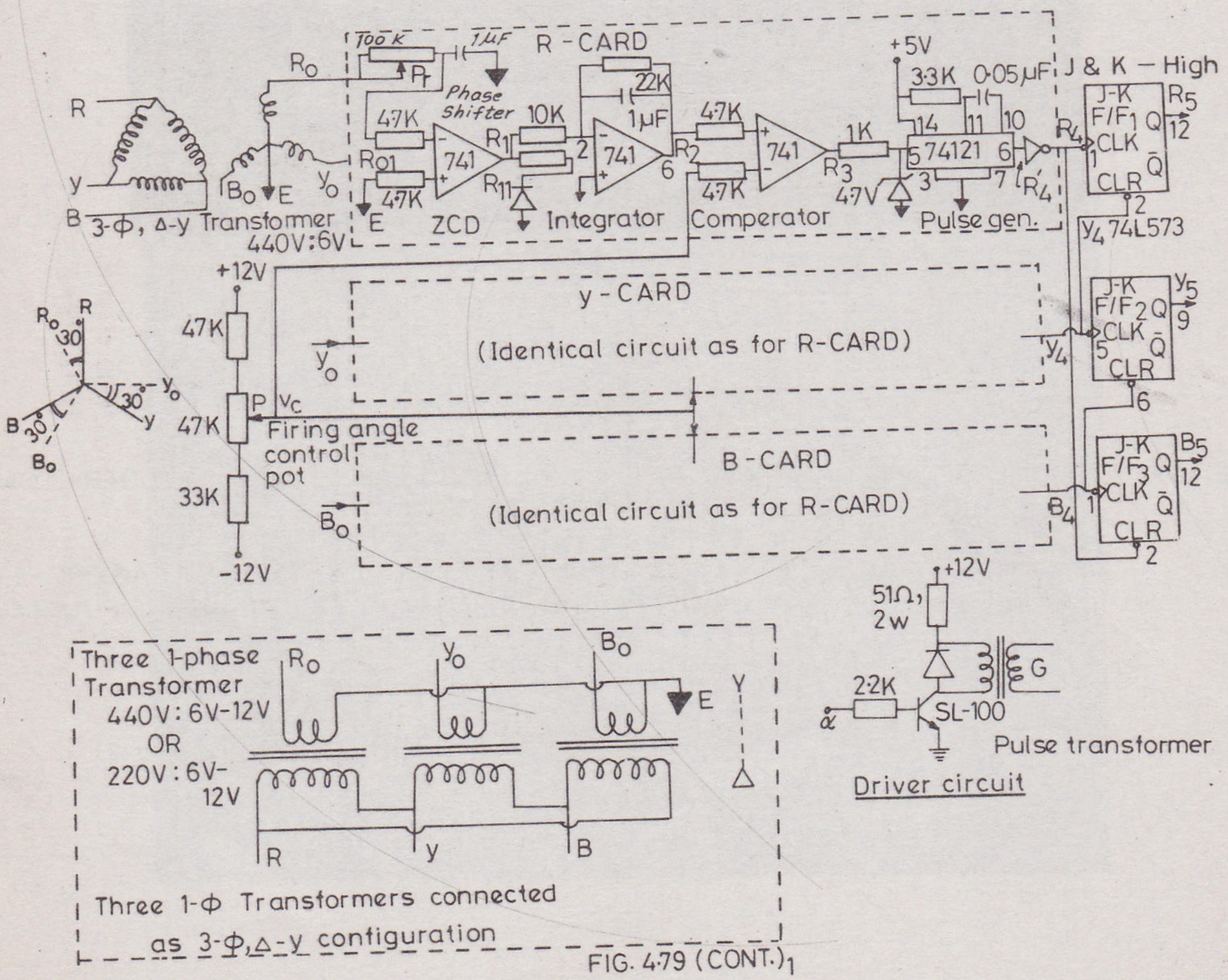


FIG. 4.79 (CONT.)

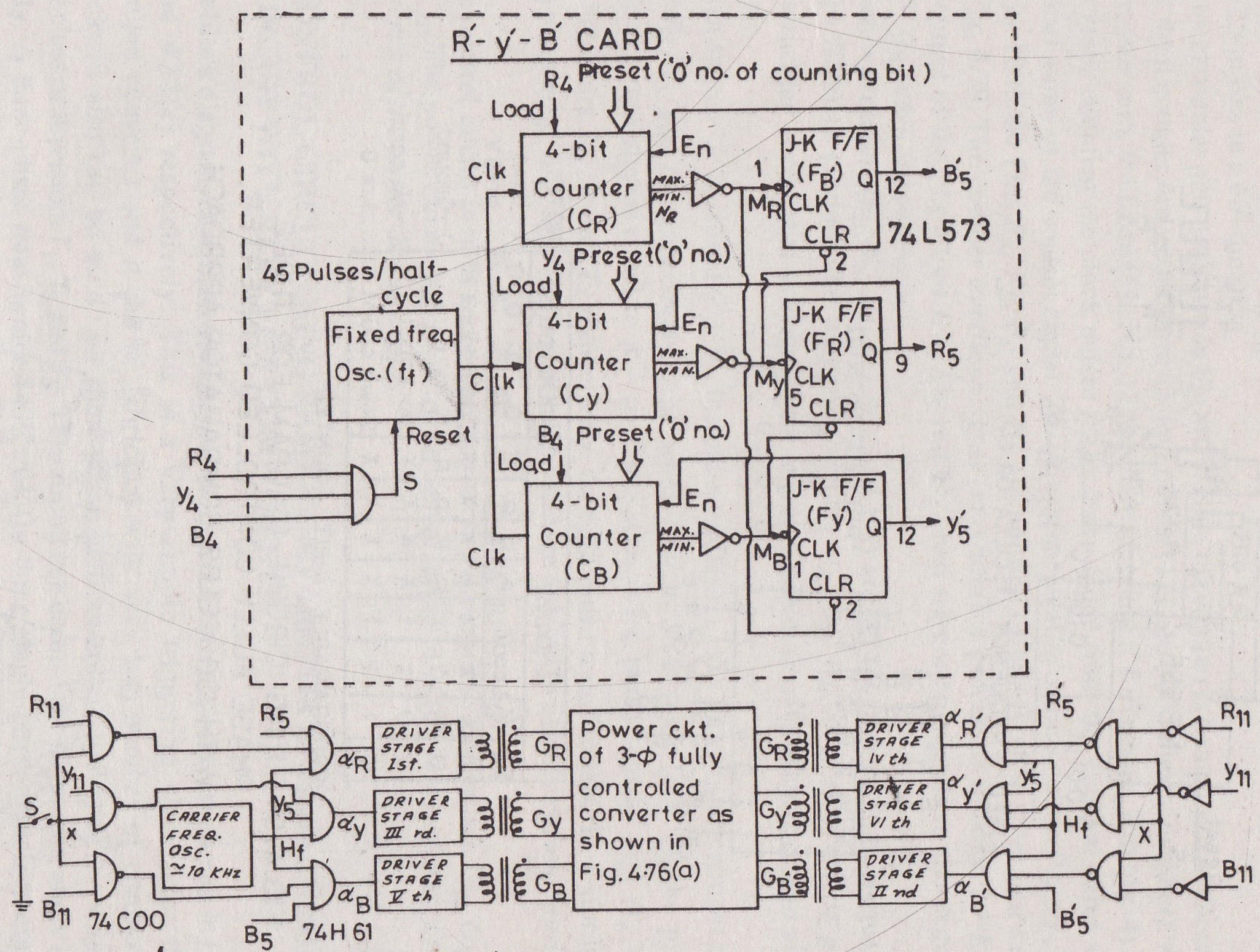
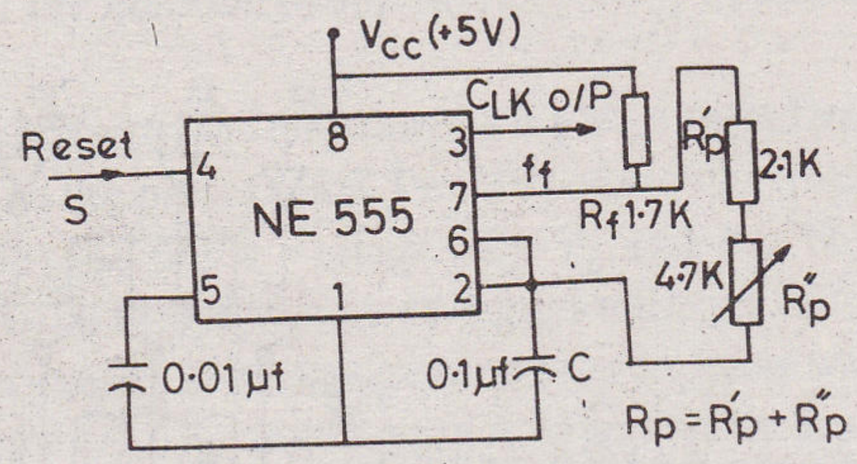
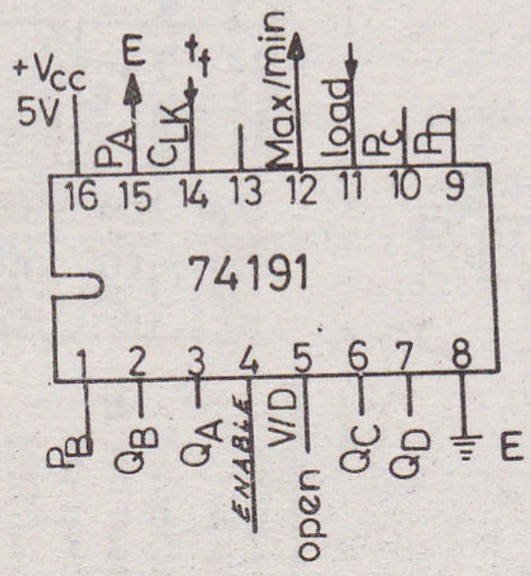


FIG. 4.79 (CONT)$_2$



FIXED FREQUENCY OSCILLATOR (f_f)



PRESET No. 'N=0'

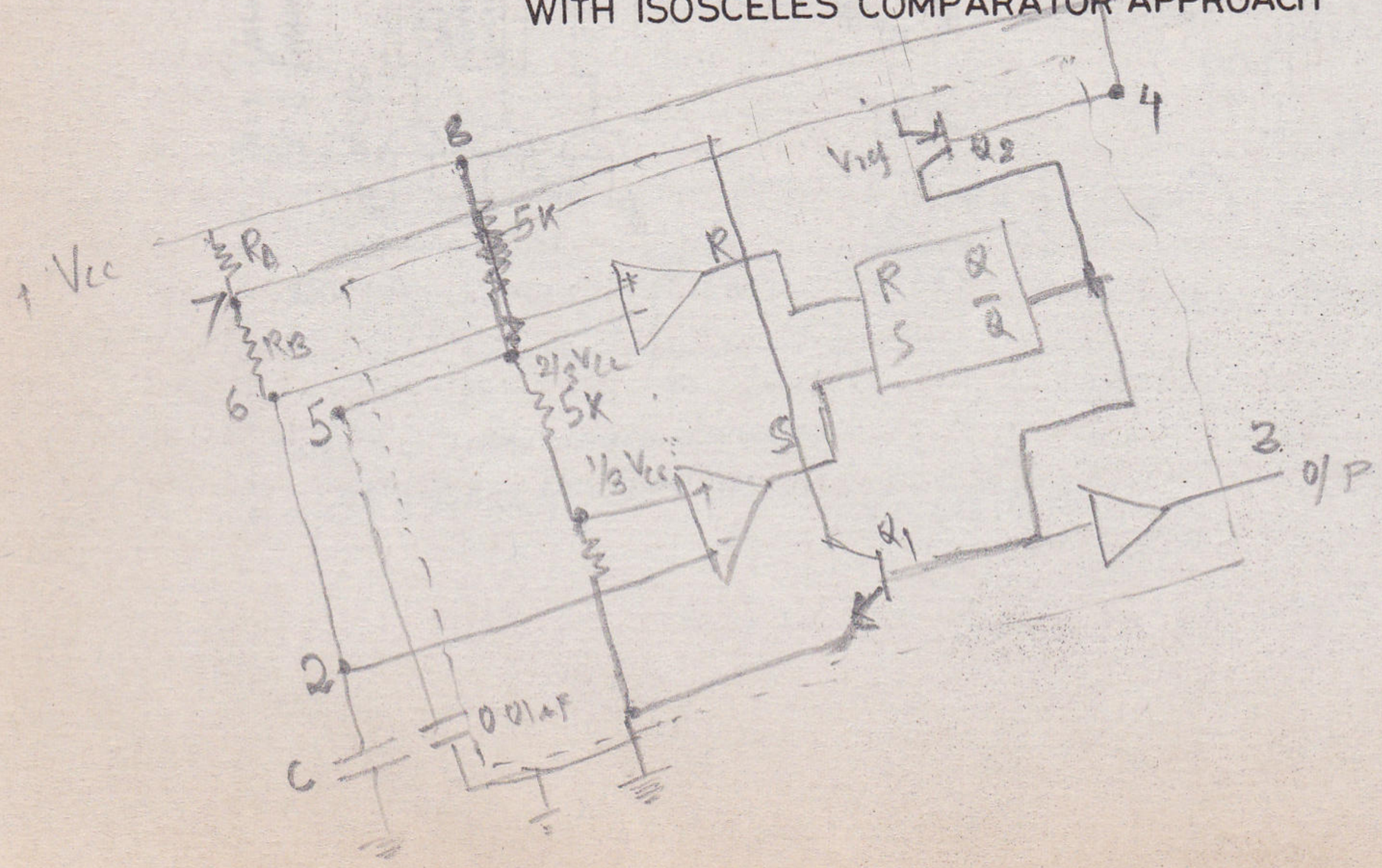
P_D	P_C	P_B	P_A
0	0	0	0

Inputs								Outputs			
E_N	$V/\overline{D}$	Load	C_{LK}	P_A	P_B	P_C	P_D	Q_D	Q_C	Q_B	Q_A
1	X	X	X	X	X	X	X	Stop count			
0	X	0	X	P_A	P_B	P_C	P_D	P_D	P_C	P_B	P_A
0	0	1	↑	X	X	X	X	Up count			
0	1	1	↑	X	X	X	X	Down count			

NOTE:
1 → Open or +5 V
0 → Ground
X → No care 1 or 0

PROGRAMABLE 4-BIT COUNTER

FIG.479: FIRING CIRCUIT DIAGRAM FOR THREE PHASE FULLY CONTROLLED CONVERTER WITH ISOSCELES COMPARATOR APPROACH



The *R'—Y'—B'*—card is used for controlling the triggering angles of the negative group thyristors T_2, T_4 and T_6. This card functions as follows :

The waveforms R_4, Y_4 and B_4 (obtained from *R*-card, *Y*-card and *B*-card respectively) are ANDed together to produce a waveform '*S*' which resets to the Fixed Frequency Oscillator (f_f). Connect one channel of the oscilloscope to synchronised signal and other channel to the output pulses of the oscillator. Adjust the preset Pot R_p" such that the oscillator generates 45 pulses in a half-cycle duration or 15 pulses in a 60^o duration.

Connect counter pins as shown in Fig. 4.79. Here the counter is being used in 'Down counting mode'. The 4-bit counter can count from 15 to 0 pulses (1111 to 0000 binary number). As soon as, R_4 signal crosses zero, the Load (Pin No. 11) become high and if *En* (enable, Pin No. 4) is low then the counter starts counting the clock pulses (f_f) in down mode from the decimal value 15 until the preset decimal value of the control signal '*N*' (*N* = binary value of pins status P_D, P_C, P_B and P_A respectively). Here the Pins P_A, P_B, P_C and P_D are put low (ground) (*N* = 0; or can say 0000) as shown in Fig. 4.79. The counter overflow signal (max/min) is processed to trigger *J-K* Flip-Flop. Thus, the, output of the Flip-Flops B'_5, R'_5 and Y'_5 form triggering signals to the negative group thyristors T_2, T_4 and T_6 respectively.

These waveforms (R_5, Y_5, B_5, B'_5, R'_5 and Y'_5) are ANDed with a high frequency carrier signal ($\simeq$ 10 *KHz*) to produce the triggering signals α_R, α_Y, α_B, α'_R, α'_Y and α'_B. The high frequency switching is essential to reduce gate power dissipation of the thyristor and size of pulse transformers.

When switch '*S*' is closed ($x = 0$), the pulse widths α_R, α_Y and α_B are almost the same as waveforms R_5, Y_5 and B_5 respectively. And when switch '*S*' is open ($x = 1$), the pulse widths α_R, α_Y and α_B are almost equal to $\pi - \alpha$. These modulated pulse signals α_R, α_Y and α_B are applied to thyristors T_1, T_2 and T_3 respectively, through pulse transformers. In a similar way, the triggering pulses α'_B, α'_R and α'_Y are obtained and are applied to negative group thyristors T_2, T_4 and T_6.

The control circuit is built and tested to give the appropriate gate pulses G_R, G_Y, G_B, G'_R, G'_Y and G'_B. The power circuit is completed as shown in Fig. 4.76(a). *It is necessary to check the phase-sequence of the power circuit supply.*

16.2 CONTROL-CIRCUIT USING RAMP-COMPARATOR APPROACH (SIMPLE CIRCUIT WITH VERY FEW COMPONENTS)

The block diagram, control circuit and waveforms at different points are shown in Fig. 4.81(a), 4.81(b) and 4.81(c) respectively. This is a very simple triggering circuit for three-phase fully-controlled converter and it can be fabricated with very less number of components. This triggering circuit also can be used for three-phase half-controlled converter by using only the triggering pulses of thyristors T_1, T_3 and T_5. This circuit can control the triggering angle (α) from 0^o to 120^o only. A three-phase transformer 440*V* : 6*V* (or three single-phase transformers 220*V* : 6*V* connected in Delta-Star (Δ–*Y*) as shown in Fig. 4.79), is employed for obtaining synchronised control triggering pulses from the control cicruit. The secondary voltages (signal voltages) v_{Rt}, v_{Yt} and v_{Bt} of the Delta-star transformer are shifted by 30^o towards forward direction (to left side). The signal voltages v_{Bt}, v_{Rt} and v_{Yt} have 180^o phase difference with v_{RB}, v_{YR} and v_{BY} (line to line voltages) as shown v_{RB} and v_{Bt} voltages in Fig. 4.81(c). Therefore, the outputs R_1, Y_1 and B_1 of the inverting

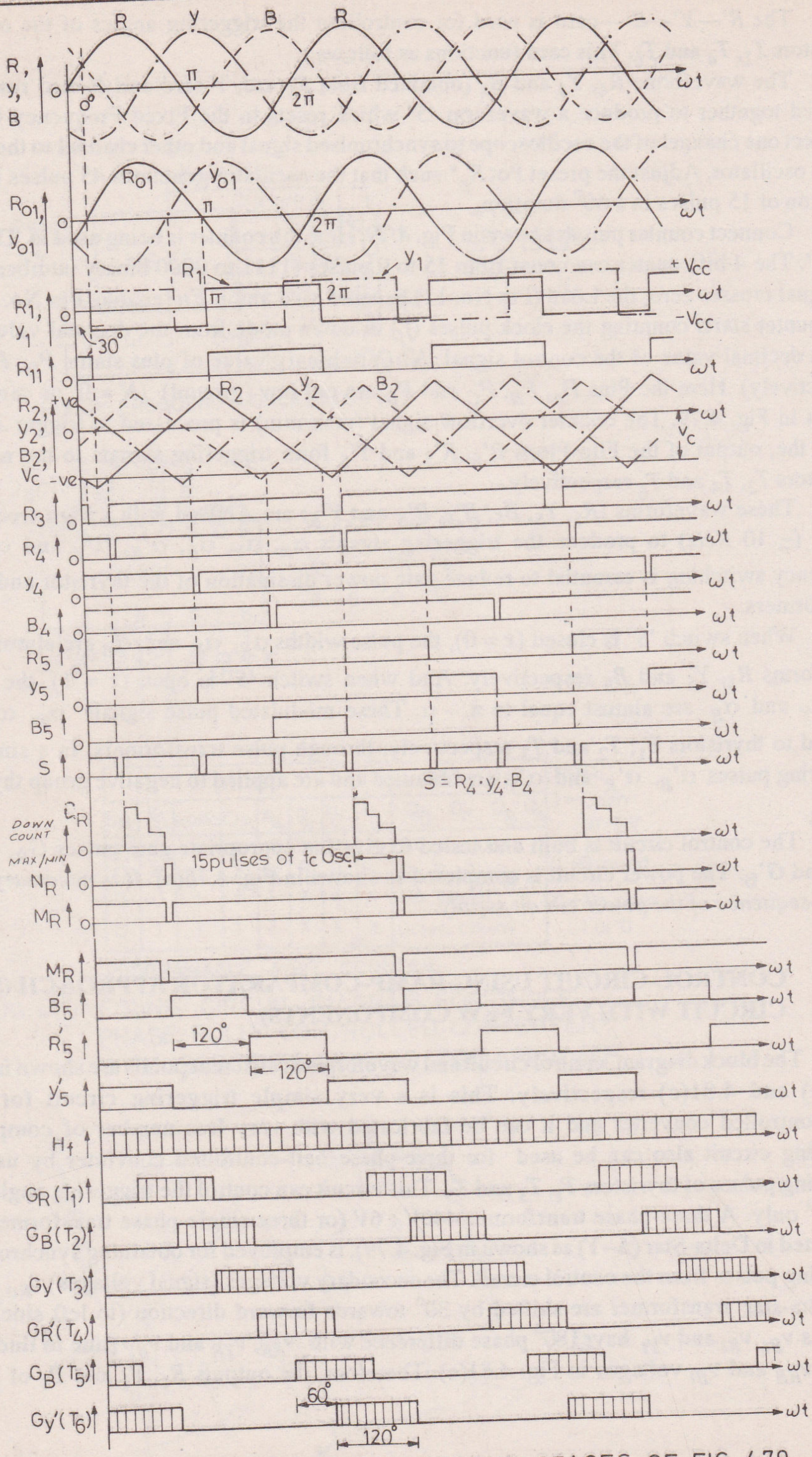
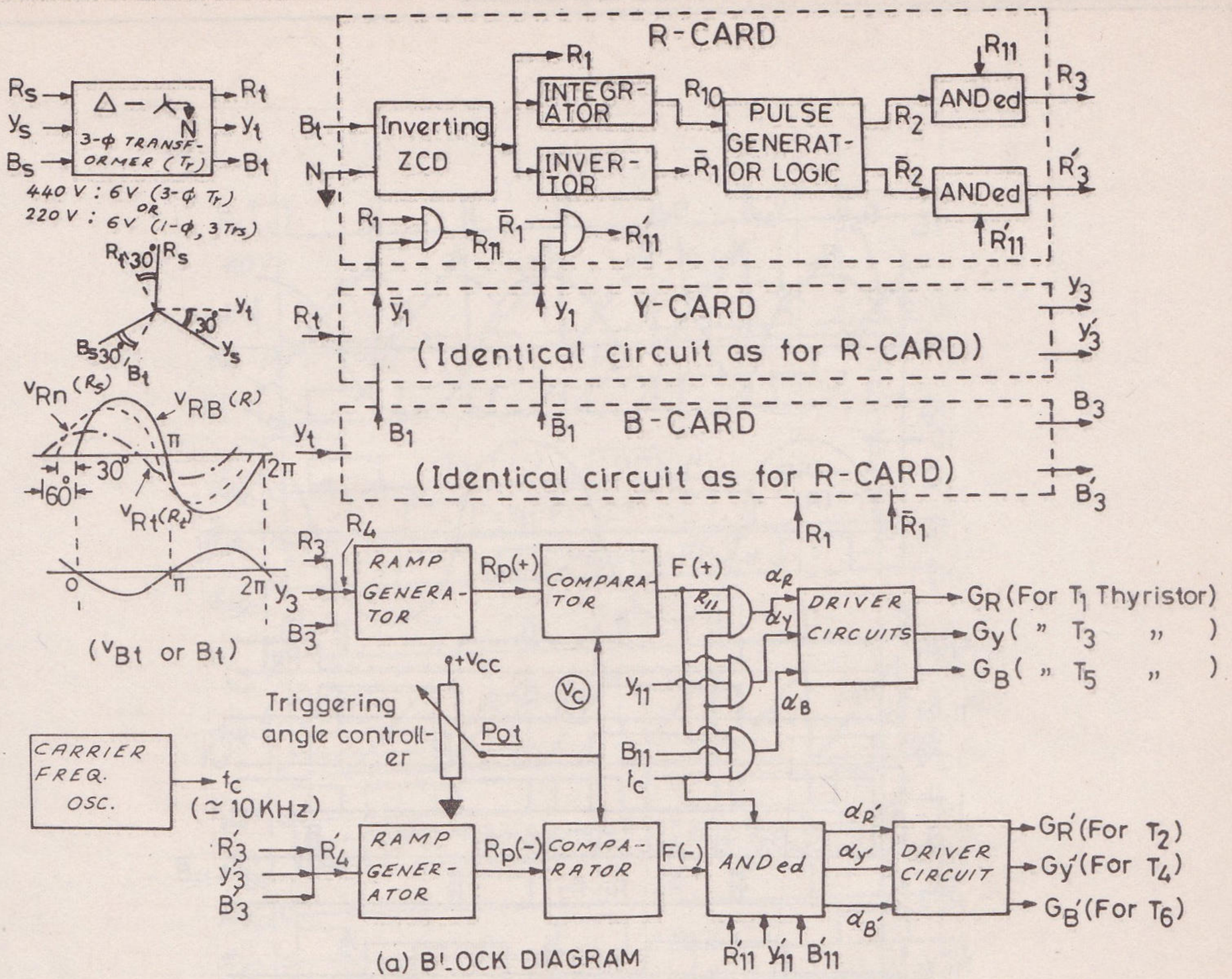
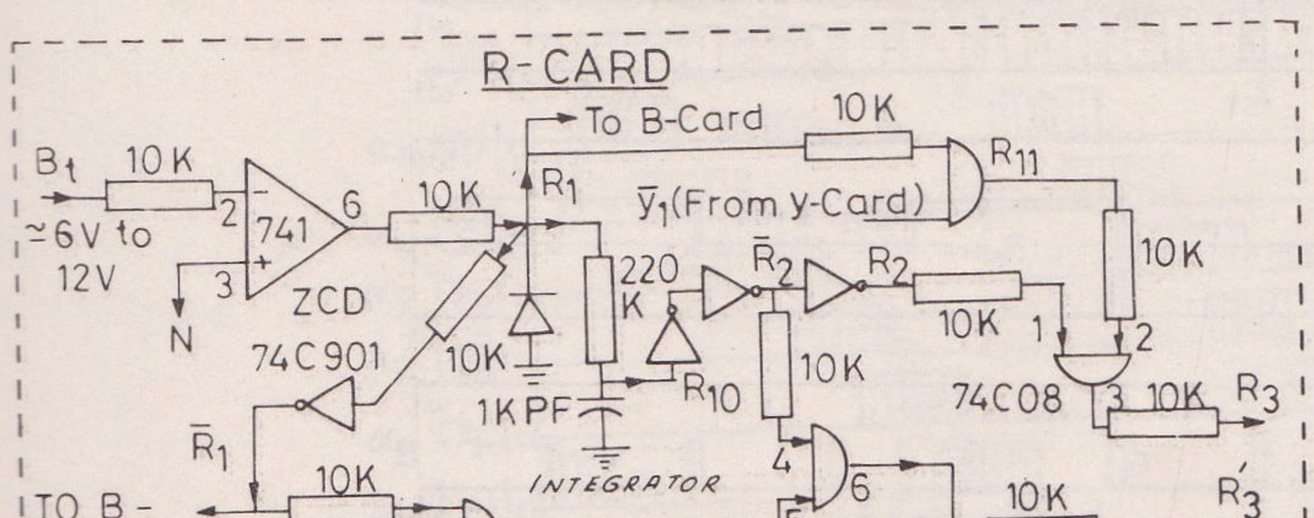
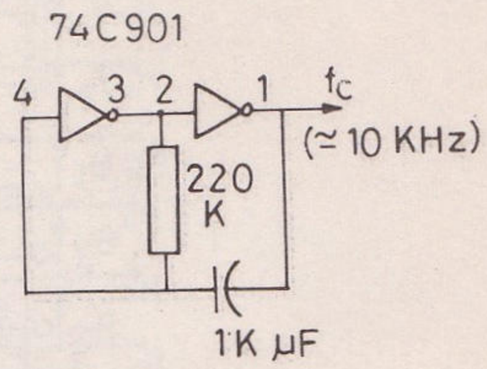


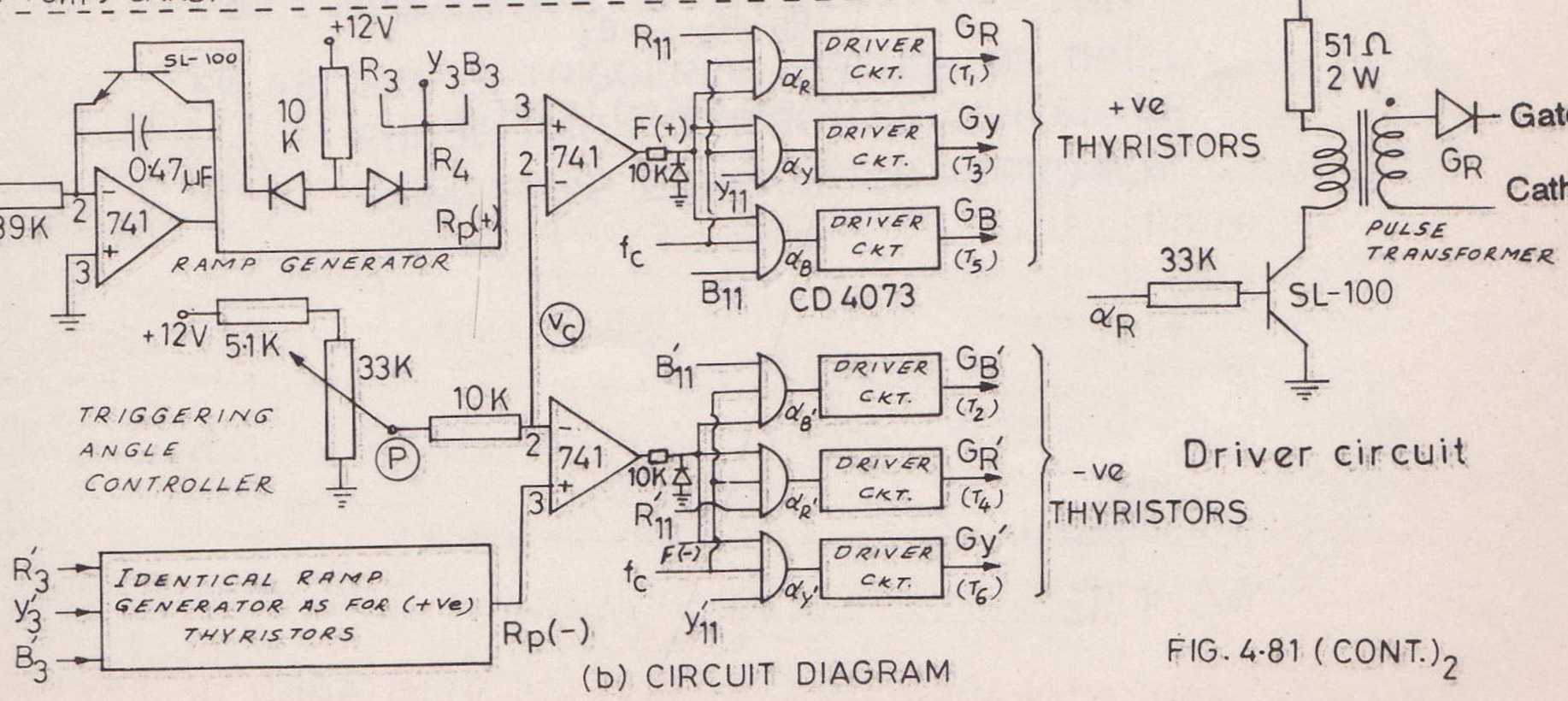
FIG. 4·80: WAVEFORMS AT DIFFERENT STAGES OF FIG 4·79



(a) BLOCK DIAGRAM







(b) CIRCUIT DIAGRAM

FIG. 4-81 (CONT.)2

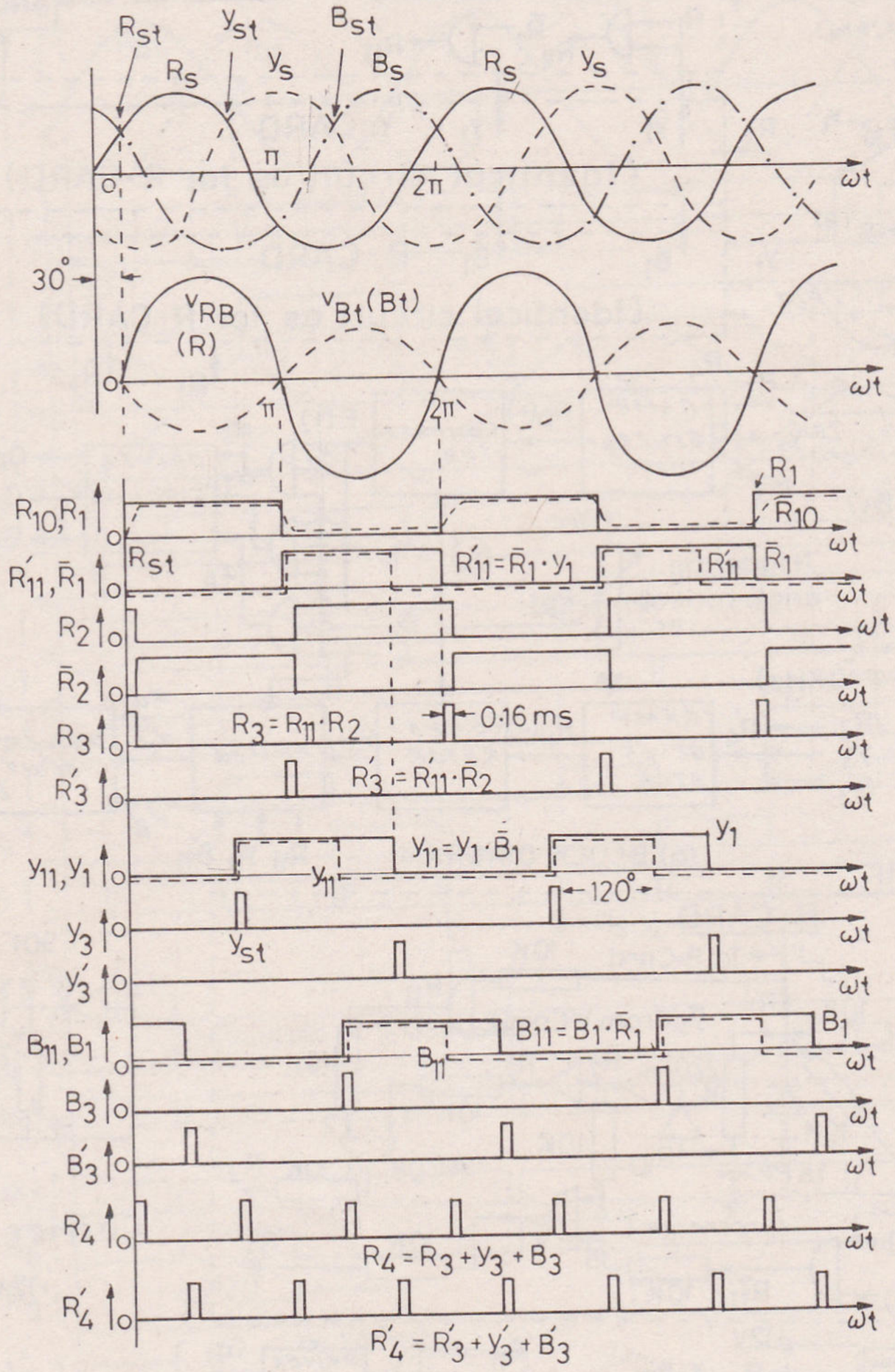
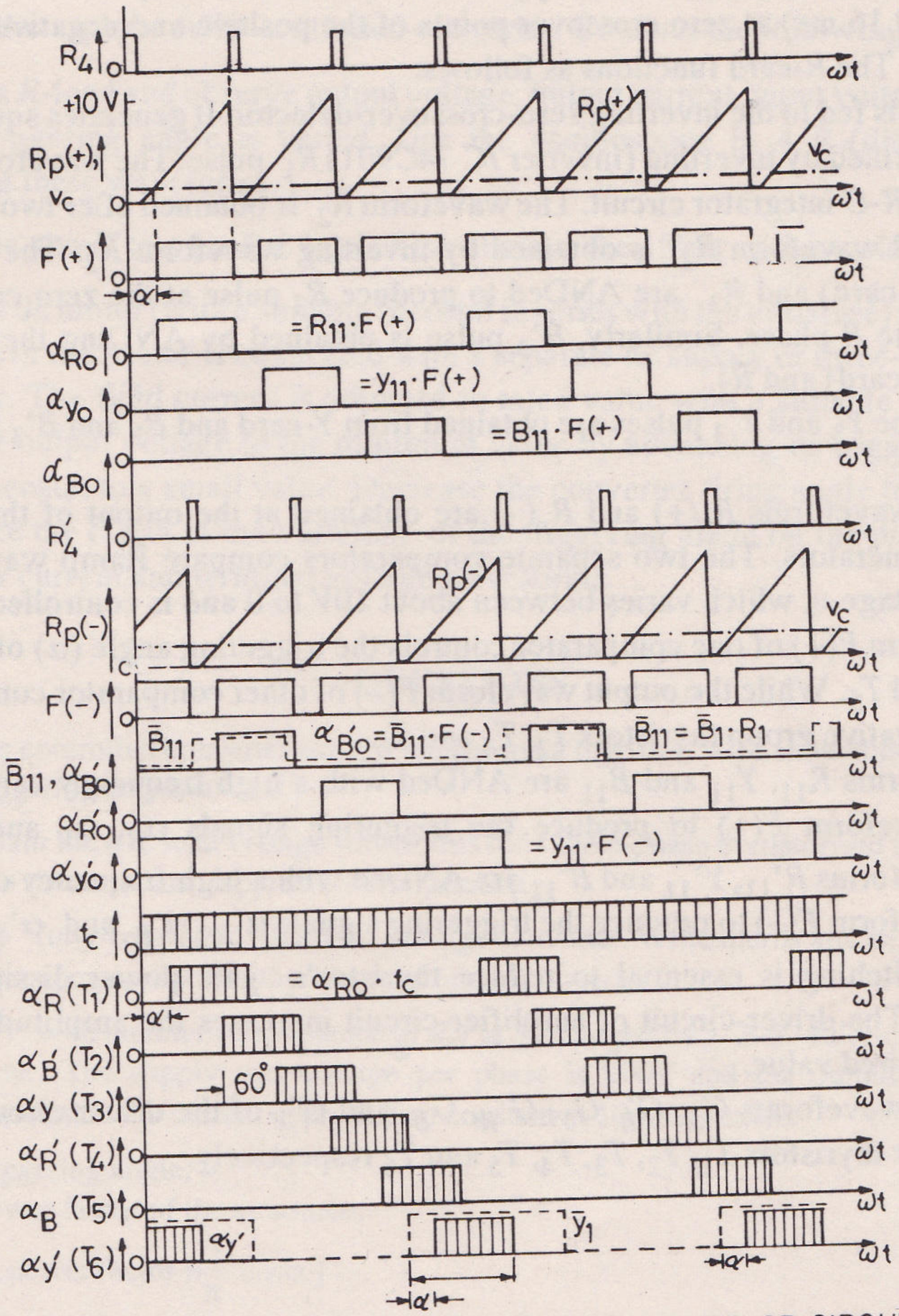


FIG.4·81 (c) (CONT)$_3$



(C) WAVEFORMS AT DIFFERENT POINTS OF CIRCUIT

FIG.4.81: SIMPLE TRIGGERING CIRCUIT FOR THREE PHASE FULLY CONTROLLED CONVERTER USING RAMP COMPARATOR APPROACH

zero-crossover-detectors which have input signal voltages v_{Bt}, v_{Rt} and v_{Yt} respectively, are used as signal voltages for *R*, *Y* and *B* phases respectively.

Three separate but identical cards (*R*-card, *Y*-card and *B*-card) are used for generating the narrow pulses ($\simeq$ 0.16 ms) at zero crossover points of the positive and negative going phases *R*, *Y* and *B* respectively. The *R*-card functions as follows:

Voltage v_{Bt} is fed to the inverting zero-crossover-detector. It generates square wave pulse R_1. The $\overline{R}_1$ pulse is obtained by inverting (inverter *IC* 74*C*901) R_1 pulse. The waveform R_{10} is obtained at the output of the *R-C* integrator circuit. The waveform $\overline{R}_2$ is obtained after two times inverting the waveform R_{10} and waveform R_2 is obtained by inverting waveform $\overline{R}_2$. The waveforms R_1, $\overline{Y}_1$ (connected from *Y*-card) and R_2 .are ANDed to produce R_3 pulse at the zero crossover point with positive slope of the *R*-phase. Similarly, R'_3 pulse is obtained by ANDing the waveforms $\overline{R}_1$, Y_1 (connected from *Y*-card) and $\overline{R}_2$.

Similarly, the Y_3 and Y'_3 pulses are obtained from *Y*-card and B_3 and B'_3 pulses are obtained from *B*-card.

The ramp waveforms $R_p(+)$ and $R_p(-)$ are obtained at the output of the two separate but identical Ramp-Generators. The two separate comparators compare Ramp waveforms $R_p(+)$ and $R_p(-)$ with a dc voltage v_c which varies between about 10*V* to 0 and is controlled by a 33*K* Pot (*P*). The output waveform *F*(+) of one comparator controls the triggering angle (α) of the positive group thyristors T_1, T_3 and T_5. While the output waveform *F*(–) of other comparator controls the triggering angle (α) of the negative group thyristors T_2, T_4 and T_6.

The waveforms R_{11}, Y_{11} and B_{11} are ANDed with a high frequency carrier signal f_c ($\simeq$ 10 *K*Hz) and the waveform *F*(+) to produce the triggering signals α_R, α_Y and α_B respectively. Similarly, the waveforms R'_{11}, Y'_{11} and B'_{11} are ANDed with a high frequency carrier signal ($\simeq$ 10 *K*Hz) and the waveform *F*(–) to produce the triggering signals α'_B, α'_R and α'_Y.respectively. The high frequency switching is essential to reduce thyristor's gate power dissipation and size of pulse-transformer. The driver-circuit or amplifier-circuit increases the amplitude of the triggering signal upto the required value.

The output waveforms G_R, G'_B, G_Y, G'_R, G_B and G'_Y of the driver circuits are used as the triggering pulses for thyristors T_1, T_2, T_3, T_4, T_5 and T_6 respectively.

Test Procedure

Make any one control circuit as shown in Fig. 4.81(a) and 4.79. Feed the three-phase power supply through three-phase Auto-Transformer to the control circuit for synchronisation. The output voltages of the three-phase Auto-Transformer are adjusted according to the rating of the primary winding of the Delta-Star (Δ–*Y*) transformer connected in the control-circuit. Check whether the firing circuit is working properly or not for all six thyristors. If it is working as expected, check the polarity and phase of the output pulses G_R, G'_B, G_Y, G'_R, G_B and G'_Y of the control circuit. Use proper thyristors and make the three-phase fully-controlled Bridge Converter power circuit as shown in Fig. 4.76(a). See that the incoming power supply (*R*, *Y* and *B*) is properly connected to the bridge and the control circuit so that proper phase sequence is maintained. For safety of the power circuit, it is connected through a properly rated ICTP switch and breaker. Again check the triggering pulses G_R, G_Y and G_B for the positive group thyristors T_1, T_3 and T_5 respectively and the triggering pulses G'_B, G'_R and G'_Y for the negative group thyristors T_2, T_4 and T_6 respectively before breaker is switched

'ON'. The triggering pulses G_R, G'_B, G_Y, G'_R, G_B and G'_Y which are shown in Fig. 4.81(c), are delivered to the gate of thyristors T_1, T_2, T_3, T_4, T_5 and T_6. Note the synchronisation w.r.t. the supply.

After completing the above procedure, connect required load and release the three-phase power supply (breaker to be switched 'ON') and firing pulses to thyristors. The cricuit will be ready for operation as a three-phase fully-controlled converter. Conduct the following tests :

Test 1 : Connect a *R*-load and observe output voltage, output current, input voltage and input current as the triggering angle is varied. Use the oscilloscope in *A-B* (differential) mode for observing these waveforms.

Test 2 : Repeat the above test for *R-L* load. Also observe the effect of the variation of *R*.

Test 3 : Connect a dc motor (with a suitable rheostat in series with the armature) across the converter. The field of the motor is connected with a separate dc supply or three-phase diodes bridge converter. The field current is adjusted to rated value with a suitable rheostat. Adjust the converter output voltage to the minimum value by advancing its triggering angle. Slowly set the rheostat to a small value. Decrease the converter firing angle to increase the motor speed. See the effect of the variation of the triggering angle on the motor speed. Observe the motor current and terminal voltage waveforms.

QUESTIONS

16.1 Describe a 3–ϕ controlled converter using 6 diodes and a thyristor. Also show time variation of *R-L* load voltage for triggering angle, $\alpha = 60^\circ$.

16.2 Draw and explain the *R-L* load voltage waveforms for a three-phase thyristorised fully-controlled bridge converter when the source has appreciable inductance.

16.3 Describe a 3–ϕ fully-controlled MOSFETs bridge converter. Write merits and demerits of a MOSFETs bridge converter compared to the thyristorised bridge converter.

16.4 A battery $400V$ with an internal resistance of $0.5\ \Omega$ is charged by a 3–ϕ fully-controlled thyristorised bridge converter. The supply rms voltage per phase is $200V$ and the output circuit has sufficient inductance to maintain the current approximate constant at $10A$. Calculate:

(i) The triggering angle, α

(ii) The power factor of the ac source.

[Hint : power factor $= \frac{3}{\pi} \cos\alpha$]

(iii) The value of resistor connected in series with the battery, if triggering angle, $\alpha = 0^\circ$.

16.5 A 3–ϕ fully-controlled converter supplies a *R-L* load. Draw a graph between the triggering angle (α) for $0 \le \alpha \le 180^\circ$ and the load voltage. Also show the value of the load voltage at the triggering angles of 0°, 45°, 60°, 90°, 110°, 150° and 175° if the supply rms voltage is $100V$ line-to-line.

Experiment No. 17

Objective : To study and test a Three-phase Thyristorised AC Regulator.

Apparatus Required

Multi (at least dual) beam oscilloscope; Thyristor lab. power module; Three-phase switch, Circuit breaker; Variac, Resistive load, *R-L* load, Induction motor load, Shunt, any one of the fabricated triggering circuits for three-phase ac regulator. See appendix 1 for selecting the rating of the apparatus.

Function

The three-phase ac regulators convert a fixed three-phase ac voltage to a variable three-phase ac voltage at the same frequency. The three-phase ac regulators (ac voltage controllers) are used for the speed control of three-phase induction motors, the temperature control of three-phase ovens and as voltage controller starters of induction motors. The induction motors controlled by ac regulators find wide applications in three-phase pumps, fans, crane drives, induction heating and food blenders.

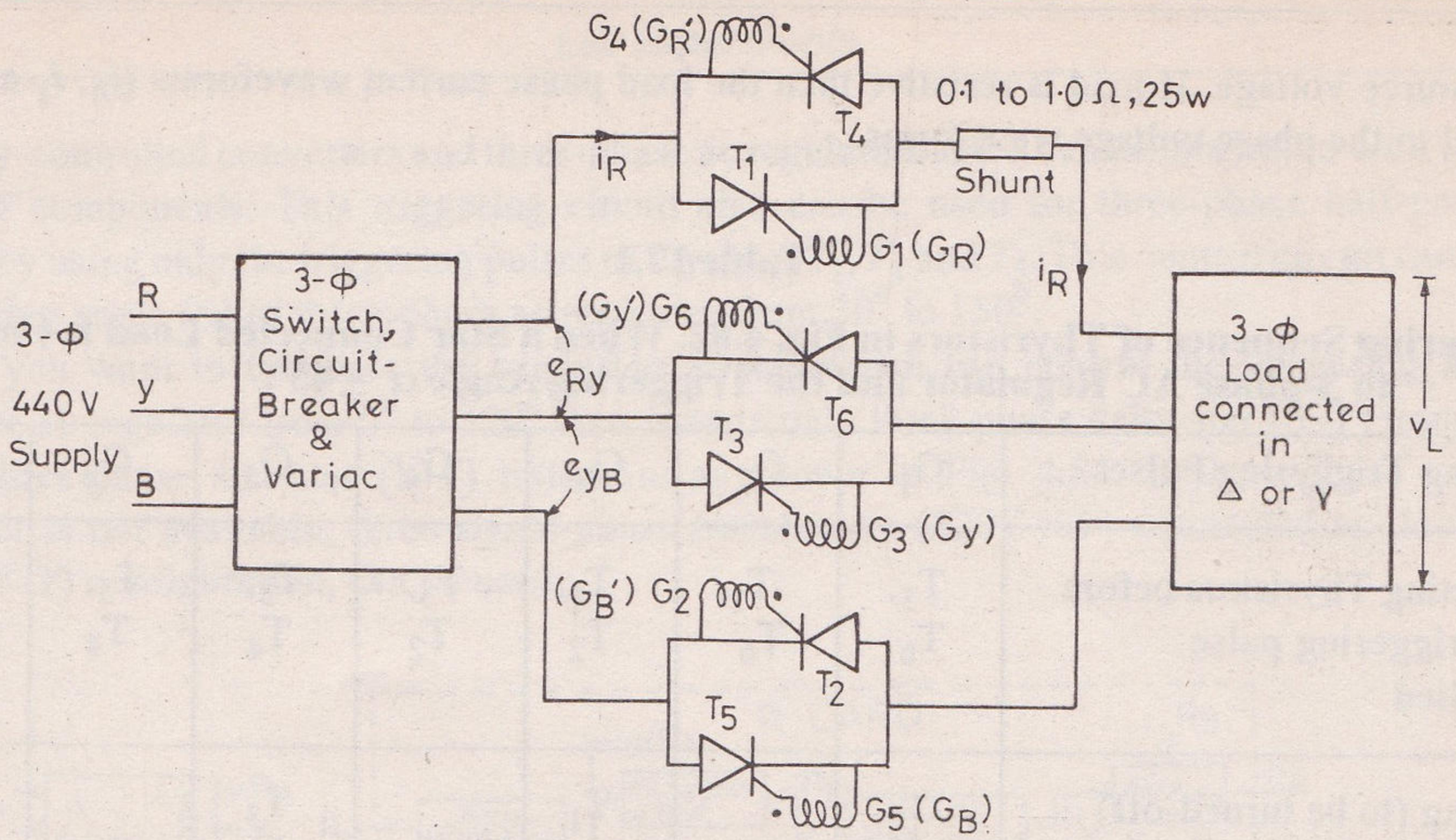
So many types of the three-phase thyristorised ac regulators are described in the literature. Fig. 4.82 shows a commonly used symmetrical three-phase ac regulator for *Y* (Wye) or Δ (Delta) connected loads. For small three-phase load, each antiparallel thyristors pair can be replaced by a triac.

If one or two antiparallel thyristor pairs are removed from three-phase ac regulator shown in Fig. 4.82 and corresponding load terminals are connected directly to the power supply, then this type of circuit is called asymmetrical circuit. The asymmetrical circuits increase harmonics in the power supply and greatly reduce the torque of the motor. Hence, the asymmetrical circuits are rarely used.

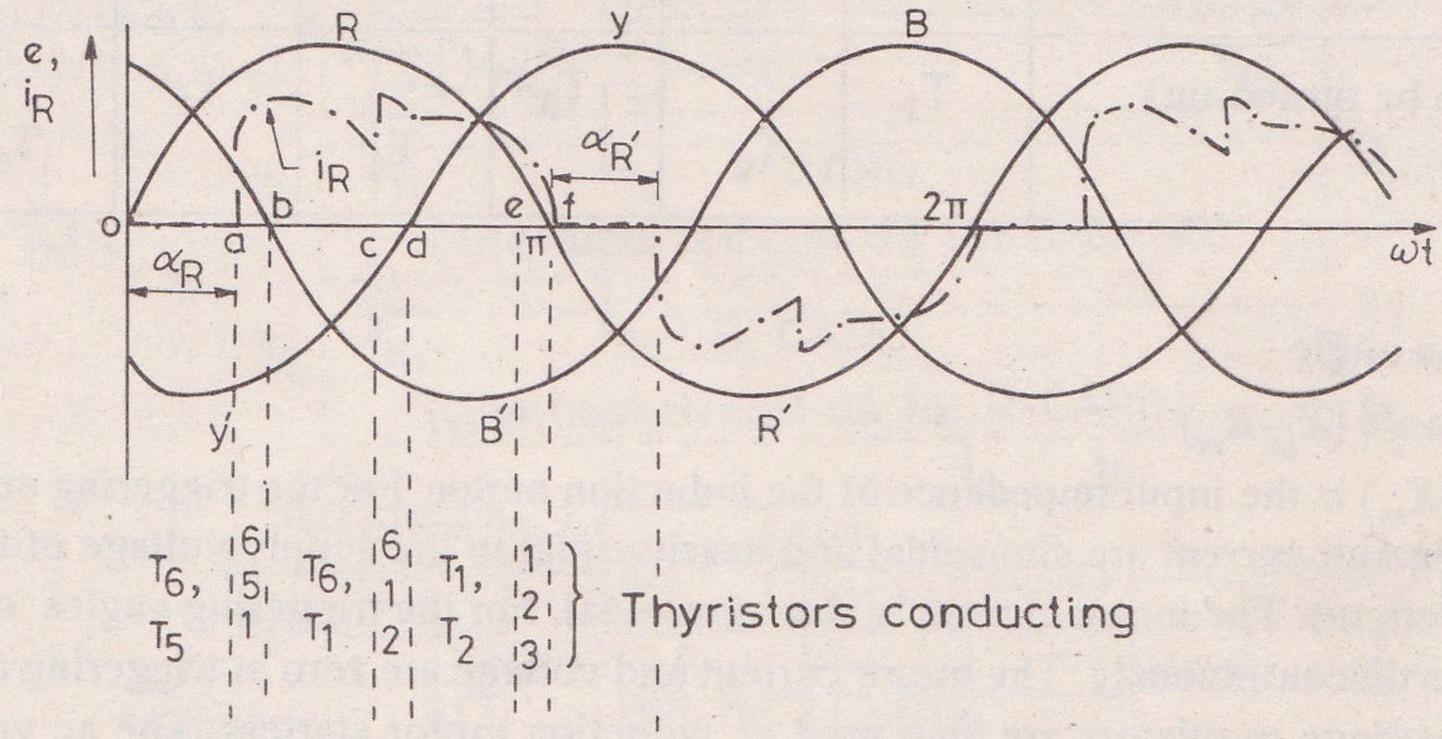
An ac regulator with cheap and simple control can be obtained by replacing one thyristor in each line by a diode. This type of circuit produces even harmonics, and the predominant harmonic is then the second compared to the fifth. At low motor speeds, the second harmonic greatly increases the power losses in the circuit.

The controlled three-phase ac voltage supply is obtained by controlling the triggering angle α of thyristors of a three-phase line-commutated ac controller shown in Fig. 4.82. The triggering angle α is measured from the instant the phase voltages e_R, e_Y and e_B have a zero value.

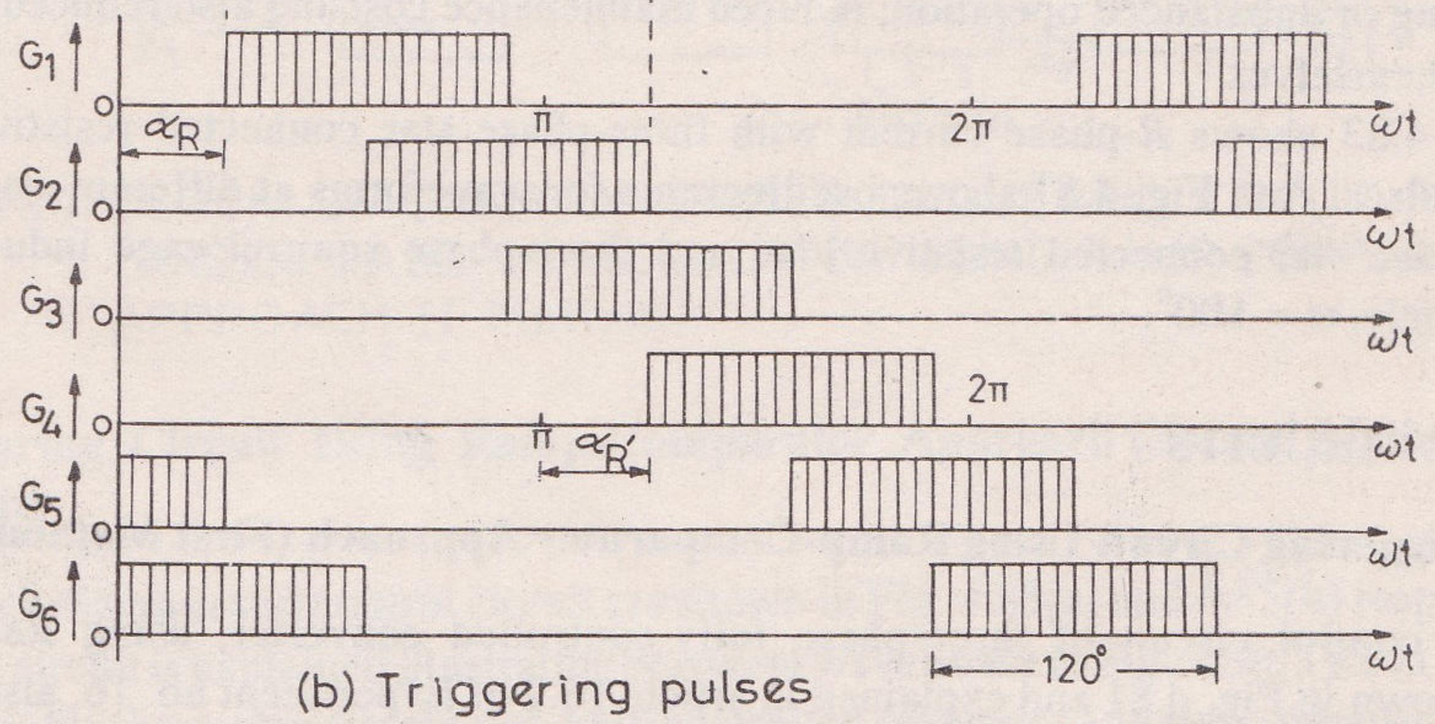
In Fig. 4.82, thyristors T_1, T_3 and T_5 are called positive group thyristors because they are turned-on when the respective phase voltages are positive. Similarly, thyristors T_2, T_4 and T_6 are called negative group thyristors. The thyristors T_1, T_2, T_3, T_4, T_5, T_6, T_1, T_2, ... are turned-on in sequence of their numbers with a phase difference of 60°. In this circuit, two or three thyristors conduct at a time. One thyristor of any pair from the positive group thyristors can supply the load current through the negative group thyristors of other thyristor pairs. So, the conducting thyristors at a time must be belonging to different thyristor pairs of the phases. For example, the conducting thyristor T_1 will be able to supply load current only when thyristors T_2 and/or T_6 are on. It can be noted that the negative group thyristors T_4, T_6 and T_2 are turned-on 180° after the positive group thyristor T_1, T_3 and T_5 respectively. When three thyristors conduct simultaneously, the load phase voltage is identical



FIG·4·82: THREE-PHASE THYRISTORISED A.C. REGULATOR



(a) Input voltage and R-Phase load current waveforms for $\alpha \simeq 45°$ with R-load



(b) Triggering pulses

FIG·8·83: INPUT VOLTAGE, R-PHASE CURRENT WITH RESISTIVE LOAD CONNECTED IN STAR (⅄) | AND TRIGGERING PULSES FOR $\alpha = 45°$

to the source voltage. If load is resistive then the load phase current waveforms (i_R, i_Y and i_B) are identical to the phase voltage waveforms.

Table 17.1

Triggering Sequence of Thyristors in Fig. 4.82. When a Star Connected Load is Connected to 3-phase AC Regulator and the Triggering Angle $\alpha \simeq 45°$.

Incoming Triggering Pulses	G_1	G_2	G_3	G_4	G_5	G_6	G_1
Conducting Thyristors before above triggering pulse are applied	T_5, T_6	T_1, T_6	T_1, T_2	T_3, T_2	T_3, T_4	T_5, T_4	T_5 T_6
Outgoing (to be turned-off) thyristor	T_5	T_6	T_1	T_2	T_3	T_4	T_5
Incoming (to be turned-on) thyristor	T_1	T_2	T_3	T_4	T_5	T_6	T_1

Let an angle

$\phi = \tan^{-1}(X_m/R_m)$

where (R_m+jX_m) is the input impedance of the induction motor. For the triggering angles $\alpha \leq \phi$, the motor voltage and current are sinusoidal and nearly equal to the supply voltage of the three- phase ac regulator circuit. The motor current is also sinusoidal. For the triggering angles $\alpha > \phi$, the motor current flows discontinuously. The motor current and voltage are zero at triggering angle $\alpha = 150°$.

AC voltage regulators are also used as induction motor starters. The ac voltage regulator starters have a number of advantages over conventional starters (star-delta starter, autotransformer starter, etc.), such as, the stepless control of the motor voltage; motor speed can be controlled by the low power control circuit; smooth acceleration and deceleration; simple protection against single-phasing or unbalanced operation; reduced maintenance cost and also reduced power losses in the starters themselves.

Fig. 4.83 shows *R*-phase current with three-phase star connected resistive load and the triggering pulses. And Fig. 4.87 shows oscillograms for waveforms at different stages of Fig. 4.82 for three-phase star connected resistive load and three-phase squirrel cage induction motor for triggering angle, $\alpha = 100°$.

CONTROL CIRCUITS

17.1 Triggering Circuit Using Ramp-Comparator Approach (First Method)

The control circuit of three-phase fully-controlled converter, using Ramp-Comparator approach shown in Fig. 4.81 and explained in article 16.2 of Experiment no. 16, also can be used as the triggering circuit for three-phase ac regulators. This is a very simple triggering circuit for three-

phase fully-controlled converters and three-phase ac regulators and it can be fabricated with very less number of components. This triggering circuit also can be used for three-phase half-controlled converter by using only the triggering pulses of thyristor T_1, T_3 and T_5. This control circuit can control the triggering angle (α) of three-phase ac regulator from 30^o to 150^o.

If you want to fabricate the triggering circuit which can control the triggering angle of three-phase ac regulator from 0^o to 120^o then change only three-phase delta-star (Δ–Y) transformer into the three-phase star-star (Y–Y) transform as shown in Fig. 4.84. If three-phase star-star transformer is not available, three signal-phase transformer ($220V$:$6V$) connected as three-phase star-star (Y–Y) configuration, can be used.

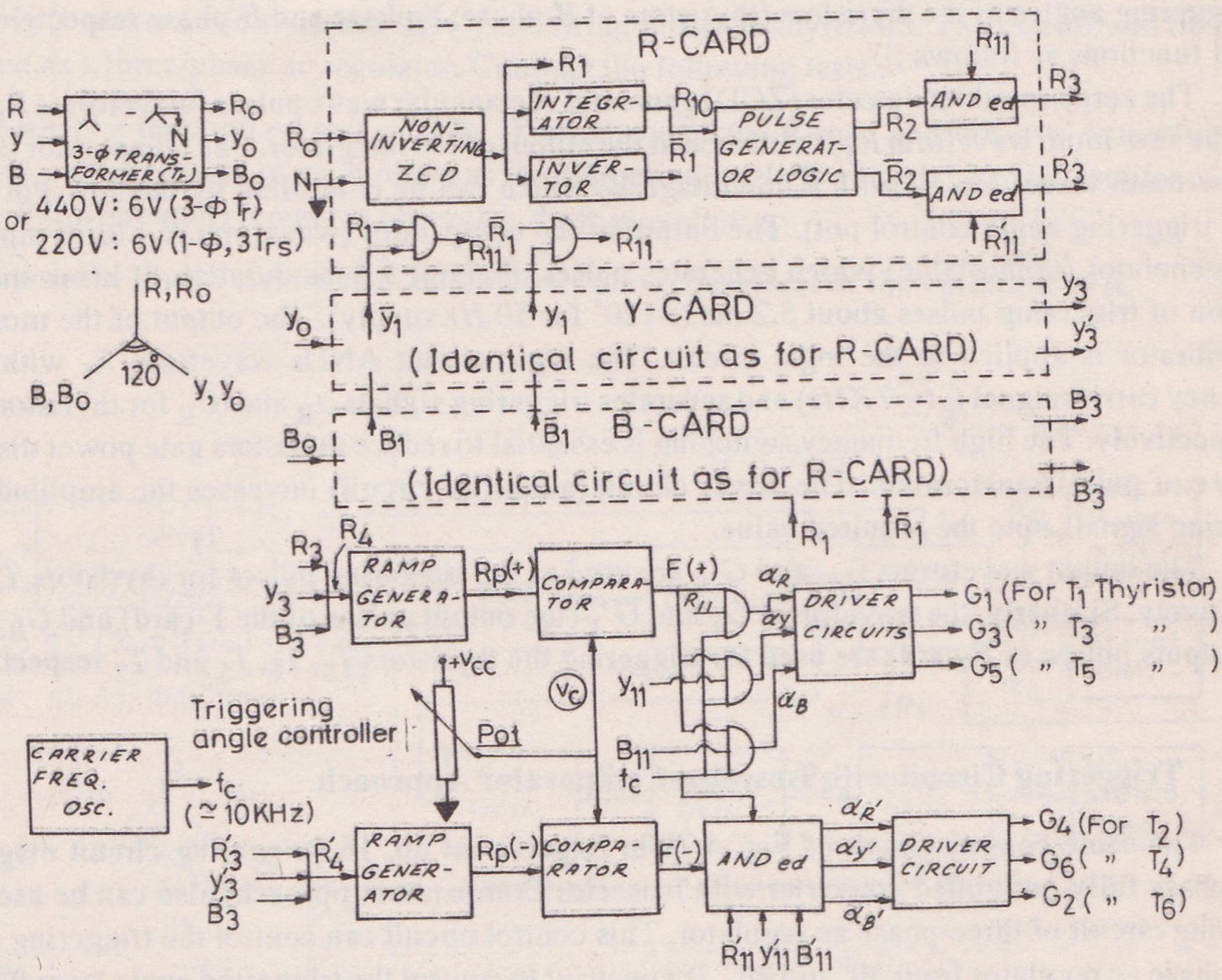


FIG. 4·84: BLOCK DIAGRAM OF SIMPLE TRIGGERING CIRCUIT FOR THREE-PHASE AC REGULATOR USING RAMP-COMPARATOR APPROACH (I- Method)

17.2 Triggering Circuit Using Ramp-Comparator Approach (Second Method — Simple Circuit)

The block diagram and control circuit are shown in Fig. 4.85(a) and 4.85(b) respectively. The operation of the circuit is explained illustrating pertinent waveforms in Fig. 4.86. This is a very simple triggering circuit for three-phase regulator, half-controlled converter and fully-controlled converter, because it can be fabricated with very less number of easy available components. This triggering circuit can be used for three-phase half-controlled converter by using only the triggering pulses of

thyristors T_1, T_3 and T_5. And this triggering circuit also can be used for triggering the single-phase regulator, half-controlled converter and fully-controlled converter by applying single-phase supply between marked R and B phases on the transformer.

The three-phase transformer connected in Delta-Star will shift secondary phase signals voltages R_o, Y_o, and B_o by 60° from the reference points (R_{st}, Y_{st} and B_{st} respectively) of the line to line voltages R, Y and B (e_{RB}, e_{YR} and e_{BY}) respectively as shown in Fig. 4.86. If three-phase transformer is not available then three single-phase transformer ($220V : 6V$) can be used as shown in Fig. 4.79. The secondary voltages (signal voltages) B_o, R_o and Y_o of the Delta-Star (Δ-Y) transformer are used for obtaining synchronised control triggering pulses for R, Y and B phases respectively.

The three separate but identical cards (R-card, Y-card and B-card) are used for controlling the triggering angles of the thyristors (thyristors of R-phase, Y-phase and B-phase respectively). The R-card functions as follows :

The zero crossover detector (ZCD) generates rectangular wave pulses (waveforms R_1, $\overline{R}_1$ and R_2). The saw-tooth waveform R_3 is obtained at the output of the integrator. The comparator compares the saw-tooth waveform R_3 with a dc voltage V_c which can be controlled by the $33K$ Pot (P; also called triggering angle control pot). The output of the comparator (waveform R_4) form input to the pulse generator (monostable) which generates pulses of about 5.2 ms duration. It keeps maximum duration of triggering pulses about 5.2 ms (>120° for 50 Hz supply). The output of the monostable multivibrator is applied to the logic circuit. The logic circuit ANDs waveform R_5 with a high frequency carrier signal f_c ($\simeq 7\,KHz$) and separates triggering signals α_R and α'_R for thyristors T_1 and T_4 respectively. The high frequency switching is essential to reduce thyristors gate power dissipation and size of pulse-transformers. The driver circuit (amplifier circuit) increases the amplitude of the triggering signals upto the required value.

The output waveforms G_R, and G'_R are used as the triggering pulses for thyristors T_1 and T_4 respectively. Similarly, the waveforms G_Y and G'_Y (the output pulses of the Y-card) and G_B and G'_B (the outputs pulses of B-card) are used for triggering the thyristors T_3, T_6, T_5 and T_2 respectively.

17.3 Triggering Circuit with Isosceles-Comparator Approach

The same control circuit of Fig. 4.79 in Experiment no. 16 (triggering circuit diagram for three-phase fully-controlled converter with Isosceles Comparator approach) also can be used as the triggering circuit of three-phase ac regulator. This control circuit can control the triggering angle in three-phase ac regulator from 30° to 180°. If you want to control the triggering angle from 0° to 180° then adjust $100K$ pot of the phase-shifter circuit (R-card of Fig. 4.79) in such a position that the signal R_{01} waveform of the phase-shifter must be in phase with R-phase. Similarly, adjust the $100K$ pot of phase-shifters of Y-card and B-card.

Test Procedure

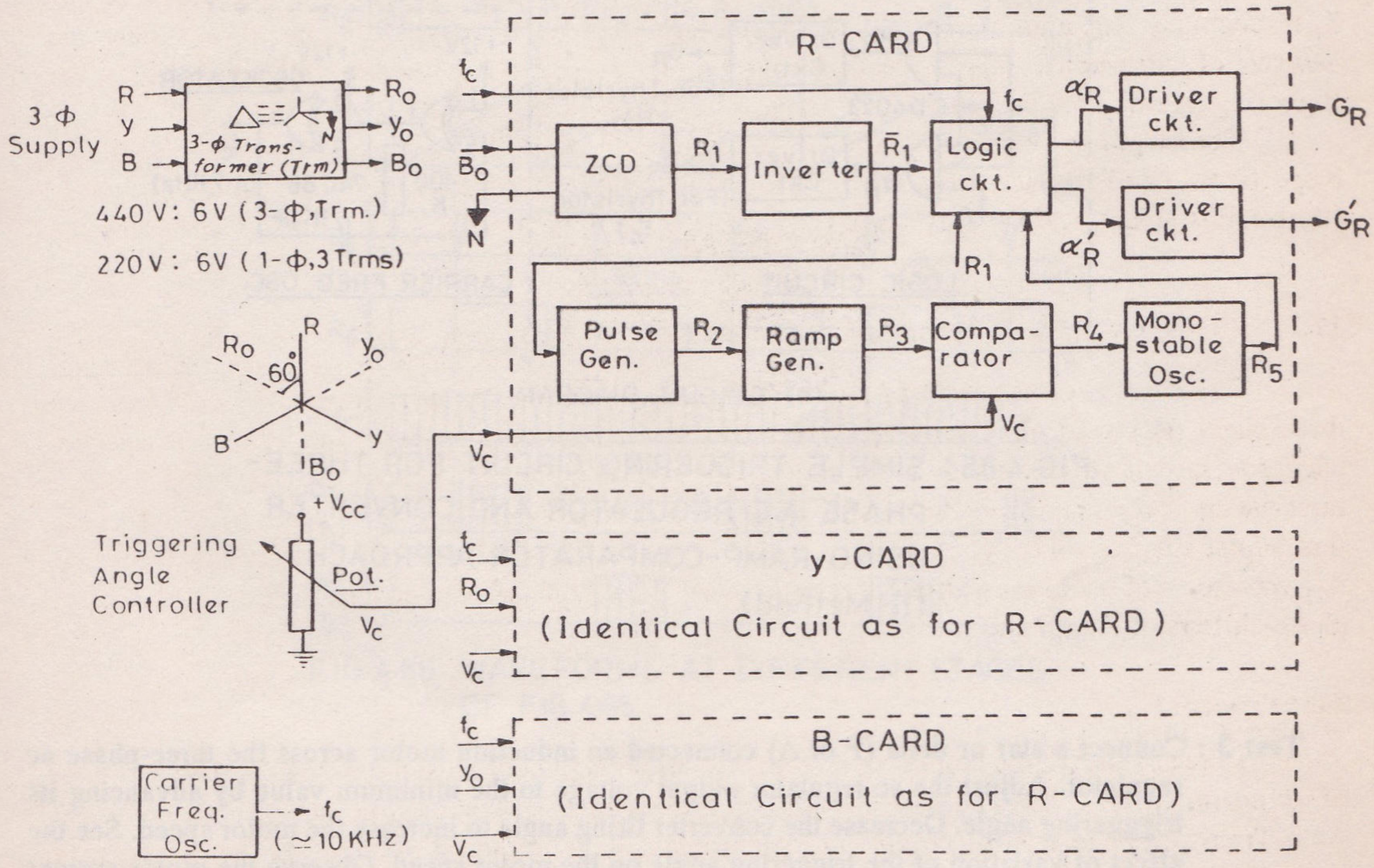
Take any one of the fabricated control circuits, as shown in Figs. 4.81(a), 4.79, 4.84 and 4.85 of Experiment nos. 16 and 17. Feed the three-phase power supply through three-phase Auto-Transformer to control circuit for synchronisation. The output voltages of the three-phase auto-transformer are adjusted according to the rating of the primary winding of the delta-star (Δ–Y) or star-star (Y–Y) transformer connected in the control circuit. Check whether the firing circuit is working properly or not for all six thyristors.

If it is working as expected, check the polarity and phase of the output pulses G_1, G_2, G_3, G_4, G_5 and G_6 of the control circuit. Use proper thyristors and make the three-phase ac regulator power circuit as shown in Fig. 4.82. *See that the incoming power supply (R, Y* and *B) is properly connected to the regulator and control circuit so that proper phase sequence is maintained.* For safety of the power circuit, it is routed through a properly rated ICTP switch and circuit breaker. Again check the triggering pulses G_1, G_3 and G_5 for the positive group thyristors respectively and the triggering pulses G_2, G_4 and G_6 for the negative group thyristors T_2, T_4 and T_6 respectively, before breaker is switched 'ON'. The triggering pulses G_1, G_2, G_3, G_4, G_5 and G_6 which are shown in Fig. 4.83, are delivered to the gate of thyristors T_1, T_2, T_3, T_4, T_5 and T_6. Note sychronisation w.r.t. the supply.

After completing the above procedure, connect the required load and release the three-phase power supply (breaker to be switched 'ON') and firing pulses to thyristors. The circuit will be ready for operation as a three-phase ac regulator. Conduct the following tests :

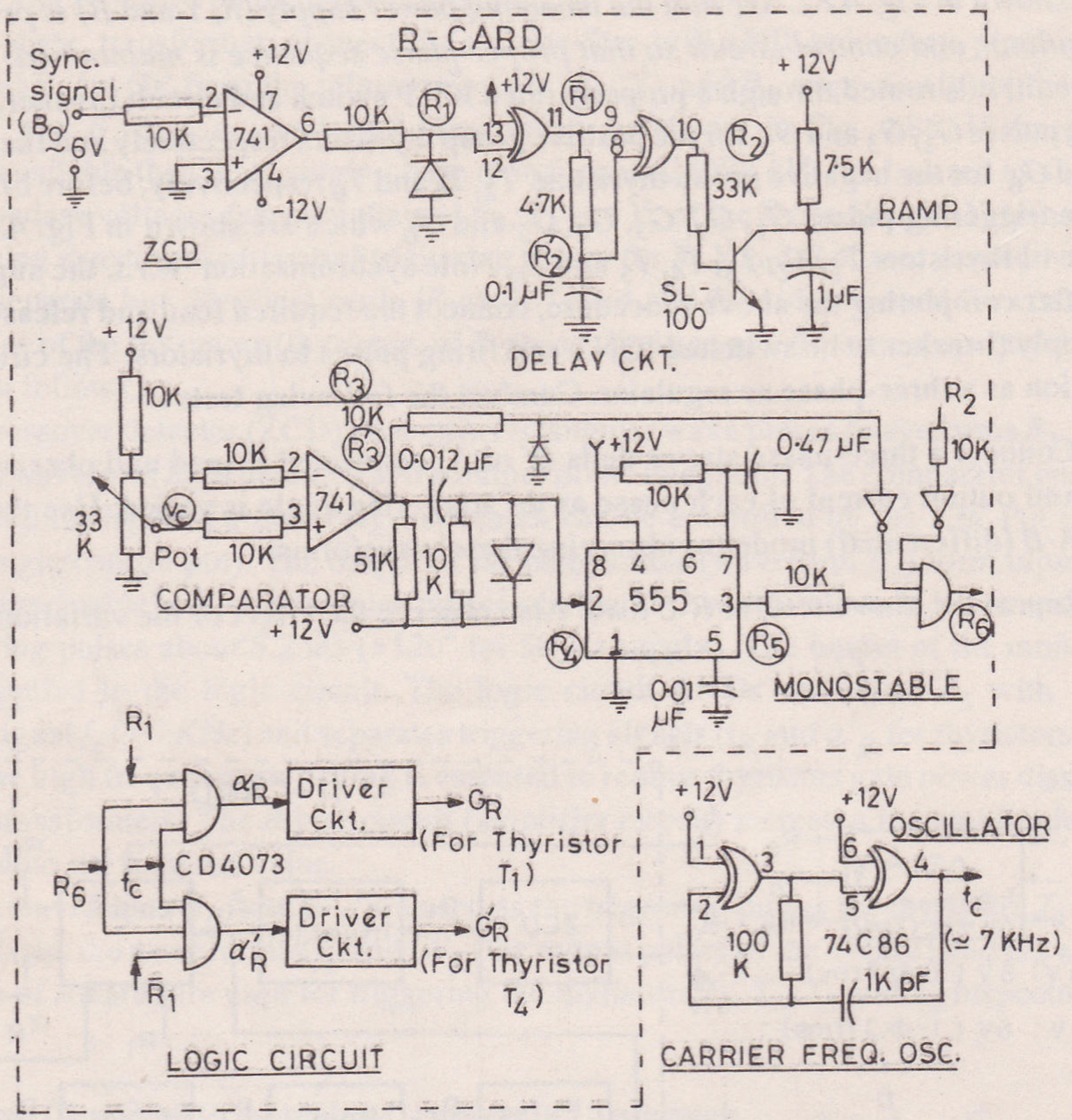
Test 1 : Connect a three-phase star or delta (Y or Δ) connected R-load and observe output voltage and output current of each phase as the triggering angle is varied. Use the oscilloscope in A-B (differential) mode for observing these waveforms.

Test 2 : Repeat the above test for R-L load. Also observe the effect of the variation of R.



(a) BLOCK DIAGRAM

FIG. 4·85 (CONT.)



(b) CIRCUIT DIAGRAM

FIG·4·85 : SIMPLE TRIGGERING CIRCUIT FOR THREE-PHASE A.C. REGULATOR AND CONVERTER USING RAMP-COMPARATOR APPROACH (II-Method)

Test 3 : Connect a star or delta (*Y* or Δ) connected ac induction motor across the three-phase ac regulator. Adjust the ac regulator output voltage to the minimum value by advancing its trigggering angle. Decrease the converter firing angle to increase the motor speed. See the effect of variation of the triggering angle on the motor speed. Observe the motor current and terminal voltage waveforms. Also observe duration of the triggering angle, until both motor current and voltage are sinusoidal.

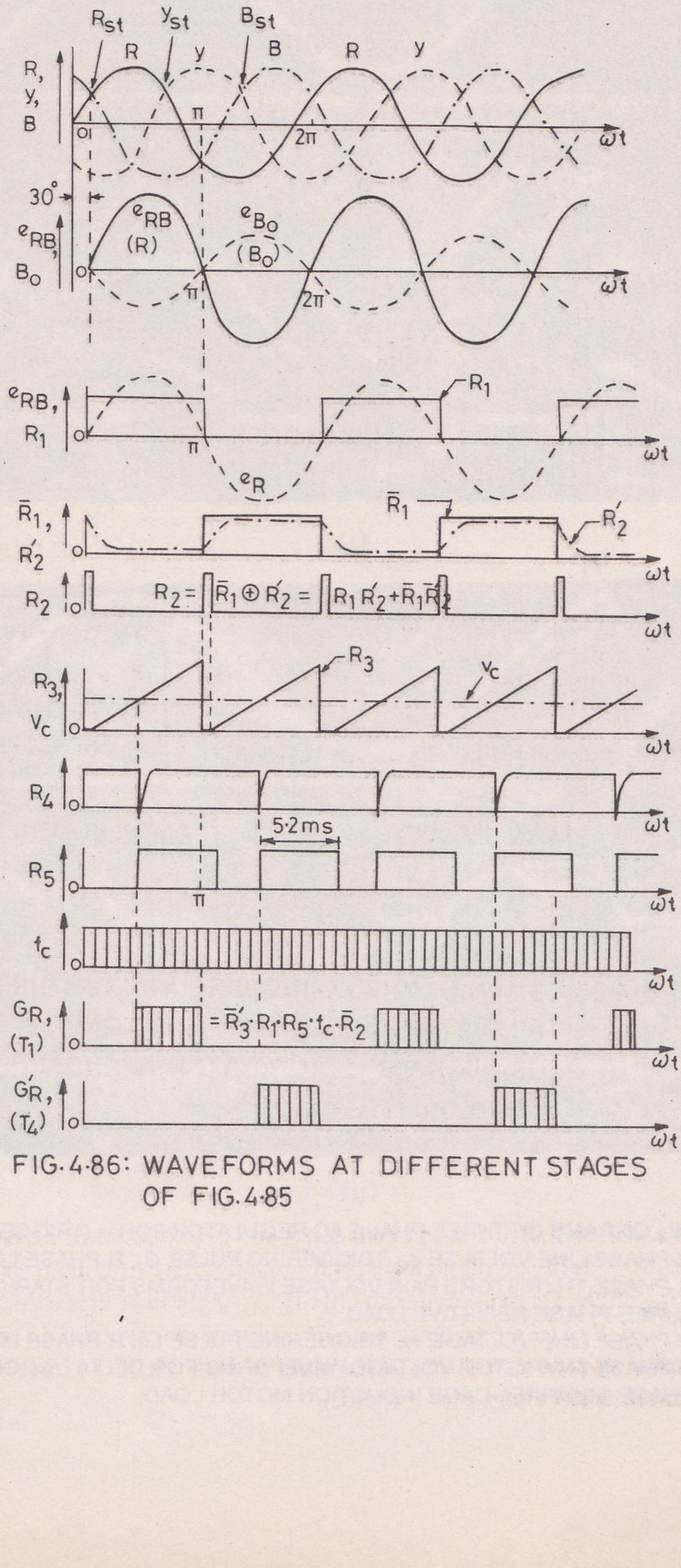
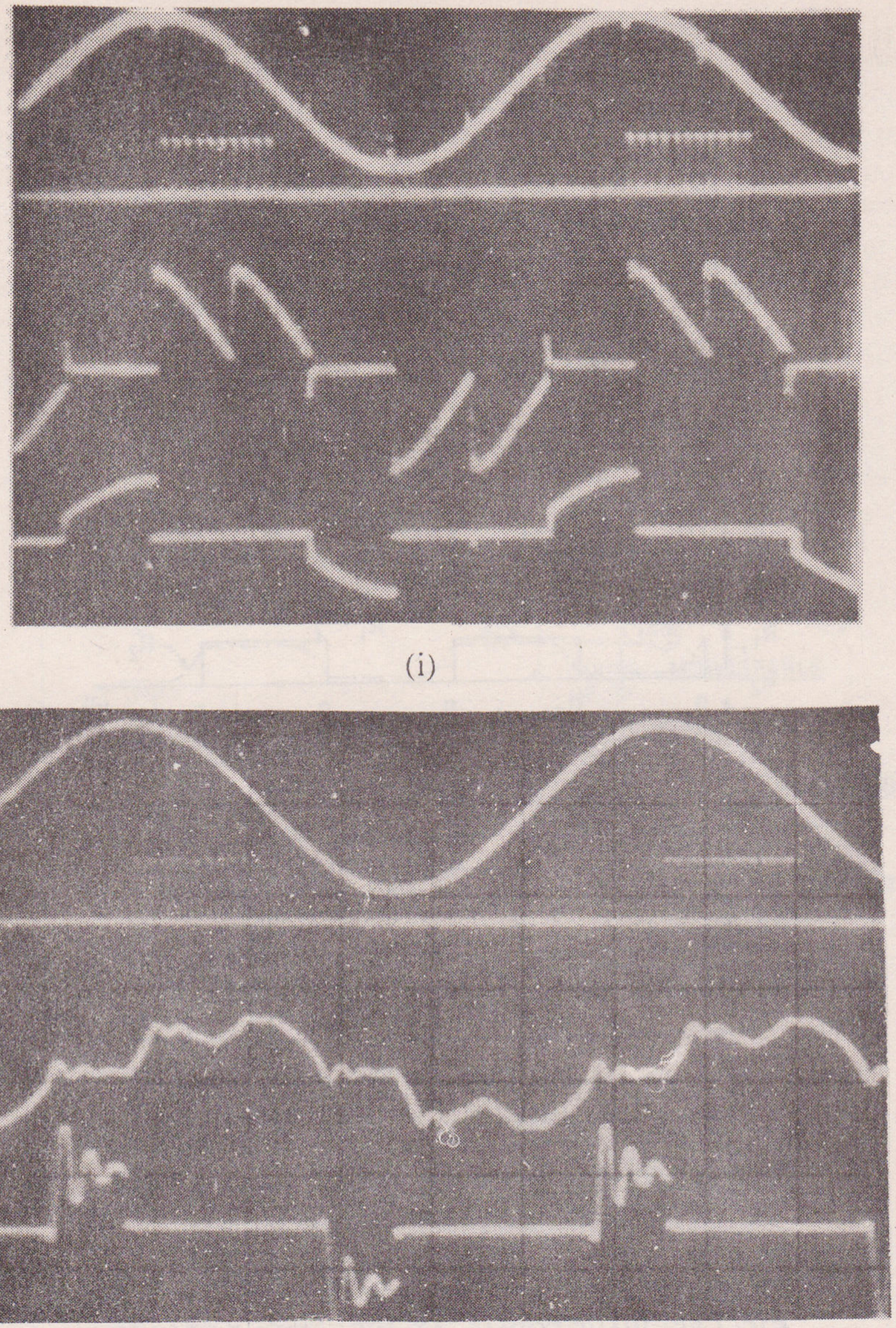


FIG. 4·86: WAVEFORMS AT DIFFERENT STAGES OF FIG. 4·85



(i)

(ii)

FIG. 4.87 : OSCILLOGRAMS OF THREE-PHASE AC REGULATOR FOR α (TRIGGERING ANGLE) $\simeq 90^\circ$
(I) R-PHASE LINE VOLTAGE e_R, TRIGGERING PULSE G_1, R-PHASE LOAD CURRENT AND R-PHASE THYRISTORS PAIR VOLTAGE WAVEFORMS FOR STAR ($\curlyvee$) CONNECTED THREE-PHASE RESISTIVE LOAD
(ii) R-PHASE LINE VOLTAGE e_R, TRIGGERING PULSE G_1, R-PHASE LOAD CURRENT AND R-PHASE THYRISTOR VOLTAGE WAVEFORMS FOR DELTA (Δ) CONNECTED THREE-PHASE SQUIRREL-CAGE INDUCTION MOTOR LOAD.

QUESTIONS

17.1 Draw and explain any one phase current waveforms of the three-phase ac regulator connected with a three-phase *Y*-connected resistive load for the triggering angles 30°, 60°, 120° and 150°.

17.2 Draw and explain the triggering pulses and the circuit diagram of the three-phase ac regulator using triacs.

17.3 Design and explain a simple triggering circuit with block diagram, circuit diagram and waveforms at some important points of the circuit, for three-phase ac regulator using triacs.

17.4 Can we use ac regulator as a starter for induction motor ? If yes, then explain how does it work as a starter and what are the advantages of an ac regulator controller starter over conventional starter ?

17.5 Draw and explain the circuit diagram of the ac voltage regulator controller starter with a three-phase squirrel cage induction motor and a slip-ring induction motor.

APPENDIX 1

GENERAL INSTRUCTIONS

(a) RATING SELECTION OF POWER SEMICONDUCTOR DEVICES, APPARATUS AND ITS PROTECTION DEVICES

Selection of the proper type and range of power semi-conductor devices (e.g., Thyristors, GTO thyristors, Power Transistors, Triacs, MOSFETs and Power Diodes, etc.) and apparatus is of utmost importance. So that, the circuit can work satisfactorily without any damage to the apparatus and components.

1. Semiconductor Devices

The rating of the semiconductor devices (e.g., current, forward voltage, reverse voltage and temperature ratings, etc.) should be at least 50 per cent more than the required rating value of the semiconductor devices in the circuit.

2. Instruments

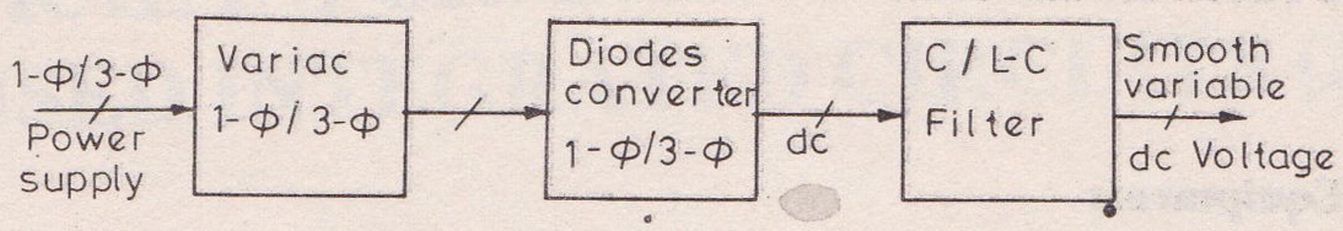
The input voltage rating of the multi beams (at least dual beam) oscilloscope should be at least 10 per cent more than the highest value of the voltage to be measured. If the measured voltage value is higher than the oscilloscope range, then 10:1 probe are used. It is better to use differential oscilloscopes. If differential oscilloscope is not available, the oscilloscopes can be electrically isolated from the power converter and its control circuit with the help of 1:1 isolation transformer. This isolation or differential feature allows the observation of waveform between any two points of the power circuit. In the absence of any of these features waveforms of any point w.r.t. earth can only be observed.

The rating of the other instruments, such as ammeters, voltmeters and ohm-meteres, etc., should be at least 25 per cent more than the maximum value of the quantity to be measured.

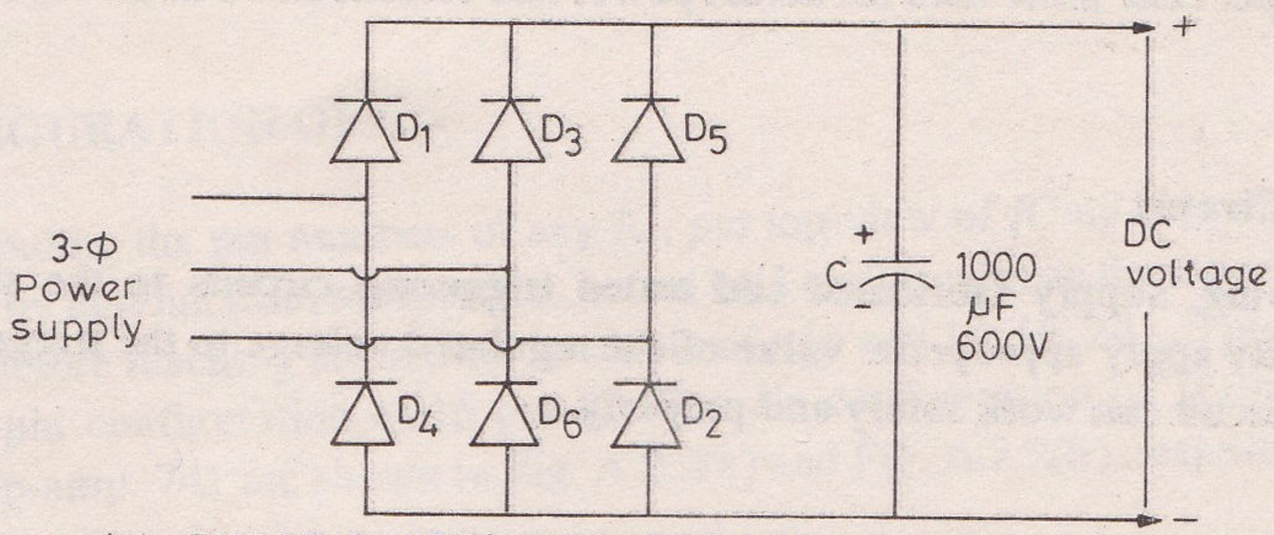
3. Converter Power Supply

Generally, the single-phase 220 volts, three-phase 440 volts and 220 volts dc isolated power supplies of high power rating should be available in the each working-table of the lab. Sometimes less voltage than the above written voltage is also used due to the lack of availability of the semiconductor devices of the required voltage rating.

The variable ac voltage can be obtained with the help of a variac (autotransformer), step-down voltage transformer and ac regulator, etc. If the required dc voltage supply is not available then use any one circuit from Fig. A.1.1 to Fig. A.1.3 for getting variable dc voltage supply.



(a) SINGLE LINE BLOCK DIAGRAM



(b) THREE-PHASE UNCONTROLLED CONVERTER WITH CAP.-FILTER

FIG. A.1.1 : METHODS OF GETTING VARIABLE DC VOLTAGE FROM FIXED 1-PHASE / 3-PHASE AC SUPPLY (I - METHOD)

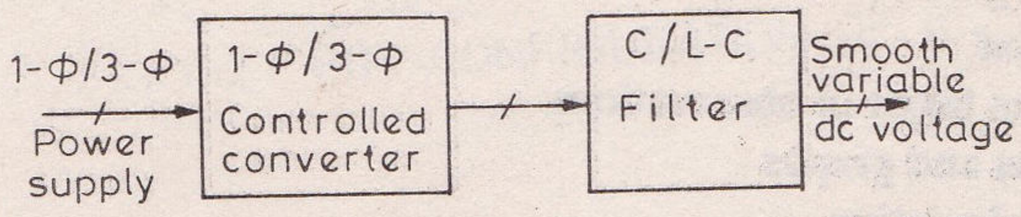


FIG. A.1.2 : SINGLE LINE BLOCK DIAGRAM FOR GETTING VARIABLE DC VOLTAGE FROM FIXED 1-Φ/3-Φ AC SUPPLY (II - METHOD)

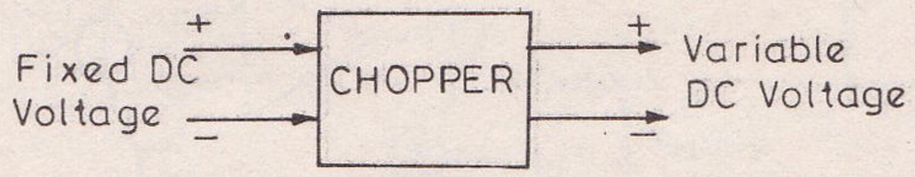


FIG. A.1.3 : METHOD OF GETTING VARIABLE DC VOLTAGE FROM FIXED DC VOLTAGE

The power rating of the variac, converter, ac regulator and chopper should be at least 50 per cent more than the maximum power drawn from them.

For the safety of the semiconductor devices, instruments and circuit, connect appropriate rating of fuses and circuit breaker in the circuit wherever there is a possibility of accidental flow of over current.

4. Loading Equipments

The power and current rating of the loading equipmcnts (rheostats, Inductors and motors, etc.) should be at least 20 per cent more than the actual power and current flows in the loading equipments in the circuit.

5. Triggering Circuit

For time saving, supply fabricated and tested triggering circuits to the students for lab experiments. Carefully apply appropriate value of the regulated voltage to the triggering circuit, so that, the triggering circuit can work safely and properly.

(b) REPORT WRITING AND SOME SUGGESTIONS

The students should come to the laboratory well prepared about the experiment to be conducted. While this will permit them to complete the experiment well within time, it will also prevent damage to the equipment due to wrong handling.

The report may be written under following distinct heads :

1. Objective of the experiment
2. Apparatus with ratings
3. Circuit diagram
4. Observation
5. Precautions taken in observations
6. Waveforms and graphs
7. Sample Calculation
8. Result
9. Discussion and Conclusions

APPENDIX 2

GENERAL INFORMATION FOR COMMONLY USED INTEGRATED CIRCUITS (*ICs*)

PIN CONFIGURATION OF *ICs*

For finding the pin numbers of any *IC*, put top-view of *IC* up-side and start to marking pin No. 1, 2, 3, ... by moving from Marker (i.e., cutted half-circle or dot on the top-view) in anti-clockwise. The last pin before reaching the marker is *n*th pin of *n* (*n* = 8, 14, 16, 24, ...) pins *IC*. Fig. A.2.1 shows how to find pin configuration of 16 pin *IC*. The pin configuration of TO-package and chip (flat) package of op-amp. 741 are shown in Fig. A.2.2(a) and Fig. A.2.2(b), respectively.

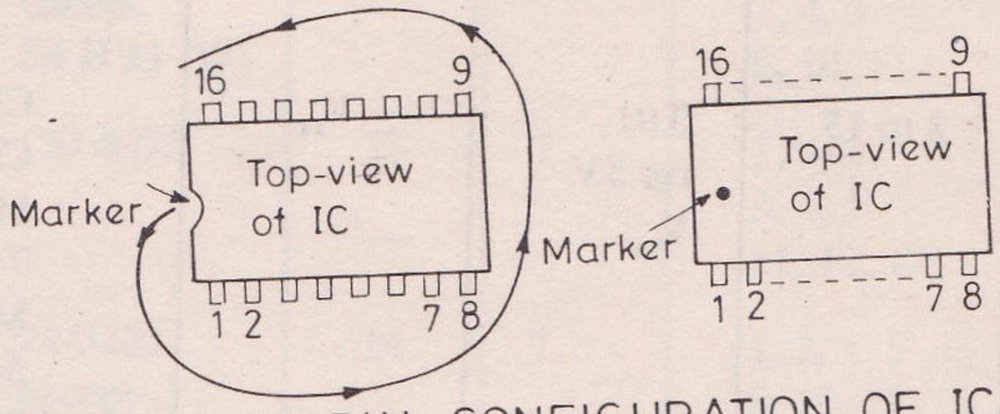
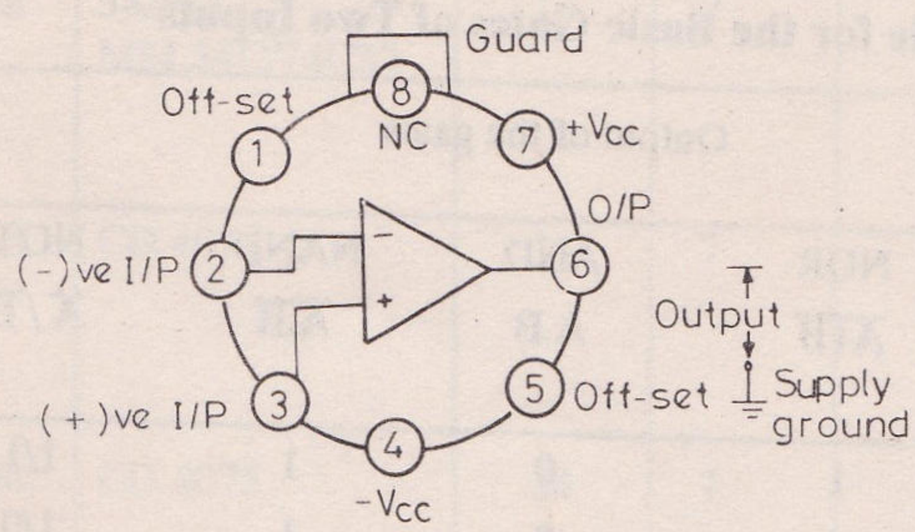
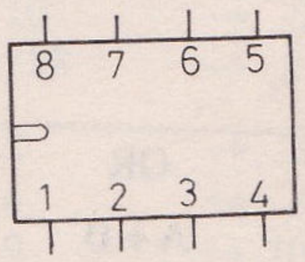


FIG. A.2.1: PIN CONFIGURATION OF ICs



(a) TOP-VIEW OF TO-PACKAGE



(b) TOP-VIEW OF FLAT (CHIP)-PACKAGE

FIG. A.2.2: PIN CONFIGURATION OF OP-AMP. 741

Table A. 2.1

Specifications of DTL, HTL, TTL and CMOS Logic ICs

	Logic	V_{cc} in Volts	Input Voltage		Series Number	Remark
			Low (0) Level Max. V	High (1) Level Min. V		
1.	DTL (Diode-Transistor Logic	5 ± 0.5	0.4	2.5		Generally not used due to lower Fan-out*
2.	TTL (Transistor-Transistor Logic)	5 ± .25 5 ± 0.5	0.4 0.4	2.4 2.4	SN 74 SN 54	Fan-ou t ≃ 10
3.	HTL (High Threshold Logic)	15 ± 1	1.5	13.5	MC6	Good for Power electronics applications due to high noise immunity (≃ 5V) but high cost and lower speed, fan-out ≃ 10
4.	CMOS Complementary Metal-oxide Logic)	3 to 15	0.01 for 5V V_{cc}	≃ V_{cc}	CD 40, CD 45, MM/NM 74C, MM/NM 54 C	Draw low power from supply, sink current 0.4 to 0.8 mA and fan-out ≃ 50

* Fan-out (or loading factor) : The number of same logic loads a particular logic device can feed reliably.

Table A. 2.2

Truth Table for the Basic Gates of Two Inputs

Input Variables		Output of the gates					
A	B	OR A + B	NOR $\overline{A+B}$	AND A.B	NAND $\overline{A.B}$	NOT $\overline{A}$ / $\overline{B}$	EX.–OR A ⊕ B = $A\overline{B} + \overline{A}B$
0	0	0	1	0	1	1/1	0
0	1	1	0	0	1	1/0	1
1	0	1	0	0	1	0/1	1
1	1	1	0	1	0	0/0	0

Table A. 2.3

ICs Function and Number of Popular TTL and CMOS Logic

Function		Devices Nos.	Pin Assignments			
			V_{cc}	Ground	Inputs → Output	Other pins
	AND Gates					
1.	Quad 2-input	54/7408 54C/74C08	14	7	1, 2 → 3; 4, 5 → 6; 9, 10 → 8; 12, 13 → 11	
2.	Quad 2-input open collector outputs	54/7409	14	7	– do –	
3.	Quadruple 2-input AND (Buffered)	CD 4081	14	7	1, 2 → 3; 5, 6 → 4; 8, 9 → 10; 12, 13 → 11	
4.	Triple 3-input	(a) 54/7411 except 54 H 11 (W)	14	7	1, 2, 13 → 12; 3, 4, 5 → 6; 9, 10, 11 → 8;	
		(b) CD 4073	14	7	1, 2, 8 → 9; 3, 4, 5 → 6; 11, 12, 13 → 10	
5.	Dual 4-input	(a) 74/5421 except 54H21 (W)	14	7	1, 2, 4, 5 → 6; 9, 10, 12, 13 → 8	3, 11 → NC*
		(b) CD4082	14	7	2, 3, 4, 5 → 1; 9, 10, 11, 12 → 13	6, 8 → NC
	OR Gates					
1.	Quad 2-input	54/5432, MM 54C/74C32	14	7	1, 2 → 3; 4, 5 → 6; 9, 10 → 8; 12, 13 → 11	
2.	Quad 2-input (Buffered)	CD 4071	14	7	1, 2 → 3; 5, 6 → 4; 8, 9 → 10; 12, 13 → 11	
3.	Triple 3-input (Buffered)	CD 4075	14	7	3, 4, 5 → 6; 1, 2, 8 → 9; 11, 12, 13 → 10	

	Function	Devices Nos.	Pin Assignments			
			V_{cc}	Ground	Inputs →Output	Other pins
4.	Dual 4-input (Buffered)	CD 4072	14	7	2, 3, 4, 5 → 1; 9, 10, 11, 12 → 13	6, 8 → NC
	NAND Gates					
1.	Quad 2-input	(a) 54/7400 except 5400 (W, T); MM54C00; MM74C00	14	7	1, 2 → 3; 4, 5 → 6; 9, 10 → 8; 12, 13 → 11	
		(b) CD 4011	14	7	1, 2 → 3; 5, 6 → 4; 8, 9 → 10; 12, 13 → 11	
		(c) 5400 (W); 54H00(W); 54L00 (T)	4	11	1, 2 → 3; 6, 7 → 5; 9, 10 → 8; 12, 13 → 14	
2.	Quad 2-input with open collector	(a) 5401 (W); 54H01 (W); 54L01 (T)	4	11	– do –	
		(b) 5401 (J); 7401; 54/74LS01	14	7	2, 3 → 1; 5, 6 → 4; 8, 9 → 10; 11, 12 → 13	
		(c) 54H01 (J) 74H01	14	7	1, 2 → 3; 4, 5 → 6; 9, 10 → 8; 12, 13 → 11	
		(d) 54/7403	14	7	– do –	
3.	Triple 3-input	(a) 54/7410 except 5400 (W &T); MM54C/74C10; 54/7412 (open collector)	14	7	1, 2, 13 → 12; 3, 4, 5 → 6; 9. 10, 11 → 8	
		(b) 5410 (W); 54H10 (W); 54L10 (T)	4	11	1, 2 14 → 3; 6, 7, 8 → 5; 9, 10, 12 → 13	
		(c) CD4023	14	7	1, 2, 8 → 9; 3, 4, 5 → 6; 11, 12, 13 → 10	

	Function	Devices Nos.	Pin Assignments			
			V_{cc}	Ground	Inputs → Output	Other pins
4.	Dual 4-input	(a) 7420; 5420 (except 54 series given in 4b); 54/7422 open collector); 54/7413 (Schmitt Trigger); (MM54C/74C20 54/7440 [buffer; except 5440 (W) and 54H40 (W)]	14	7	1, 2, 4, 5 → 6; 9, 10, 12, 13 → 8	3, 11 → NC
		(b) 5420 (W); 54H20 (W); 54L20 (T); 54H22 (W) (open-collector) 5440 (W) and 54H40 (W) (buffer)	4	11	1, 12, 13, 14 → 2; 6, 7, 8, 9 → 10	3, 5 → NC
		(c) CD 4012	14	7	2, 3, 4, 5 → 1; 9, 10, 11, 12 → 13	6, 8 → NC
	NOR Gates					
1.	Quad 2-input	(a) 54/7402 [except 5402 (W) and 54L02 (T)]; MM54C/74C02; 54/7433 (open collector); 54/7428 (buffer)	14	7	2, 3 → 1; 5, 6 → 4; 8, 9 → 10; 11, 12 → 13	
		(b) 5402 (W); 54L02 (T)	4	11	1, 2 → 3; 6, 7 → 5 9, 10 → 8; 12, 13 → 14	
		(c) CD 4001 (buffer)	14	7	1, 2 → 3; 5, 6 → 4; 8, 9 → 10; 12, 13 → 11	
2.	Triple 3-input	(a) 54/7427	14	7	1, 2, 13 → 12; 3, 4, 5 → 6; 9, 10, 11 → 8	

Function	Devices Nos.	V_{cc}	Pin Assignments		
			Ground	Inputs → Output	Other pins
	(b) CD 4025	14	7	1, 2, 8 → 9; 3, 4, 5 → 6; 11, 12, 13 → 10	
3. Dual 3-input NOR Gates + one INVERTER	CD 4000	14	7	3, 4, 5 → 6; 11, 12, 13 → 10; Not Gate 8 → 9	1, 2 → NC
4. Dual 4-input with Strobe O/P = $\overline{St\,(A+B+C+D)}$ St : Strobe	54/7425	14	7	1, 2, 4, 5 and 3 (St) → 6; 9, 10, 12, 13 and 11 (St) → 8	
5. Dual 4-input	CD 4002	14	7	2, 3, 4, 5 → 1; 9, 0, 11, 12 → 13	6, 8 → NC
EX.–OR Gates					
Quad 2-input	(a) 54/7486 (except 54L86 (T); 54L86 (J) and 74L86); 54/74136 (open-collector)	14	7	1, 2 → 3; 4, 5 → 6; 9, 10 → 8; 12, 13 → 11	
	(b) 54L86 (T)	4	11	2, 3 → 1; 5, 6 → 7; 9, 10 → 8; 12, 13 → 14	
	(c) 54L86 (J); 74L86 (J, N) 54C/74C86; CD4030; CD4070 (buffer)	14	7	1, 2 → 3; 5, 6 → 4; 8, 9 → 10; 12, 13 → 11	
INVERTER (NOT) Gates					
1. Hex Inverter	(a) 5404 (W); 54H04 (W); 54L04 (T); 5405 (W) (open-collector)	4	11	1 → 14; 3 → 2; 5 → 6; 7 → 8; 9 → 10; 13 → 12	
	(b) 54C/74C901	14	7	2 → 1; 4 → 3; 6 → 5; 8 → 9; 10 → 11; 12 → 13	

Function	Devices Nos.	Pin Assignments			
		V_{cc}	Ground	Inputs →Output	Other pins
	(c) 54/7404 [except 5404 (W), 54H04 (W) & 54L04(T)]; 54/7405 [open-collector; except 5405 (W) & 54H05 (W)]; 54/7406 (buffer); 54/7416 (buffer); 54c/74C04	14	7	1 → 2; 3 → 4; 5 → 6; 9 → 8; 11→ 10; 13 → 12	
2. Hex-Schmitt-Trigger Inverter	54/7414; 54C/74C14; CD40106	14	7	– do –	
Buffer Gates					
(1) Hex Buffer (open collector)	54/7404; 54/7414	14	7	– do –	
(2) Hex Buffer	54/74C903	14	7	2 → 1; 4 → 3; 6 → 5; 8 → 9; 10→ 11; 12 → 13	

* NC : Not Connected.

Table A. 2.4

Commonly used Operational Amplifiers (OP-Amp) and their Pin Assignments

Functions	Op-amp IC No.	Pin Assignments								Remarks
		V_{cc} +	V_{cc} —	Inputs INV (—)	Inputs NON-INV- (+)	O/P	Offset Null	Freq. Comp.	Other Pins	
1. Low Cost, High Accuracy	AD741 Series (e.g., AD741C, 741, 741J, ... etc.)	7	4	2	3	6	1,5	—	8–NC	(1) For Off-set: Used Voltages: —V_{cc} and Pot: 10K (2) For pin config. :
2. Ultra Low bias current (0.075 pA max) FET-Input Electro-meter	AD515	7	4	2	3	6	1, 5	—	8–GND	– do –
3. Wide-band Fast-Setting FET-Input	AD3554	2	7	5	6	1	4, 8	3	—	– do –
4. Low power precission	OPA21	7	4	2	3	6	1, 5	—	8–NC	– do –
5. Wide-Temp. (–55°C–175°C), General purpose	OPA11HT	7	4	2	3	6	1, 5	—	8–NC	– do – but offset voltage : +V_{cc} and Pot : 100K
6. Low cost, General purpose	LM 107	7	4	2	3	6	—	—	5–NC	Can be connected only one bias supply :*** $V_{cc\,(max)} \simeq$ +40V or–40V

Functions	Op-amp IC No.	Pin Assignments								Remarks
		V_{cc} +	V_{cc} –	Inputs INV (–)	Inputs NON-INV (+)	O/P	Offset Null	Freq. Comp	Other Pins	
7. – do –	LM101	7	4	2	3	6	—	1, 8	5–NC	(i) – do – (ii) For Comp. : ****
8. Beets FETs on input current	LM108 (TO-Package)	7	4	2	3	6	—	1, 8	5–NC	(i) For Comp. : **** (ii) Guard→ between pin 4 and 3
9. Very high input impe-dance	LM11	7	4	2	3	6	1, 8	5	—	(i) – do – (ii) – do – (iii) For off-set.:* Used voltage : $+V_{cc}$ and Pot : 1*K*

* For Off-set : Connect variable terminal of Pot with V_{cc} ($-V_{cc}$ or $+V_{cc}$; according to given in table) and connect other Pot's terminals (fixed terminals) with "off-set Null" pins which shown in table.

** Pin Configuration of TO-Package : Put top-view of op-amp upside. Pin configuration is same as shown in Fig. A. 2.2

The pin configuration of chip (flat) package is same as other *ICs*.

*** Generally op-amp is connected with $\pm V_{cc}$ for biasing. But if required, it can be connected with only one polarity ($+V_{cc}$ or $-V_{cc}$) voltage as follows :

(i) If bias supply is positive : Connect V_{cc} and ground terminals of power supply with pin No. 7 and 4 respectively.
(ii) If bias supply is negative : Connect V_{cc} and ground terminals of power supply with pin No. 4 and 7 respectively.

**** Frequency compensation : If the frequency of the circuit is more than 2 *KHz* then connect a 30 pF capacitor between frequency compensation terminals.

O/P : Output

N C : Not connected

GND : Ground

The biasing voltage ($+V_{cc}$ and $-V_{cc}$) of different types of op-amps is given in Table A2.5.

Table A 2.5

Electrical Specifications of Op-amps

Op-amp No.	I/P Impedance Differential	Open Loop Gain	O/P Short Circuit Current	I/P Offset Voltage		I/P Offset Current		Supply Voltage (V_{cc})			I/P Voltage Max. (Typ.)		Frequency Range 0 to		Temperature Range		I/P Bias Current
	(Typ.)	(Typ.)	(Typ.)	Typ.	Max.	Typ.	Max.	Min.	Typ.	Max.	Diff.	Common Mode	Small Signal	Full Power	Min.	Max.	Max.
	MΩ		mA	mV	mV	nA	nA	V	V	V	V	V	MHz	KHz	°C	°C	mA
AD741C	2	20K	25	1	6	20	200	± 5	± 15	–	–	± 13	1	10	0	70	500
AD741	2	20K	25	1	5	20	200	± 5	± 15	–	–	± 13	1	10	–55	+ 125	500
AD741J	1	20K	25	1	3	5	50	± 5	± 15	± 18	± 30	± 15	1	10	0	70	500
AD741K	2	20K	25	0.5	2	2	10	± 5	± 15	± 22	± 30	± 15	1	10	0	70	500
AD741L	2	20K	25	0.2	0.5	2	5	± 5	± 15	± 22	± 30	± 15	1	10	0	70	500
AD741S	2	20K	25	1	2	2	10	± 5	± 15	± 22	± 30	± 15	1	10	–55	125	500
AD3554	10^5	100dB	± 125	0.5	2	10pA	50pA	± 5	± 15	± 18	± V_{cc}	± V_{cc}–4	90	19MHz	–25	85	500
AD515	10^7	20K	25	0.4	3	–	–	± 5	± 15	± 18	± 20	± 10	0.35	16	0	70	0.05 pA
LM108	70	300K	–	0.7	–	50pA	–	± 2	± 20	–	–	± 14	1	1	–	–	0.8
LM11	10^6	300K	–	0.1	–	0.5	–	± 2	± 15	–	–	–	–	–	–55	125	25 pA
OPA11HT	300	103 dB	–	± 1	± 5	± 10	± 25	–	± 8 to ± 12	± 15	± 12	± 11	10	–	–55	175	± 25 nA
OPA21	6	2K	–	40 μV	100 μV	0.3	1	± 15	± 18	–	± 12.5	–	–	–	–25	85	25 nA

I/P : Input

O/P : Output

Table A. 2.6

Flip-Flops

Function	IC No.	Pin Assignments									Function Table							
				INPUTS					OUTPUTS		INPUTS					OUTPUTS	
		V_{cc}	GND	Ist Pin J	IInd Pin K	PR	CK	CLR	Q	$\overline{Q}$	J	K	CK	PR	CLR	Q	$\overline{Q}$
1) Dual J-K Flip-Flops with clear	a) 74/5473 MM74C/54C73 except 54/74LS73A	4	11	14	3		1	2	12	13	X	X	X		L	L	H
		IInd		7	10		5	6	9	8	L	L	H		H	PR — ST	
											H	L	H		H	H	L
											L	H	H		H	L	H
											H	H	H		H	CH — ST	
	b) 54/74107 and MM54C/74C107	14	7	1	4		12	13	3	2				– do –			
		IInd		8	11		9	10	5	6							
	c) 54/74LS107A					– do –								– do – see note (1)			
											X	X	H		H	PR — ST	
	d) 54/74H103 and 54/74LS73A (–)ve edge triggered	4	11	14	3		1	2	12	13				– do –			
		IInd		7	10		5	6	9	8							
				D							D						
2) Dual D-Type (+)ve edge triggered Flip-Flops with preset and clear	a) 54/7474 and MM54C/74C74 except 5474(W) 54H74 (W) and 54L74 (T)	14	7	2		4	3	1	5	6	X		X	L	H	H	L
		IInd		12		10	11	13	9	8	X		X	H	L	L	H
											X		X	L	L	Avoid	
											H		↑	H	H	H	L
											L		↑	H	H	L	H
											X		L	H	H	PR — ST	
	b) 5474 (W), 54H74 (W) and 54L74 (T)	4	11	2		14	1	3	13	12				– do –			
		IInd		6		8	7	5	9	10							
				J	K												
3) Dual J-K Flip-Flops with Preset and clear	a) 54/7476 and 54C/74C76 except 54/74LS76A	5	13	4	16	2	1	3	15	14	X	X	X	L	H	H	L
		IInd		9	12	7	6	8	11	10	X	X	X	H	L	L	H
											X	X	X	L	L	Avoid	

APPENDIX 3

DEVICES EMPLOYED IN CONTROL AND FIRING CIRCUITS

The electronic devices which are commonly used in the control circuits of the power semiconductor converters, are briefly given here. For detail operation refer any book on electronics.

The devices commonly used in the control circuits of power semiconductor converters are operational amplifier (op-amp, 741, TL081, TL082, SN72709, etc.), *IC* timer (NE 555, 74121, etc.), PLL (Phase Locked Loop; NE565, CD4046 ICs, etc.) unijunction transistor (UJT; 2N2646, etc.), the basic digital *ICs* (gates, flip-flops, counters, etc.), optocoupler IC (6N135, 6N137, etc.), analog to digital (*A/D*) and digital to analog conversion *ICs* (DAC-100, ADC 0808, etc.), etc. The brief descriptions of some electronic devices are as follows :

1. OPERATION AMPLIFIER (Op-amp.)

The open loop gain of an op-amp. is very high ($\simeq 50K$, typical). Fig. A.3.1 shows the symbol of the op-amp. The op-amp. *IC* has the following properties:

1. Infinite input impedance (in MΩ) and zero output impedance.
2. Differential input (inverting and non-inverting terminals).
3. Infinite gain and bandwidth amplifier.
4. The output voltage can vary between $+V_{cc}$ and $-V_{cc}$ where $\pm V_{cc}$ is the biasing voltage of the op-amp.

An external feedback network is connected between output and input terminals for obtaining a desired gain.

2. TIMER IC-NE555

The block diagram of IC-NE555 is shown in Fig. A.3.2. It consists of the following devices:

1. Ist comparator has $2V_{cc}/3$ voltage at non-inverting terminal and inverting input terminal is connected with pin No. 6 (Threshold).
2. IInd comparator has $V_{cc}/3$ voltage at non-inverting input terminal and inverting input terminal is connected with pin No. 2 (Trigger).
3. A flip-flop : its output is set at high (1) when the Ist comparator has low (o) output state, (i.e., pin 6 voltage > $2V_{cc}/3$). The high state of the output of the flip-flop turns-on the discharge transistor (T_d). And the flip-flop is reset at low when the IInd comparator has low output state (i.e., pin 2 voltage < $V_{cc}/3$). This causes the T_d (discharge transistor) to turn off.

Table A. 2.7

Function and Number of Popular HTL (High Threshold Logic) ICs

	Function	Devices No.
	GATES	
1.	Expandable Dual 4-Input NAND Gate (active pullup)	MC660
2.	Expandable Dual 4-Input NAND Gate (passive pullup)	MC661
3.	Triple 3-Input NAND Gate (passive pullup)	MC670
4.	Triple 3-Input NAND Gate (active pullup)	MC671
5.	Quad 2-Input NAND Gate (passive pullup)	MC668
6.	Quad 2-Input NAND Gate (active pullup)	MC672
7.	Expandable Dual 2-Wide 2-Input AND–OR INVERT Gate (active pullup)	MC673
8.	Expandable Dual 2-Wide 2-Input AND–OR INVERT Gate (passive pullup)	MC674
9.	Quad 2-Input Exclusive–OR Gate	MC683
	FLIP-FLOPS	
1.	Dual J-K Flip-Flop	MC663
2.	Master-Slave R-S Flip-Flop	MC664
3.	Quad Latch	MC682
4.	Dual J-K Flip-Flop	MC688
	COUNTERS	
1.	Decade Counter (4 J-K Flip-Flops with additional gating)	MC 684
2.	Binary Counter (4-J-K Flip-Flops with additional gating)	MC685
	MULTIVIBRATORS	
1.	Dual Monostable Multivibrator	MC667
	PULSE STRETCHERS	
1.	Dual Monolithic Pulse Stretcher	MC675
	INVERTERS	
1.	Hex Inverter with Strobe (active pullup)	MC677
2.	Hex Inverter with Strobe (without output resistors)	MC678
3.	Hex Inverter (active pullup)	MC680
4.	Hex Inverter (open collector)	MC681
5.	Hex Inverter (high voltage, open collector, no input diodes)	MC689
6.	Hex Inverter (active pullup, no input diodes)	MC690
	DECODERS	
1.	BCD-To-Decimal Decoder-Driver	MC676
	REGISTERS	
1.	4-Bit Shift Register	MC686

Function	IC No.	Pin Assignments									Function Table						
		V_{cc}	GND	INPUTS Ist Pin J	INPUTS IInd Pin K	PR	CK	CLR	OUTPUTS Q	OUTPUTS $\overline{Q}$	INPUTS J	INPUTS K	CK	PR	CLR	OUTPUTS Q	OUTPUTS $\overline{Q}$
											L	L	H	H	H	PR	ST
											H	L	H	H	H	H	L
											L	H	H	H	H	L	H
	b) 54/74LS76A, 54H/74H106 (–)ve edge triggered					– do –					H	H	H	H	H	CH	ST
														– do – see note (1)			
											X	X	H	H	H	PR	ST
4) Dual J-K Flip-Flops with PR, common CLR and CK	a) 54H/74H78 except 54/74LS78A and 54/74L78	14	7	4	1	13	9	12	2	3	— Same as of 7476 —						
		IInd		11	8	10	9	12	6	5							
	b) 54H/74H108 (–)ve edge triggered					– do –								– do – see note (1)			
											X	X	H	H	H	PR	ST
	c) 54/74LS78 (–)ve edge triggered	4	11	3	14	2	1	5	13	12				– do –			
		IInd		10	7	6	1	5	8	9							
	d) 54/74L78					– do –											
				J	$\overline{K}$						— Same as 7476 —						
5) Dual J-$\overline{K}$ (+)ve edge triggered Flip-Flops with PR and CLR	54/74109	16	8	2	3	5	4	1	6	7	X	X	X	L	H	H	L
		IInd		14	13	11	12	15	10	9	X	X	X	H	L	L	H
											X	X	X	L	L	Avoid	
											L	L	↑	H	H	L	L
											H	L	↑	H	H	CH	ST
											L	H	↑	H	H	PR	ST
											H	H	↑	H	H	H	L
											X	X	L	H	H	PR	ST

Note : 1. (–)ve edge triggered Flip-Flop means outputs position change at the time when clock goes from (+)ve to gound (↓). Read (↓) at the place of (H) in the 'clock (CK)' column of previous Function Table.

2. In the output column of the Function Table :
PR-ST : Previous state; CH-ST : Change state (Toggle); L : Low (o); H : High (I); X : (L or H) undecided

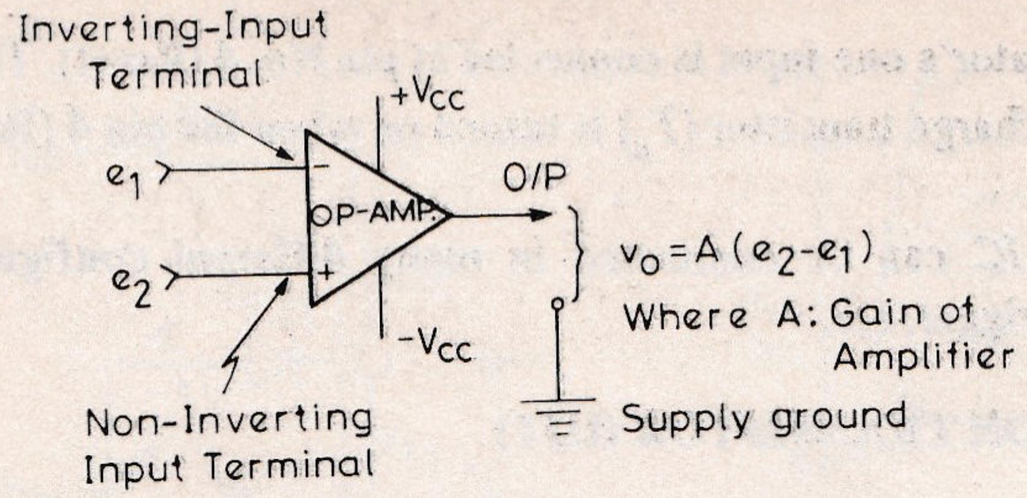


FIG. A.3·1: SYMBOL OF AN OPERATIONAL AMPLIFIER (OP-AMP.)

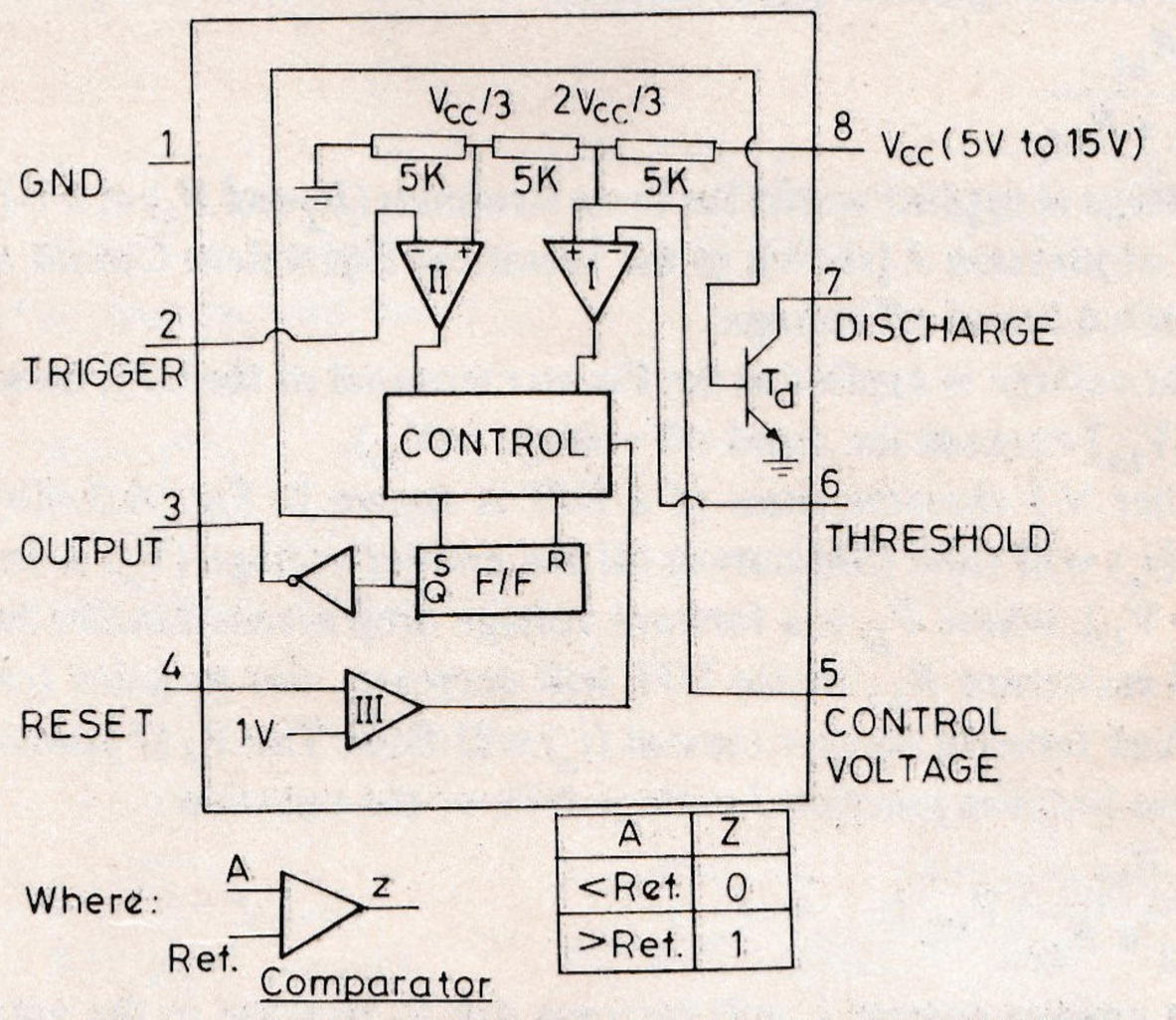
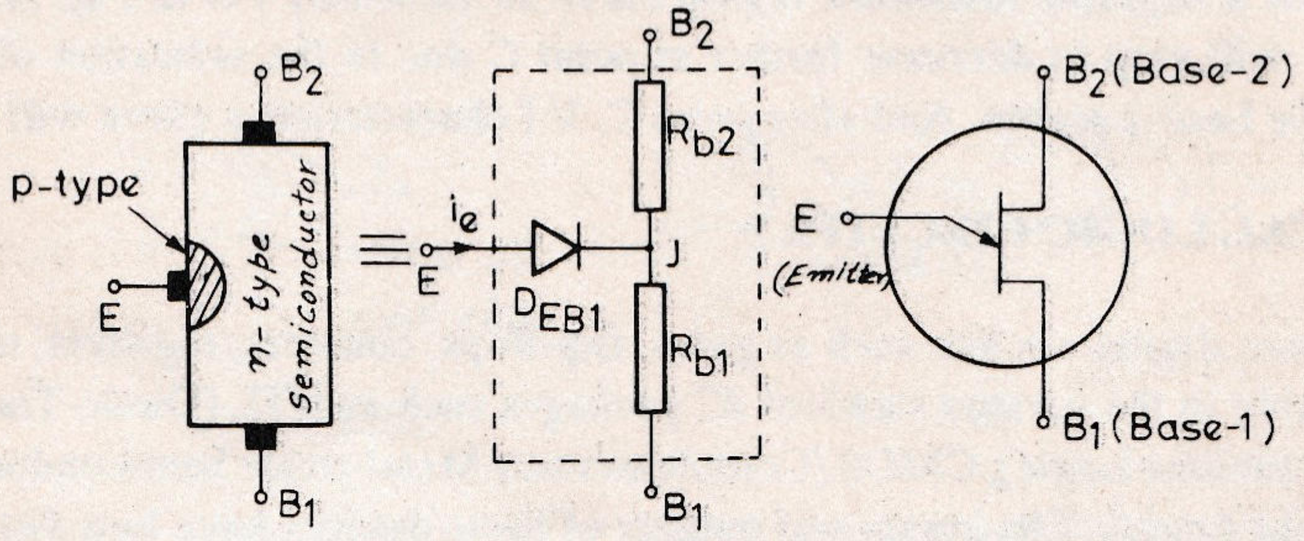


FIG. A.3·2: BLOCK DIAGRAM OF IC 555 TIMER



(a) BASIC STRUCTURE (b) ELECTRICAL EQUIVALENT CIRCUIT (c) SYMBOL

FIG. A.3·3: BASIC STRUCTURE, ELECTRICAL EQUIVALENT CIRCUIT AND SYMBOL OF A UJT

4. IIIrd comparator's one input is connected at pin No. 4 (Reset). The flip-flop can also be set high and discharge transistor (T_d) is turned on when the pin 4 (Reset) has voltage less than 1 volt.

The NE-555 *IC* can be connected in many different configurations such as astable, monostable, schmitt-trigger, etc.

3. UNIJUNCTION TRANSISTOR (UJT)

The switching time of a UJT is very low and switching action of the device can be controlled by controlling the emitter-voltage. So it is used as a relaxation oscillator. The structure, electrical equivalent circuit and symbol of a UJT circuit are shown in Fig. A.3.3.

The ratio of internal base resistance-1 (R_{b1}) to the total UJT's internal resistance ($R_{b1} + R_{b2}$), is called *Intrinsic Stand-off Ratio* (η) of the UJT.

$$\eta = \frac{R_{b1}}{R_{b1} + R_{b2}}$$

If V_{bb} voltage is applied across the main terminals (B_2 and B_1) of a UJT with emitter (E) open, then the voltage at junction J [shown in the Electrical Equivalent Circuit of Fig. A.3.3(b)] will be ηV_{bb}, which is called *Stand-off Voltage.*

If variable voltage is applied at the Emitter terminal of the UJT, then it is turned on when the emitter voltage (V_{be}) exceeds the stand-off voltage (ηV_{bb}).

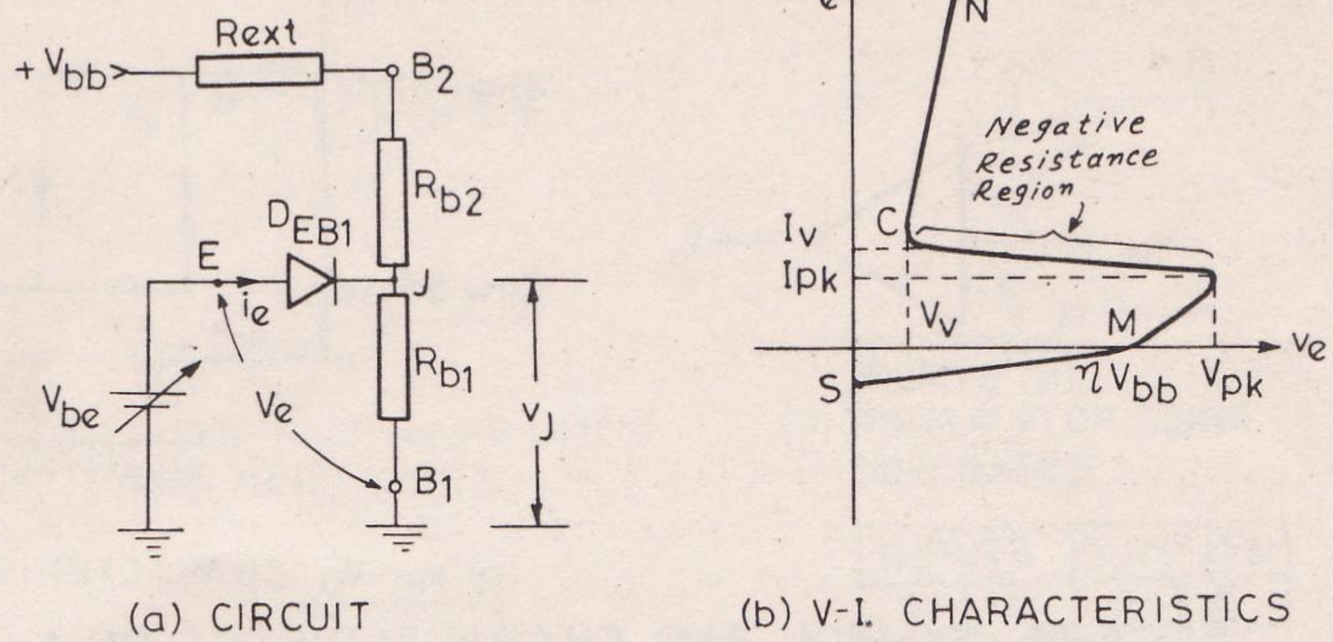
The emitter V-I characteristics of a UJT is shown in Fig. A.3.4(b). Some reverse emitter leakage current (i_e) will flow (*SM* curve) till the emitter voltage (V_e) is less than ηV_{bb}. When V_e exceeds ($\eta V_{bb} + V_D$), where V_D is a forward voltage drop across Emitter and Base-1 diode (D_{EB1}), then the internal resistance R_{b1} of the UJT will decrease due to holes (carriers) injected into the Base-1 region. And forward emitter current (i_e) will flow. The V_J (J junction voltage of UJT) will gradually decrease because junction J voltage follows the equation :

$$V_J = \frac{R_{b1}}{R_{b1} + R_{b2}} V_{bb}$$

Thus, the emitter current i_e will increase due to increase in the voltage ($V_e - V_J$). Thus, the UJT will follow a *negative resistance region curve* as shown by *PC* in Fig. A.3.4(b). The internal resistance R_{b1} will stop to decrease further at point C due to the saturation of carriers (holes and electrons) in the base-1 region. And after point C, V-I characteristics curve will follow *CN* path.

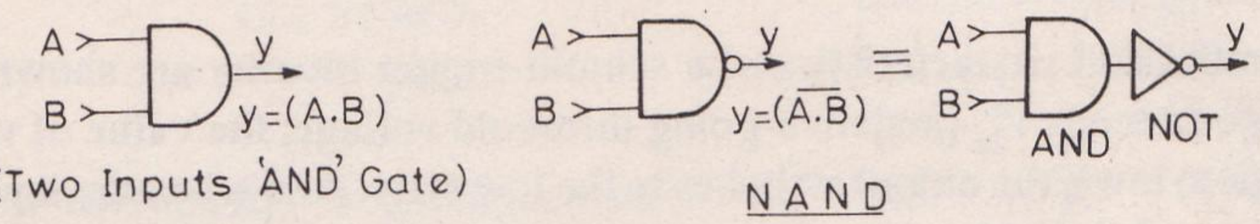
4. DIGITAL LOGIC CIRCUITS

The basic digital circuits such as gates, flip-flops, counters, registers, microprocessor chip, etc., are available in the various standard *IC* packages such as DTL (Diode-Transistor Logic), TTL (Transistor–Transistor Logic), CMOS (Complementary Metal-oxide Semiconductor Logic) and HTL (High Threshold Logic). The inputs and outputs of these devices have two distinct states: 'High or Logic one (1)' and 'Low or logic zero(0)'. The low and high voltage level of different logics are given in Table A. 2.1. The symbols of basic gates are shown in Fig. A. 3.5. The digital circuits can easily be analysed by 'Boolean Algebra'. The Boolean Algebra is based on three basic mathematical operations of the binary variables (1 and 0) called OR (+), AND (•) and NOT (–). Some basic Boolean relations are listed in Table A. 3.1.



(a) CIRCUIT (b) V-I. CHARACTERISTICS

FIG. A.3·4: CIRCUIT AND V-I CHARACTERISTICS OF A UJT



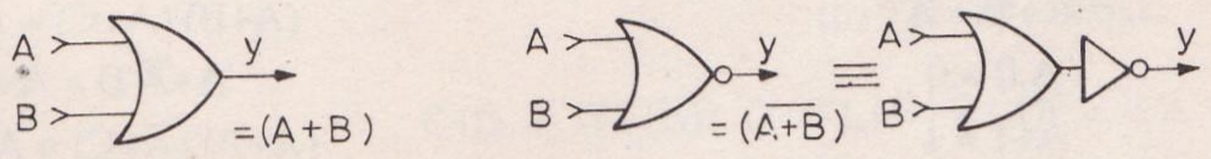


FIG. A.3·5: BASIC LOGIC GATES AND THEIR SYMBOLS

(Note: IC Packages of Basic gates come in 2-inputs, 3-inputs, 4-inputs, 8-inputs, and 12-inputs.)

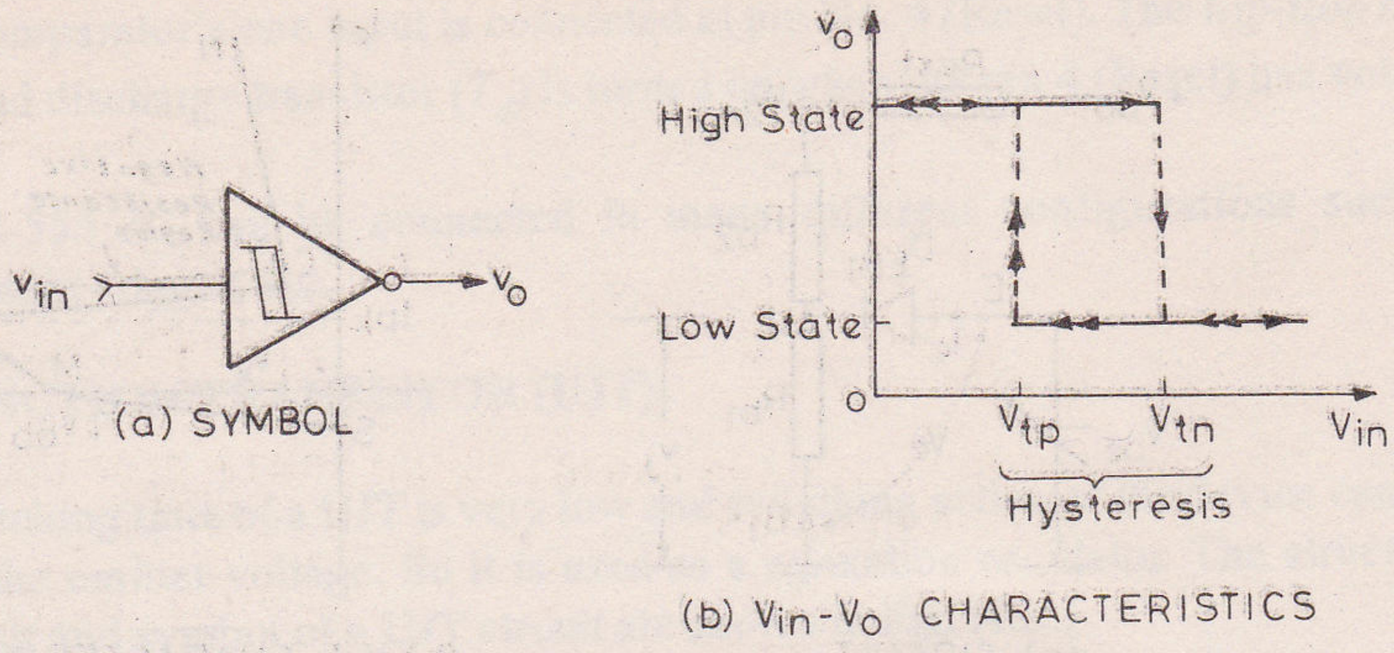


FIG. A.3·6 SYMBOL AND CHARACTERISTICS OF A SCHMITT-TRIGGER INVERTER

Schmitt-Trigger

The symbol and characteristics of a schmitt-trigger inverter are shown in Fig. A.3.6. When the input voltage exceeds V_{tn} (negative-going threshold voltage; the value of v_{in} at which the output jumps from high to low), the output switches to the low state. And when the input voltage goes below V_{tp} (positive-going threshold voltage), the output switches to the high state. The difference between two threshold voltages is called *hysteresis* (= $|V_{tn} - V_{tp}|$). The *IC* 7414 is a hex schmitt-trigger inverter.

Table A. 3.1

Some Basic Boolean Relations

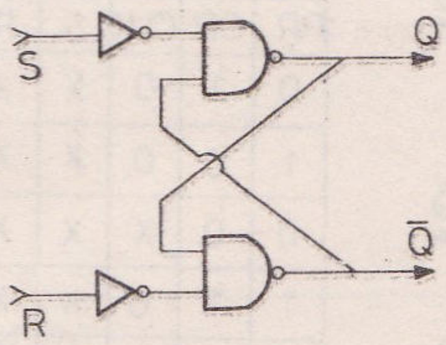
$A+A=A$	$A(A+B)=A$
$A.A=A$	$A+AB=A$
$A+0=A$	$(A+B)(A+C)=A+BC$
$A.0=0$	$A+\overline{A}B=A+B$
$A+1=1$	$(A+B)(\overline{A}+C)=AC+\overline{A}B$
$A.1=A$	
$\overline{A}+A=1$	$AB+\overline{A}C=(A+C)(\overline{A}+B)$
$A.\overline{A}=0$	$\overline{A+B}=\overline{A}.\overline{B}$ } Also called
$\overline{\overline{A}}=A$	$\overline{A.B}=\overline{A}+\overline{B}$ } DeMorgan's laws

Where A and B are binary variables '1' or '0'

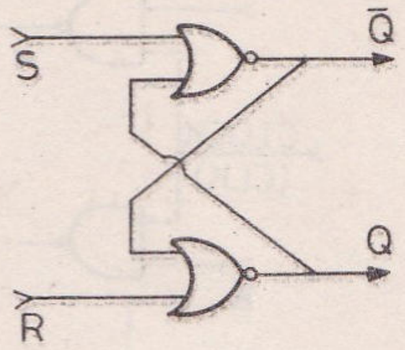
5. FLIP-FLOPS (F/Fs)

A flip-flop is also known as bistable (two stable states : low (0) and high (1) multivibrator; it holds one of these states until triggered into the other state. The flip-flops are also called memory elements of the computer.

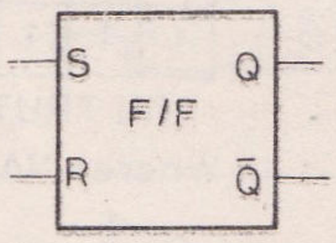
The *RS* Flip-Flop (or *RS* Latch) and D-Flip-Flop (or *D*-Latch) are the simplest flip-flops (or say 'asynchronous memory elements'). The *RS* Latch and *D*-Latch are shown in Fig. A.3.7 (a) and Fig. A.3.7(b) respectively. Generally, the synchronous flip-flops, which are simply latches with the



(i) RS-FLIP FLOP (or RS Latch) USING NAND GATES



(ii) RS-FLIP FLOP USING NOR GATES

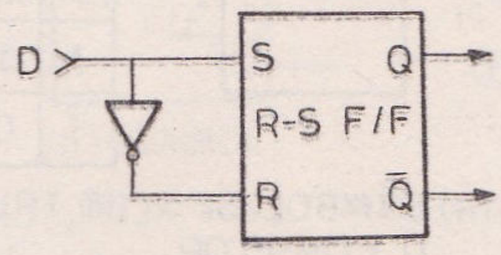


(iii) SYMBOL

INPUTS		OUTPUTS	
S	R	Q	$\bar{Q}$
0	0	Last State	
1	0	1	0
0	1	0	1
1	1	not allowed	

(iv) TRUTH TABLE

FIG. A.3.7(a) RS (Reset-Set) FLIP-FLOP WITH SYMBOL AND TRUTH TABLE

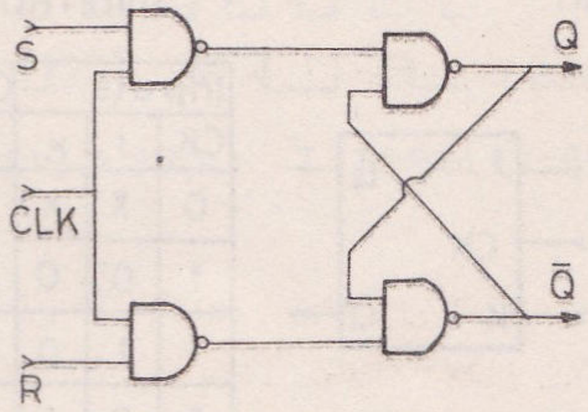


(i) SYMBOL

INPUTS	OUTPUTS	
D	Q	$\bar{Q}$
1	1	0
0	0	1

(ii) TRUTH TABLE

FIG. A.3.7(b): 'D' FLIP-FLOP

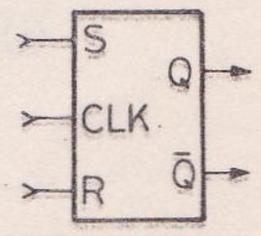


(i) CLOCKED RS FLIP-FLOP CIRCUIT

Inputs			Outputs	
CLK	S	R	Q	$\bar{Q}$
0	X	X	LAST STATE	
⎍	0	0		
⎍	1	0	1	0
⎍	0	1	0	1
⎍	1	1	NOT ALLOWED	

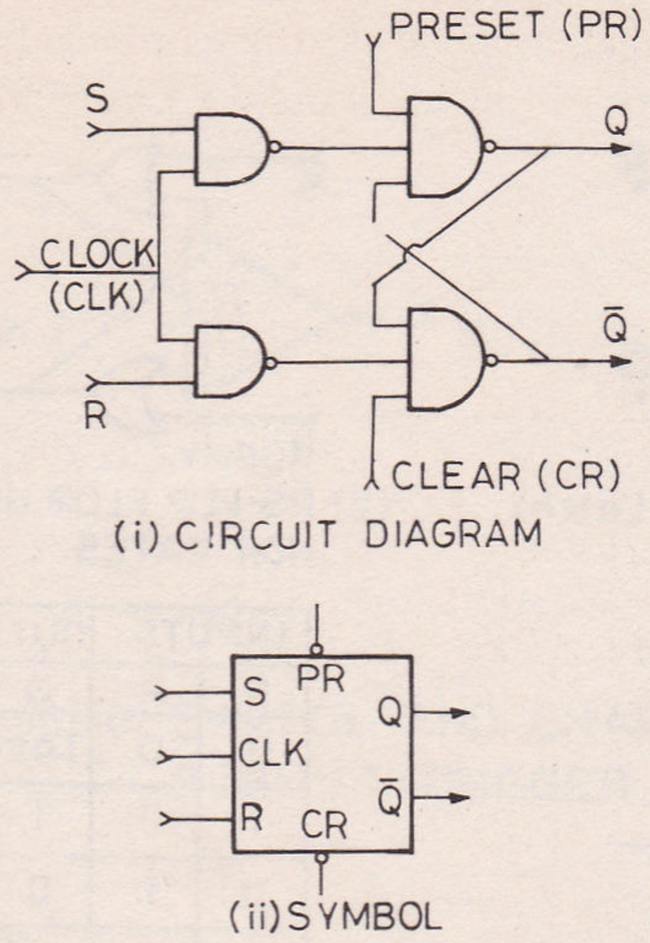
(ii) TRUTH TABLE

Where:
X = Any one state '1' or '0'



(iii) SYMBOL

FIG. A.3.7(c): CLOCKED RS FLIP-FLOP WITH TRUTH TABLE AND SYMBOL



(i) CIRCUIT DIAGRAM

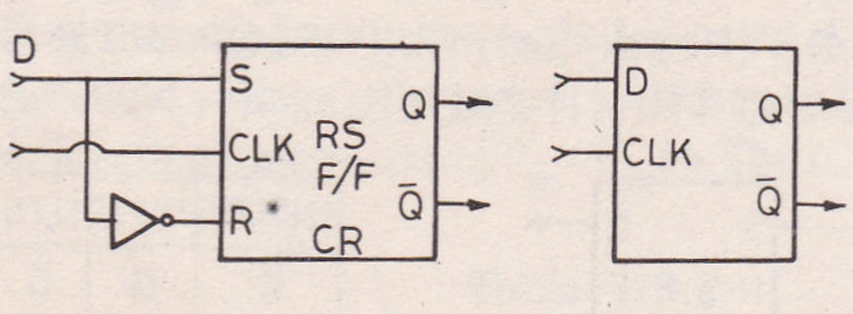
(ii) SYMBOL

Inputs					Outputs	
PR	CR	CLK	S	R	Q	$\bar{Q}$
0	1	0	X	X	1	0
1	0	0	X	X	0	1
0	0	X	X	X	NA	
1	1	0	X	X	LAST STATE	
1	1	1	0	0		
1	1	1	1	0	1	0
1	1	1	0	1	0	1
1	1	1	1	1	NA	

(ii) TRUTH TABLE

Where: NA = Not allowed

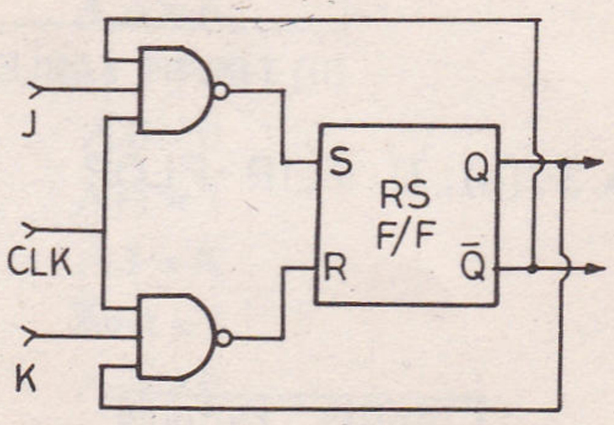
FIG. A.3·7(d): CLOCKED RS FLIP-FLOP WITH PRESET AND CLEAR



Inputs		Outputs	
CLK	D	Q	$\bar{Q}$
0	X	LAST STATE	
1	1	1	0
1	0	0	1

(i) CIRCUIT DIA. (ii) SYMBOL OF D FLIP-FLOP (iii) TRUTH TABLE

FIG. A.3·7(e): CLOCKED D (DELAY) FLIP-FLOP WITH SYMBOL AND TRUTH TABLE

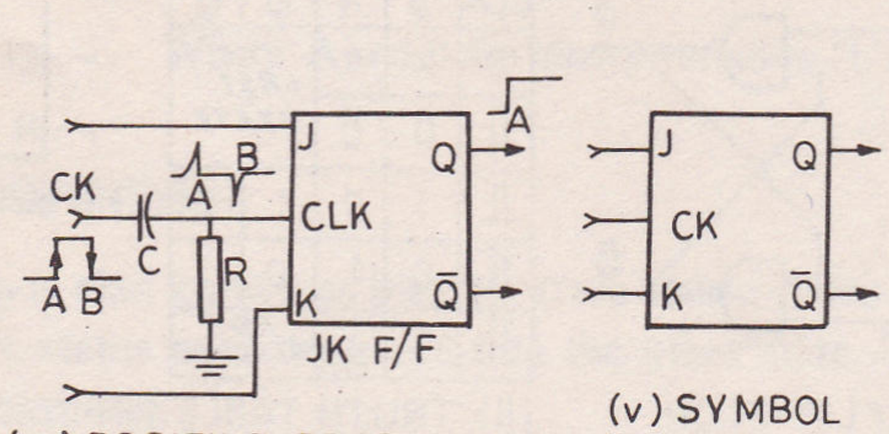


(i) JK FLIP-FLOP CIRCUIT

(ii) SYMBOL OF JK F/F

Inputs			Outputs	
CLK	J	K	Q	$\bar{Q}$
SAME AS CLOCKED RS FLIP-FLOP EXCEPT ONE STATE				
1	1	1	TOGGLE WITH RACING	

(iii) TRUTH TABLE



(iv) POSITIVE-EDGE-TRIGGERED JK FLIP-FLOP (for avoiding racing)

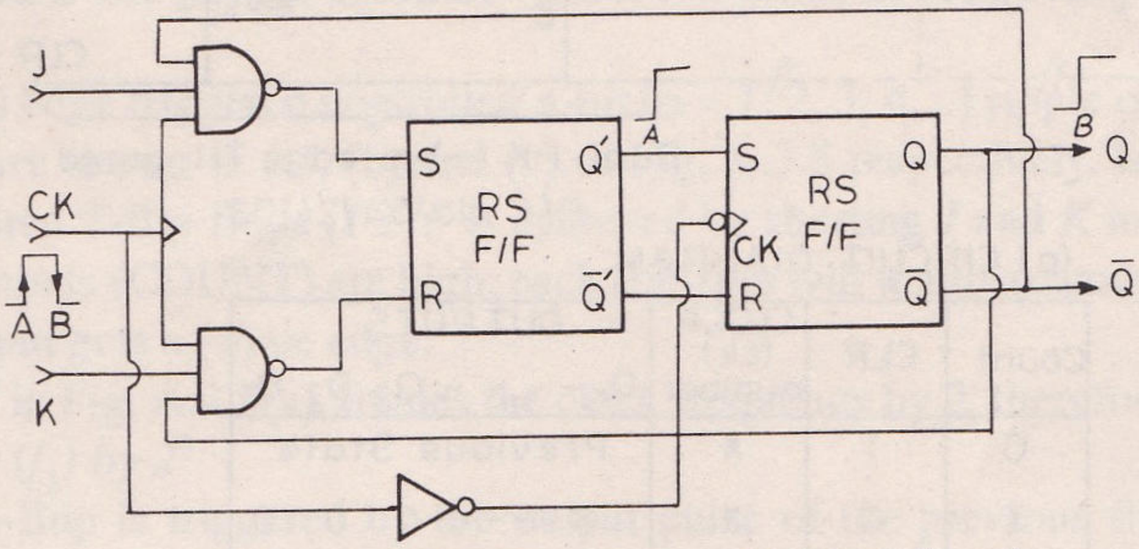
(v) SYMBOL

Inputs			Outputs	
CK	J	K	Q	$\bar{Q}$
0	X	X	LAST STATE	
↑	0	0		
↑	1	0	1	0
↑	0	1	0	1
↑	1	1	TOGGLE	

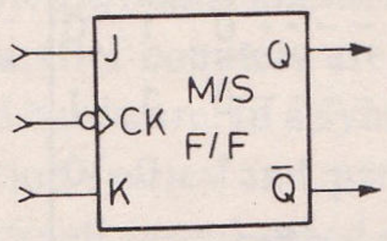
(vi) TRUTH TABLE OF EDGE-TRIGGERED JK F/F

FIG. A.3·7(f): JK FLIP-FLOP AND EDGE-TRIGGERED JK FLIP-FLOP

clocking provision added, are used. The set (S) and Reset (R) terminals are also provided with a CK (clock) terminal in a synchronous Flip-Flop, so that, it can be used synchronously or asynchronously, according to the circuit requirements. Some type of flip-flops and their truth table are given in Fig. A.3.7. (a to h).



(i) JK MASTER/SLAVE FLIP FLOP CIRCUIT

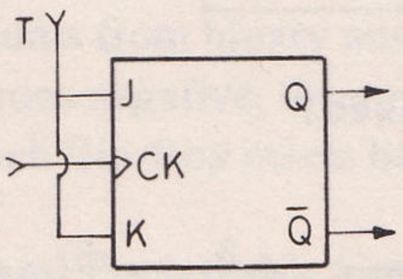


(ii) SYMBOL

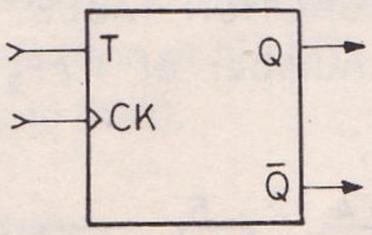
① It is also another way to avoid racing

② Truth Table: Same as for edge triggered J-K F/F

FIG. A.3.7(g): JK MASTER/SLAVE FLIP-FLOP



(i) CIRCUIT



(ii) SYMBOL

I/Ps			O/P
Previous Q	CK	T	Q
X	0	X	LAST STATE
X	1	0	
0	1	1	1
1	1	1	0

(iii) TRUTH TABLE

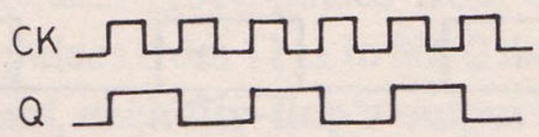
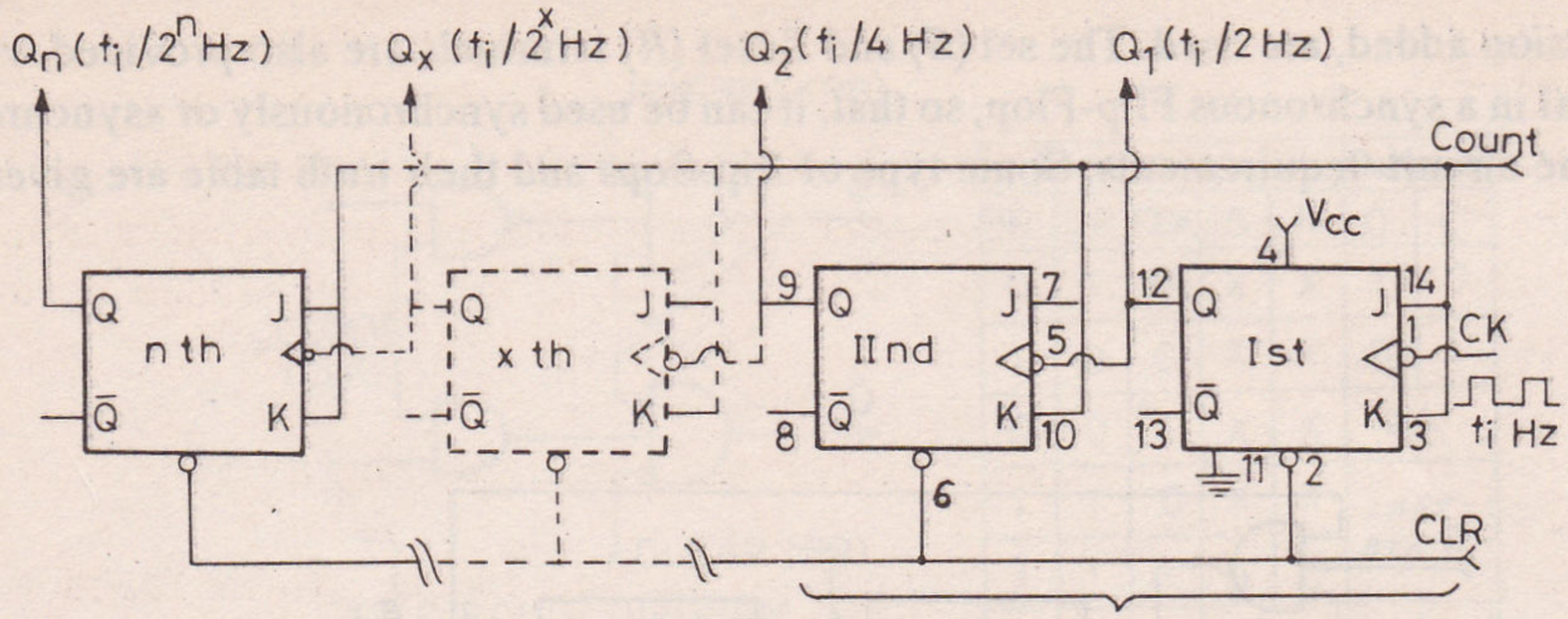


FIG. A.3.7(h): T (TOGGLE)-FLIP-FLOP



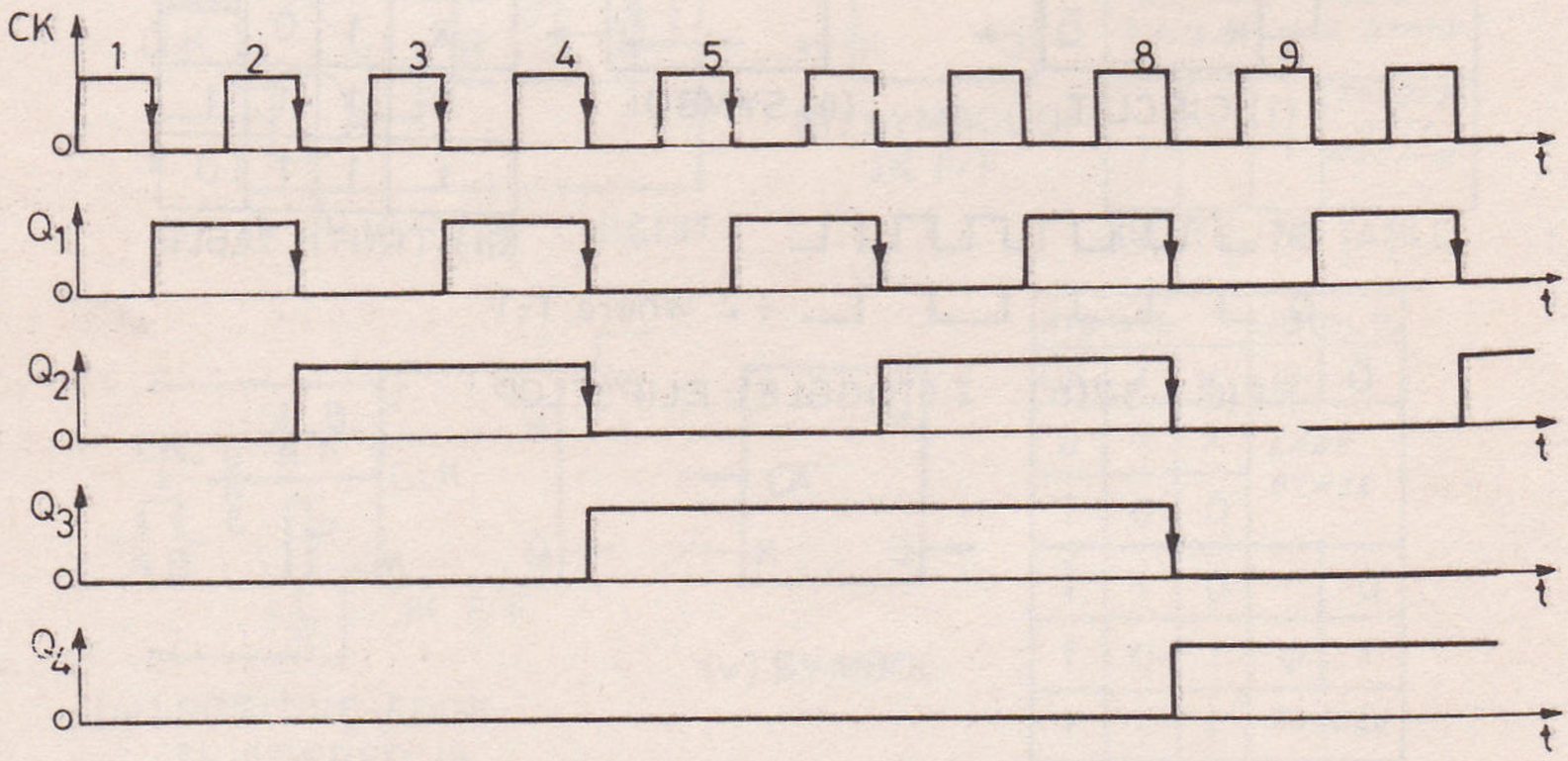
Dual J-K (-)ve edge Triggered
F/F No. 54/24103

(a) CIRCUIT DIAGRAM

Count	CLR	CLOCK (ck) number	OUTPUTS Q_n - - - - Q_3 Q_2 Q_1
0	1	X	Previous State
X	0	X	0- - - - 0 0 0
1	1	0	0- - - - 0 0 0
1	1	1(↓)	0- - - - 0 0 1
1	1	2	0- - - - 0 1 0
1	1	3	0- - - - 0 1 1
1	1	4	0- - - - -1 0 0
- - -	- - -	- - -	- - - - - - - - - - - -
- - -	- - -	- - -	- - - - - - - - - - - -
1	1	2^{n-1}	1- - - - -1 1 1
1	1	2^n	0- - - - -0 0 0

(b) FUNCTION TABLE

(Where, n: number of F/F_s used)



(c) TIMING DIAGRAM OF 4-BIT RIPPLE COUNTER

FIG. A.3.8: CONTROLLED n-BIT BINARY (OR RIPPLE) COUNTER

6. COUNTERS

A counter counts the number of clock cycles arriving at its clock input terminal. Since the frequency of the clock pulses is fixed, the counter can be used as frequency divider, an instrument for measuring time and frequency, selecting firing angle (α) of the semiconductor devices and in microcomputers.

(i) Controlled n-Bit Ripple Counter (Binary counter or frequency divider)

The (–ve) edge triggered controlled n-bit (n = 1, 2, 3, 4, ..) ripple counter, function table and timing diagram are shown in (a), (b) and (c) of Fig. A.3.8 respectively. In this ripple counter, four (–ve) edge triggered *T*-flip-flops (*T F/F* is achieved by shorting *J* and *K* inputs of *J-K F/F*) are used in cascade. If T-inputs (COUNT) are high, each flip-flop will toggle (change its previous state) when its clock (*CK*) input gets a (–) ve edge.

Each *F/F* in Fig. A.3.8(a) divides the clock frequency by 2, therefore, *n F/Fs divide the input clock freuquency* (f_1) *by* 2^n.

Each flip-flop is triggered by the output pulse of the previous flip-flop, so *nth* flip-flop's propagation delay time is the sum of the individual delays ($\simeq$ nx delay time of one *F/F*; if all *F/Fs* have equal delay time). Therefore, it limits the highest operating frequency. Such type of counters are also called *serial or asynchronous counters.*

Synchronous or parallel counters are used for increasing the speed of operation. But it is achieved with complicated hardware. In a synchronous counter, input clock pulses drive all flip-flops in parallel. The combination (series and parallel combination) counters are used to compromise between hardware in construction and speed of operation.

(ii) Decade Counter (Mod-10 counter or divided by 10-counter)

One type decade counter is shown in Fig. A.3.9. It is a 4-bit ripple counter with some modification. It counts from binary number 000 to 1001 (decimal number 0 to 9). And when the 10th input clock pulse goes negative, the combination of NAMD and AND gates generate its own low (o) clear signal and each flip-flop resets back to 0000.

(iii) Up-down and Presettable Counters

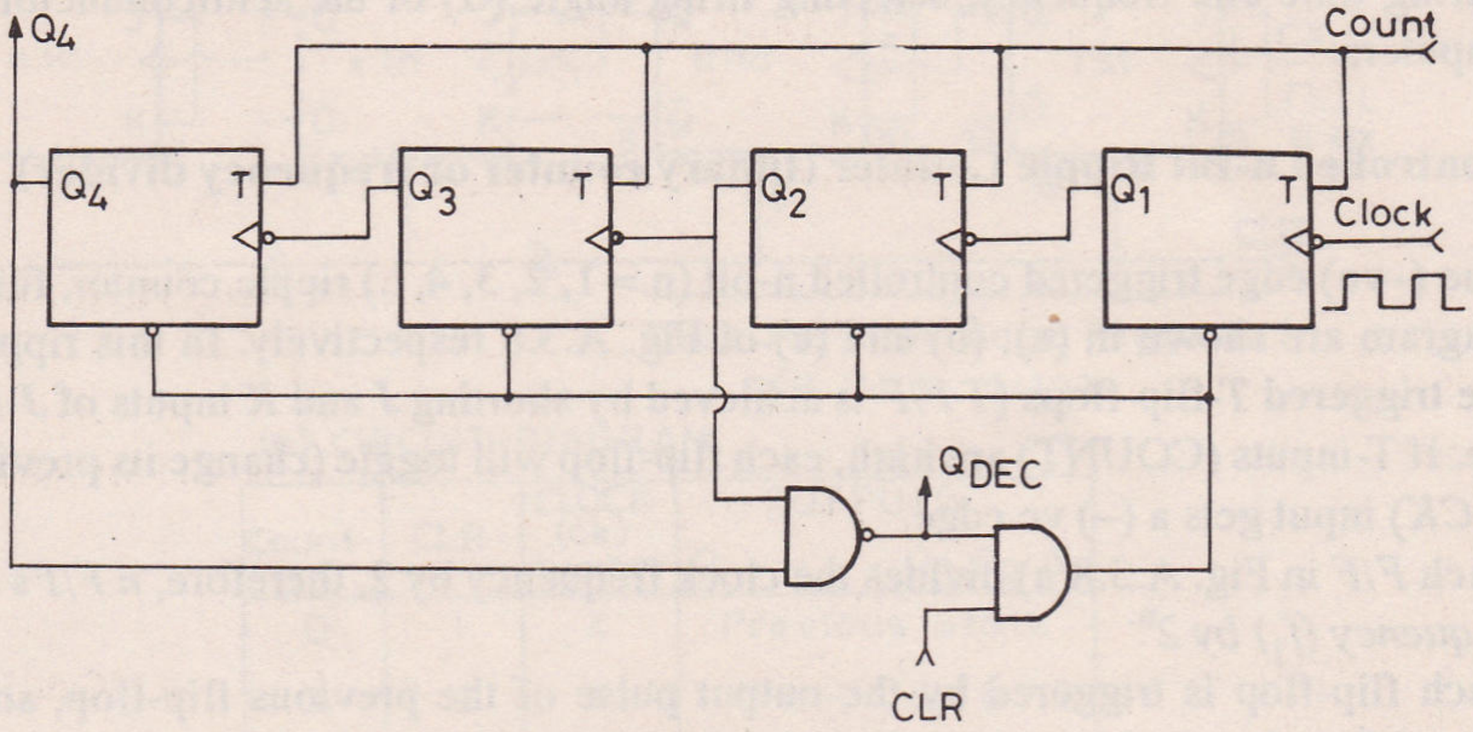
If a counter counts clock pulses from 0000 to 1111, it is called 4-bit up-counter. And if a counter counts clock pulses from 1111 to 0000 then it is called 4-bit down counter. In the down counter, before starting to count, each flip-flop's output is set high (1) by applying a pulse at preset terminal.

A 4-bit presettable counter starts to count at a number greater than zero and less than 1111. The starting number of the count $P_D P_C P_B P_A$ is loaded in the counter through preset terminals. Let preset number is

$$P_D P_C P_B P_A \quad 0111\ (7)$$

then presettable up-counter starts to count from 7 to 15 (binary 0111 to 1111). And down counter starts to count from 7 to 0 (binary 0111 to 0000).

The pin configuration and function table of the *SN* 54/74191 *IC* (Synchronous Up/Down presettable counter) are given in Fig. 4.14(c) of Experiment No. 3.4.



(a) CIRCUIT DIAGRAM

Count	CLR	Clock Pulse Number	OUTPUTS Q_4 Q_3 Q_2 Q_1 Q_{DEC}
0	1	X	Previous state
X	0	X	0 0 0 0 1
1	1	0	0 0 0 0 1
1	1	1(↓)	0 0 0 1 1
1	1	2	0 0 1 0 1
- - -	- - -	- - -	- - - - -
1	1	9	1 0 0 1 1
1	1	10(↓)	1 0 1 0 ⊓ 1 / _0
			0 0 0 0 1
1	1	11	Repeat cycle

(b) FUNCTION TABLE

FIG. A.3·9: DECADE (MOD-10) COUNTER

(iv) Counter ICs

Some commonly used counters are listed in Table A. 3.2.

Table A. 3.2

Commonly Used Counters

S.No.	Description	TTL IC No.	CMOS and HTL IC No.
Negative Edge Triggered Counters			
1.	Decade Counters	54/7490, 54/74176, 54/74196, 54/74290	54C/74C90 and MC 684 (HTL)
2.	Divided by 12-counters	54/7492	
3.	4-bit Binary counters (÷ 16 counter)	54/7493, 54/74177, 54/74197, 54/74293	54C/74C93 and MC 685 (HTL)
4.	Dual Decade	54/74390, 54/74490	
5.	Dual 4-bit Binary	54/74693	
Positive Edge Triggered Counters			
6.	Presettable Decade	54/74160, 54/74162	54C/74C160, 54C/74C162, CD40160, CD40162
7.	Presettable Decade Up/Down	54/74168, 54/74190, 54/74192	54C/74C192, CD 40192
8.	Presettable 4-Bit Binary	54/74161, 54/74163	54C/74C161, 54C/74C163, CD40161, CD40163
9.	Presettable 4-Bit Binary Up/Down	54/74169, **54/74191 54/74193	54C/74C193, CD40193

** : Pin Configuration and Function Table of 54/74191 are shown in Fig. 4.14(c) of Experiment no. 3.4.

7. PHASE–LOCKED LOOP (PLL)

NE 565 and LM 565 are PLL *ICs*. The block diagram of a PLL is shown in Fig. A.3.10(a). It consists of a double balanced phase detector, a low-pass filter, a dc amplifier and a voltage controlled oscillator (VCO). Without input signal, the error voltage V_d is equal to zero and the VCO operates at a set frequency 'f_r' which is also called free running frequency of the VCO.

Let the free-running frequency of the VCO is f_r and input signal frequency f_i is increasing from zero. If input frequency is less than F_{i1} (between F_{i0} and F_{i1}) then the error voltage V_d is equal to zero as shown in Fig. A.3.10(c) and the VCO operates at a frequency f_r. When input signal frequency f_i reaches a frequency f_{i1} (the lower edge of the capture range), then the output voltage of the detector (V_d) jumps from 0 to some –ve voltage with beat notes of frequency (difference between input signal frequency and actual VCO output signal frequency; f_i–f_o). This error voltage (V_d) is then filtered,

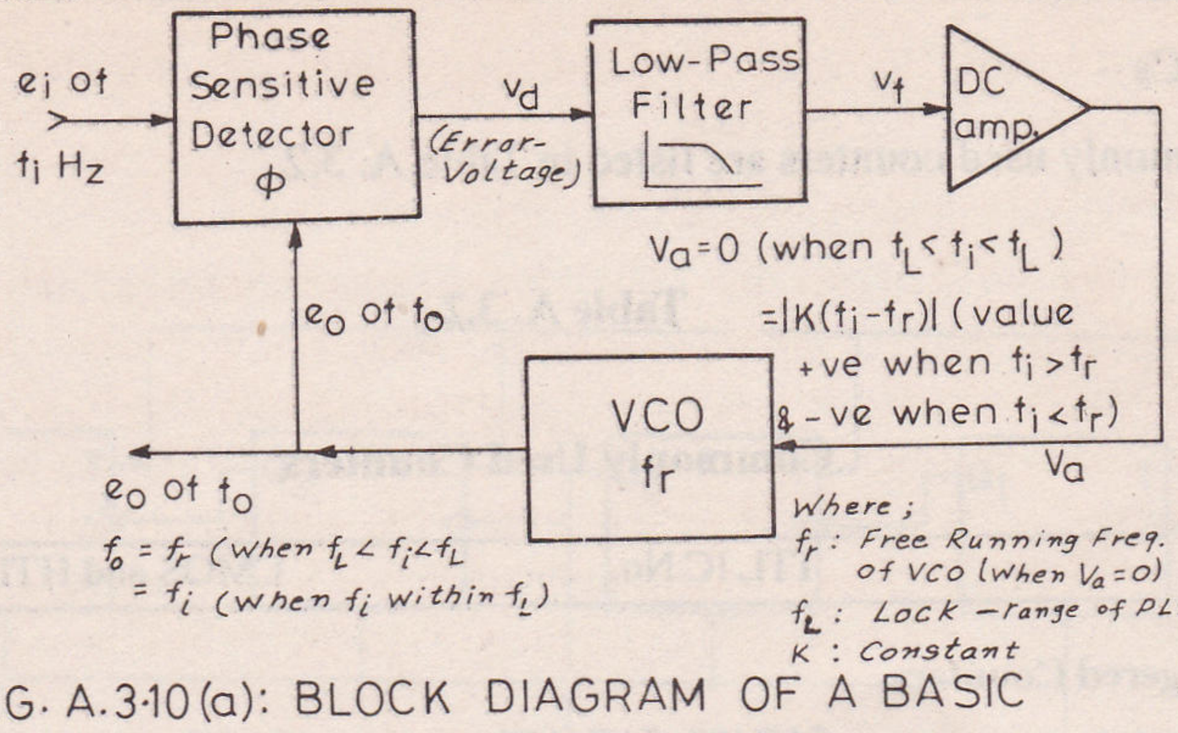


FIG. A.3·10(a): BLOCK DIAGRAM OF A BASIC PHASE-LOCKED-LOOP (PLL) IC

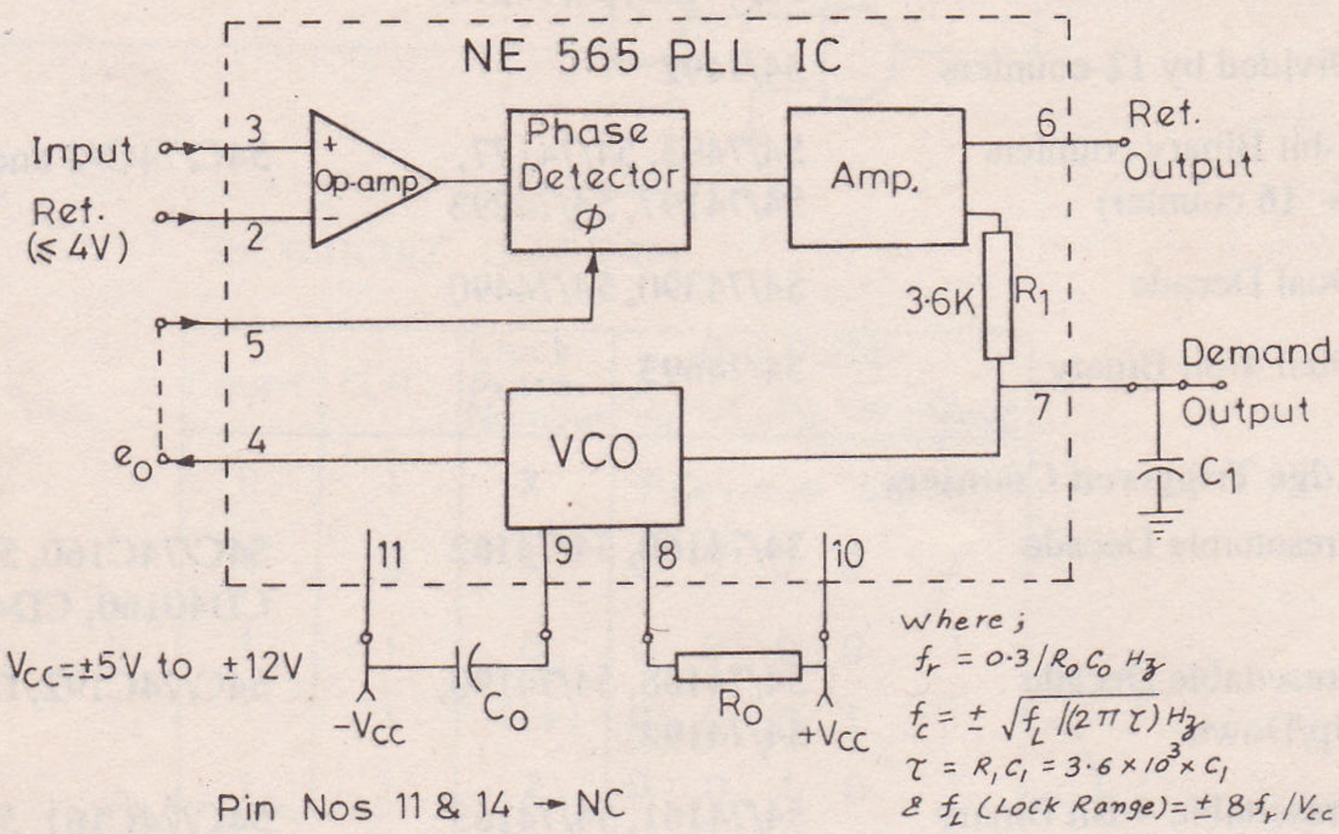


FIG. A.3·10(b): BLOCK DIAGRAM OF A NE 565 PLL IC
(R_o, C_o and C_1 are connected externally to IC

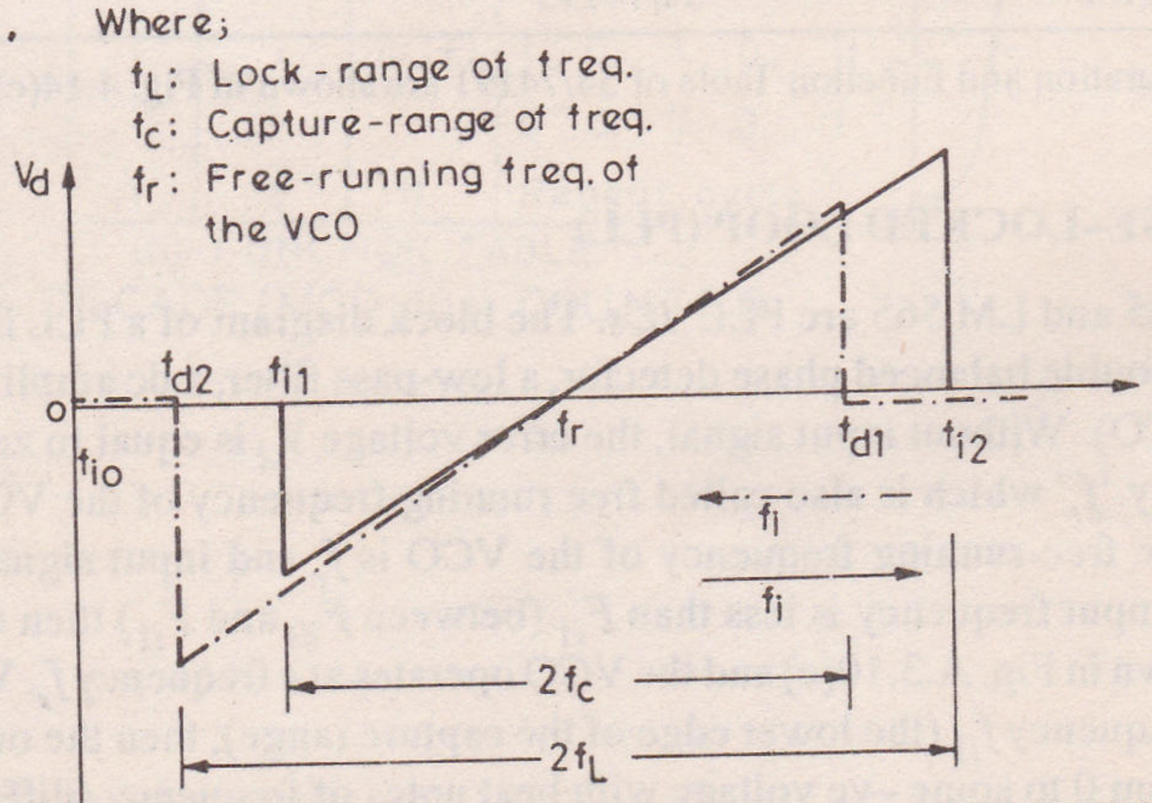


FIG. A.3·10(c): THE OUTPUT VOLTAGE (V_d) OF THE PHASE-DETECTOR WITH VARIATION OF THE FREQUENCY OF THE INPUT VOLTAGE OF PLL IC

amplified and amplified voltage 'V_a' is applied to the control terminals of the VCO. The instantaneous frequency of the VCO is decreasing because

$$f_o \text{ (output signal frequency of the VCO)} \alpha \, |V_a|,$$

but f_o falls if V_a is negative and increases if V_a is positive. At some instant of time, the falling frequency of the VCO equals f_{i1} (lower edge of the capture-range), then lock will result. And the output signal frequency of the VCO may equal to the input signal frequency (f_o=f_i). The VCO frequency locks with input signal frequency upto f_{i2} (the upper edge of the lock-range). When the input signal frequency exceeds from f_{i2} frequency then V_d falls to zero and the VCO operates at the free-running frequency (f_r) as shown in Fig. A.3.10(c). And if the input signal frequency is now slowly swept back and it reaches a frequency f_{d1}, then the loop (VCO frequency) locks on the input frequency, causing a positive jump of the error voltage (V_d). Therefore, the VCO frequency increases from f_r continuously till f_o=f_i. The VCO frequency (f_o) locks with input signal frequency (f_i) upto f_{d2} (the lower edge of the lock range) as shown in Fig. A.3.10(c) by dotted lines (–.–.–). When the input signal frequency decreases from f_{d2} frequency then the output voltage (v_d) of Phase-Detector falls to zero and the VCO operates at the free-running frequency (f_r).

The following formula hold good for PLL IC 565 (Fig. A.3.10(b) :

Free running frequency of VCO, $f_r = 0.3/R_oC_o$. Hz (1)

Lock-range, $f_L = \pm \dfrac{8f_r}{V_{cc}}$ Hz (2)

and Capture-range, $f_c = \pm \sqrt{\dfrac{f_L}{2\pi C_1 \times (3.6 \times 10^3)}}$ Hz (3)

where f_L (lock range) : The range of frequencies over which the PLL can maintain lock with the input signal frequency after lock has occurred.

f_C (capture range) : The range of frequencies over which the output signal frequency of the VCO will be able to lock with input signal frequency as shown in Fig. A.3.10(c). The capture range (f_C) is always smaller than the lock range (f_L).

Applications of PLL

PLL *IC* can be used for frequency multiplication, FM demodulation, frequency synchronisation, speed control of motors, etc. But our interest is in PLL application in Power Electronics, such as speed control of motors which is shown in Fig. A.3.11.

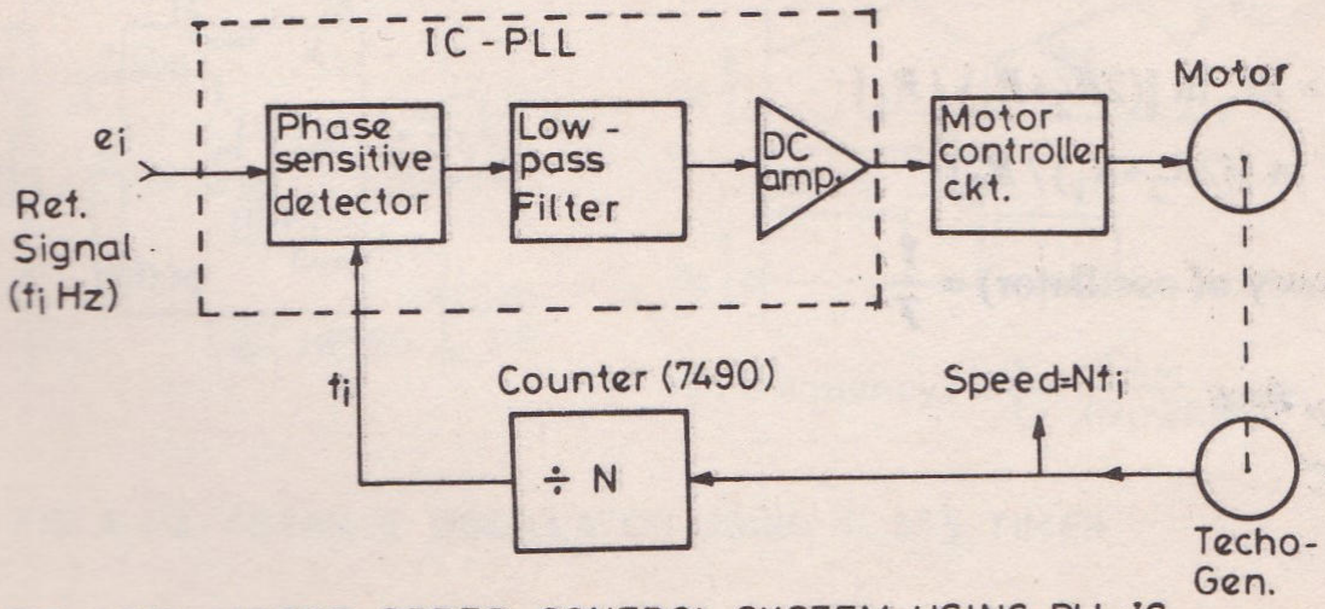


FIG-A.3-11: MOTOR SPEED CONTROL SYSTEM USING PLL IC

APPENDIX 4

CIRCUITS EMPLOYED IN CONTROL UNIT

Some electronic circuits which are generally used in the control circuits of the power semiconductor converters, are given here.

1. SQUARE WAVE OSCILLATORS (ASTABLE OR FREE-RUNNING MULTIVIBRATORS)

The oscillator has two states (high and low or ON and OFF states) but is stable in neither. In ON and OFF periods of the oscillator circuit can be varied by varying the value of circuit's components.

(i) Op-Amp. Oscillator (bias supply (V_{cc}) : ± 5V to 18V)

Fig. A.4.1 shows the Op-Amp. oscillator. Where

$$T_1 = RC \ln [(V_{OH} - V_{IL})/(V_{OH} - V_{IH})] \quad (1)$$

$$T_2 = RC \ln [(V_{IH} - V_{OL})/(V_{IL} - V_{OL})] \quad (2)$$

where V_{OH} : High-level output voltage = $+V_{cc}$

V_{OL} : Low-level output voltage = $-V_{cc}$

V_{IH} : High-level input voltage = $+\vartheta_{nt}$

V_{IL} : Low-level input voltage = $-\vartheta_{nt}$

$$V_{IH} = [R_2 / (R_1+R_2)] V_{OH} = [R_2 / (R_1+R_2)] V_{cc} \quad (3)$$

and

$$V_{IL} = [R_2 / (R_1+R_2)] V_{OL} = -[R2 / (R_2+R_1)] V_{cc} \quad (4)$$

Therefore,

$$T_1 = T_2 = RC \ln [(2R_2+R_1) / R_1] \quad (5)$$

So $$T = 2RC \ln [(2R_2+R_1) / R_2] \quad (6)$$

and $$f \text{ (frequency of oscillator)} = \frac{1}{T} \quad (7)$$

If $R_1 = R_2$, then

$$T \simeq 2RC \quad (8)$$

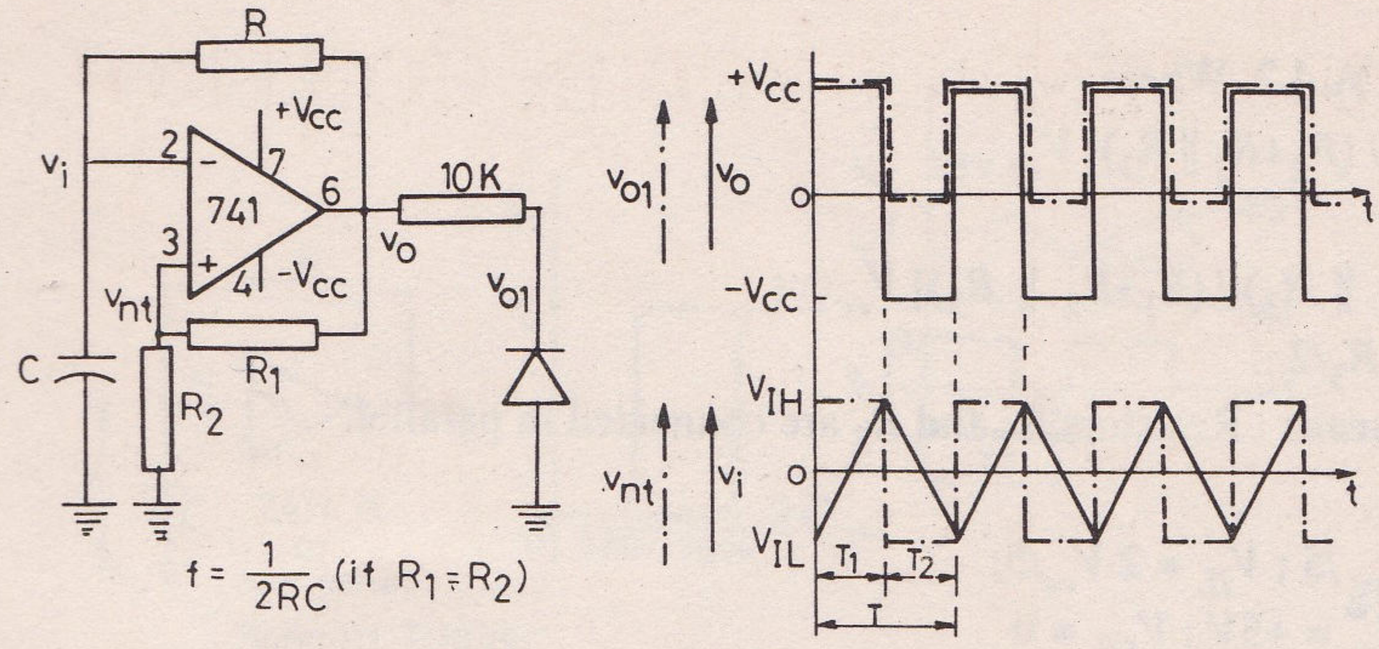


FIG. A.4·1: FREE-RUNNING SQUARE WAVE OSCILLATOR USING AN OP-AMP.

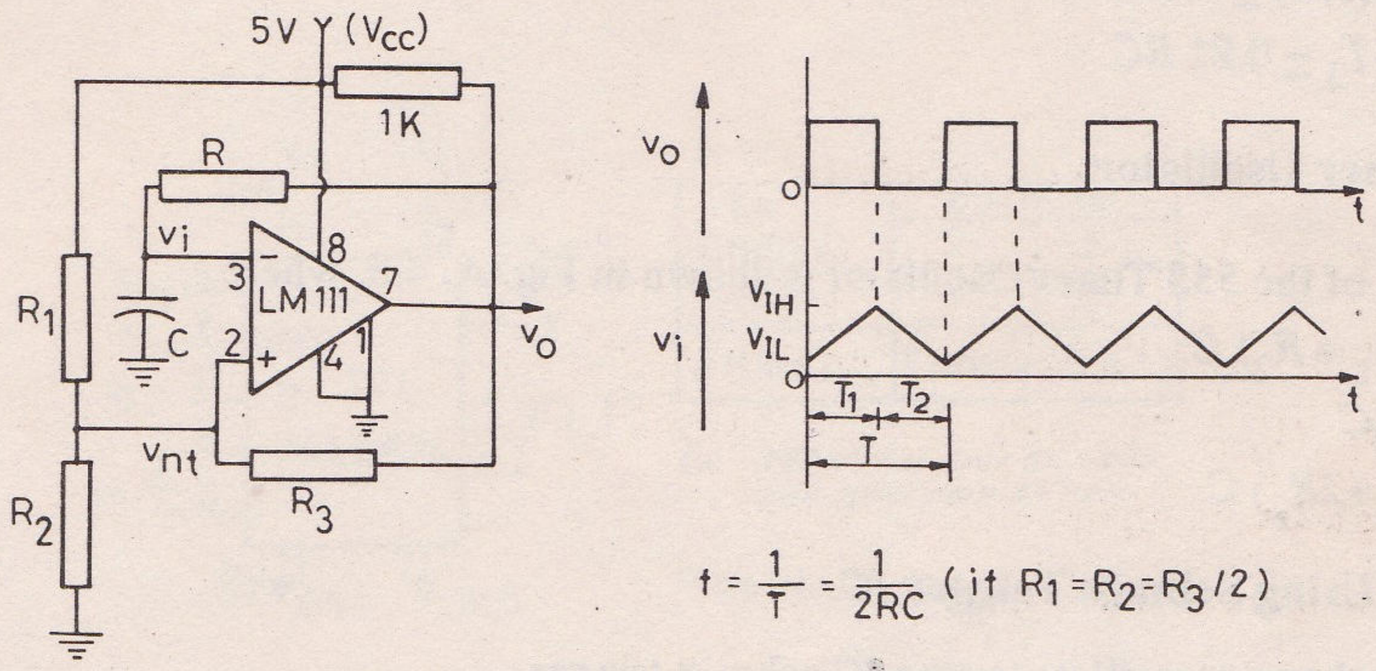


FIG. A.4·2: OSCILLATOR USING LM 111 OP-AMP.

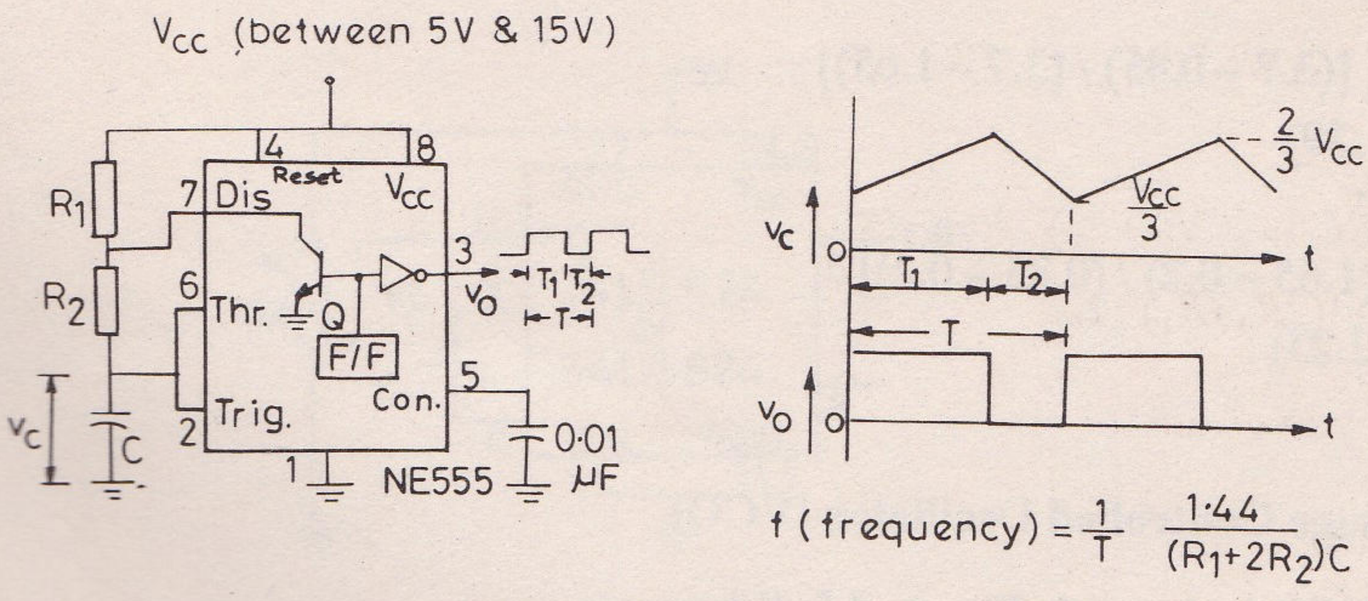


FIG. A.4·3: ASTABLE OSCILLATOR USING IC 555 TIMER

(ii) LM 111 Op-Amp. Oscillator [bias supply (V_{cc}) : + 5V or –5V]

It is shown in Fig. A.4.2. Where

$$V_{IH} = [R_2 / (R_2 + R_1 \parallel R_3)]\, V_{cc} \quad (9)$$

and

$$V_{IL} = [(R_2 \parallel R_3) / (R_1 + R_2 \parallel R_3)]\, V_{cc} \quad (10)$$

If $R_1 = R_2 = R_3/2$

Above, $R_2 \parallel R_3$ means : Resistors R_2 and R_3 are connected in parallel.

then,

$$V_{IH} = 3\, V_{cc}/5\ ;\ V_{IL} = 2\, V_{cc}/5;$$

and $V_{OH} = +V_{cc}^{*} = +5V : V_{OL} = 0$

The equations for T_1 and T_2 are obtained by substitution of V_{IH}, V_{IL}, V_{OH} and V_{OL} in equations (1) and (2).

$$T_1 = RC \ln (3/2) \simeq 0.405\, RC$$

and $T_2 = RC \ln (3/2) \simeq 0.405\, RC$

Therefore, $T = T_1 + T_2 \simeq 0.81\, RC$

(iii) IC 555 Timer Oscillator

The circuit of the 555 Timer Oscillator is shown in Fig. A. 4.3, where

$T_1 \simeq 0.7\,(R_1 + R_2)\, C$

and $T_2 \simeq 0.7\, R_2 C$

then $T = 0.7\,(R_1 + 2R_2)\, C$

(iv) Oscillator Using Schmitt Trigger *IC*

Fig. A. 4.4 shows a oscillator using *IC* schmitt trigger,

where $V_{OH} = 3.7V\ ;\ V_{OL} = 0.2V$

$V_{IH} = 1.65V\ ;\ V_{IL} = 0.85V$

The equations for T_1 and T_2 are obtained by substituting the following values in equations (1) and (2). Therefore,

$$T_1 = RC \log_e [(3.7 - 0.85) / (3.7 - 1.65)]$$
$$= RC \ln (1.39)$$
$$\simeq 0.33\, RC$$

and $T_2 = RC \ln [(1.65 - 0.2) / (0.85 - 0.2)]$
$= RC \ln (2.23)$
$\simeq 0.8\, RC$

(v) Astable Voltage Controlled Oscillator (VCO)

The astable VCO is shown in Fig. A. 4.5. Where

f_o (frequency of the output pulses) $= K_1 + K_2\, V_{FC}$

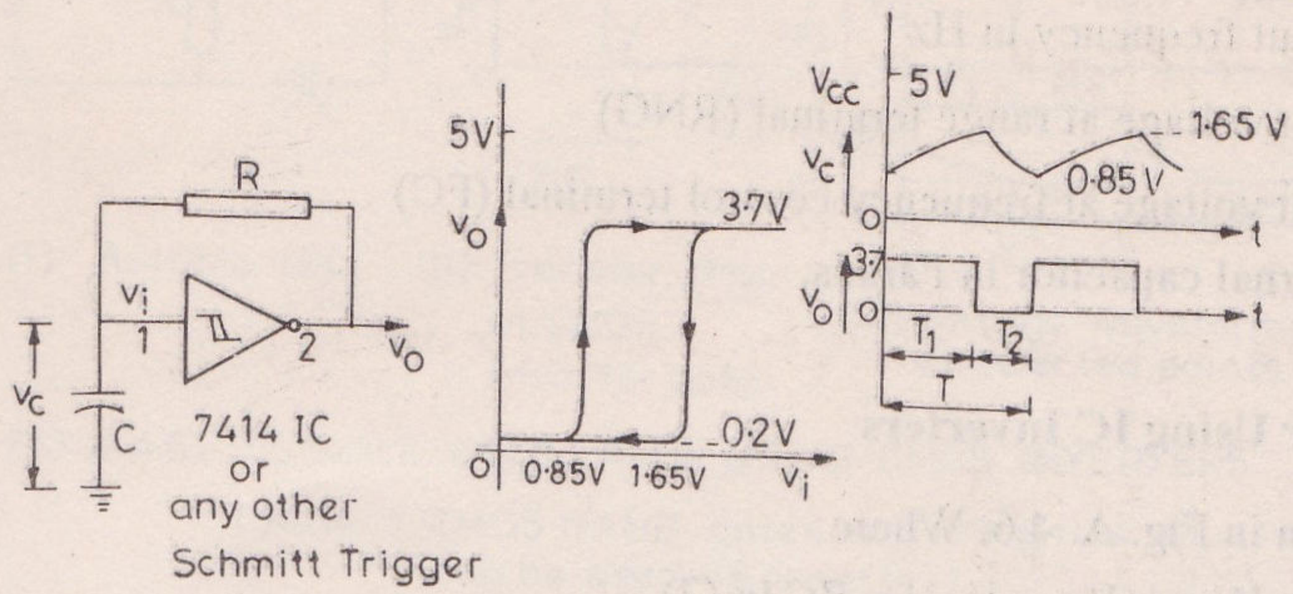
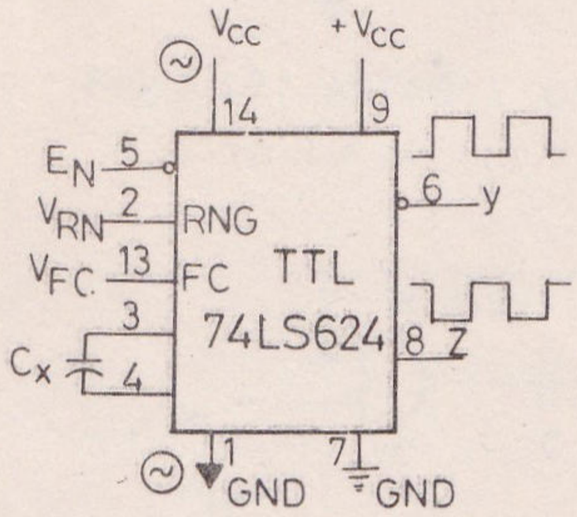


FIG. A.4·4: ASTABLE OSCILLATOR USING SCHMITT TRIGGER



E_N (Enable)	outputs	
	y	Z
1 (High)	1	0
0 (Low)	Enable (0 & 1)	

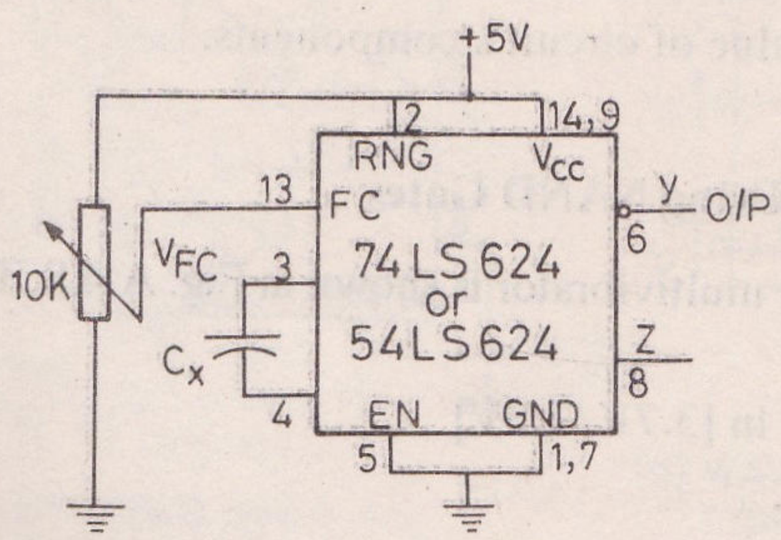
'E_N' TERMINAL CAN BE USED FOR SYNCHRONISATION.

Pins No. 10, 11 & 12 → NC

$V_{CC} = \circledcirc V_{CC} = 5V$ when $V_{RN} = V_{FC} = 2{\cdot}5\,V$

$$f \simeq \frac{5 \times 10^{-4}}{C_x}$$

(a) LOGIC OF 74LS624 VCO



(b) CIRCUIT

FIG. A.4·5: ASTABLE VCO USING A TTL 74LS624 IC

(for a fixed C_x, K_1 and K_2 are constant)

$$f_o \alpha [V_{FC} / (V_{RN} \cdot C_x)]$$

where f_o : output frequency in Hz

V_{RN} : input voltage at range terminal (RNG)

V_{FC} : input voltage at frequency control terminal (FC)

C_x : external capacitor in Farads.

(vi) Oscillator Using IC Inverters

It is shown in Fig. A. 4.6. Where

$$T_1 = RC \ln [V_{cc} / (V_{cc} - V_{th})] = RC \ln (2)$$

and $$T_2 = RC \ln [V_{cc} / V_{th}] = RC \ln (2)$$

because generally CMOS have V_{th} (threshold voltage) $\simeq V_{cc}/2$

$$T = 2RC \text{ in } (2) \simeq 1.4\, RC$$

(vii) Oscillator Using NAND Gates

It is shown in Fig. A.4.7. Where

$$T_1 = T_2 = RC \ln (V_{OH} / V_{th})$$

but $$V_{th} \simeq V_{OH}/2$$

So $$T_1 = T_2 = RC \ln (2)$$

or $$T = 2RC \ln (2) \simeq 1.4\, RC$$

2. MONOSTABLE (ONE-SHOT) MULTIVIBRATOR

The monostable multivibrator is stable in one state (0 or 1) and unstable in the other state which is generated by a triggering pulse. One rectangular pulse is received at the output terminal of the monostable multivibrator for each positive or negative edge of the triggering pulse. So the monostable multivibrator is also called a *one-shot multivibrator.* The width (or period) of the output pulse can be varied by varying the value of circuit's components.

(i) Monostable Multivibrator Using NAND Gates

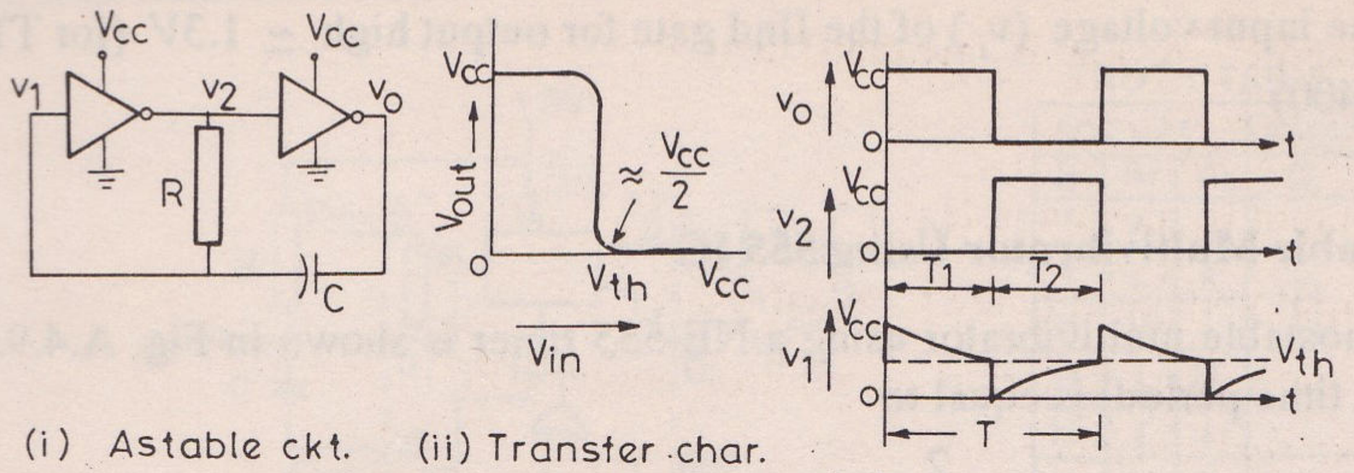
The NAND gates monostable multivibrator is shown in Fig. A.4.8. The generated pulse width is :

$$t_l = RC \ln [V_{HL} / V_{LH}] \simeq RC \ln [3.7V / 1.3V]$$

$$= 1.05\, RC$$

where

V_{HL} : The input voltage (v_i) of the IInd gate for output low $\simeq 3.7V$ (for TTL-NAND gate 7400)



(i) Astable ckt. of CMOS Inverter Gate

(ii) Transfer char.

(iii) Voltage Waveforms at selected points

FIG.A.4.6: ASTABLE OSCILLATOR USING CMOS INVERTERS

(Note : CMOS NAND gates or NOR gates also can be used as inverter)

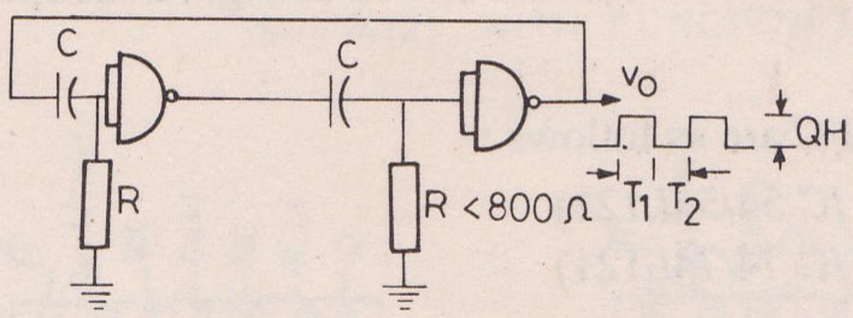


FIG.A.4.7: ASTABLE OSCILLATOR USING TTL NAND GATES

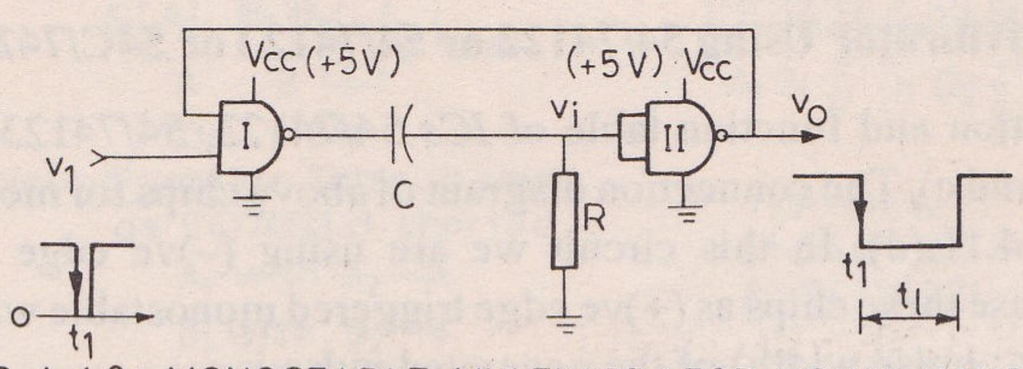
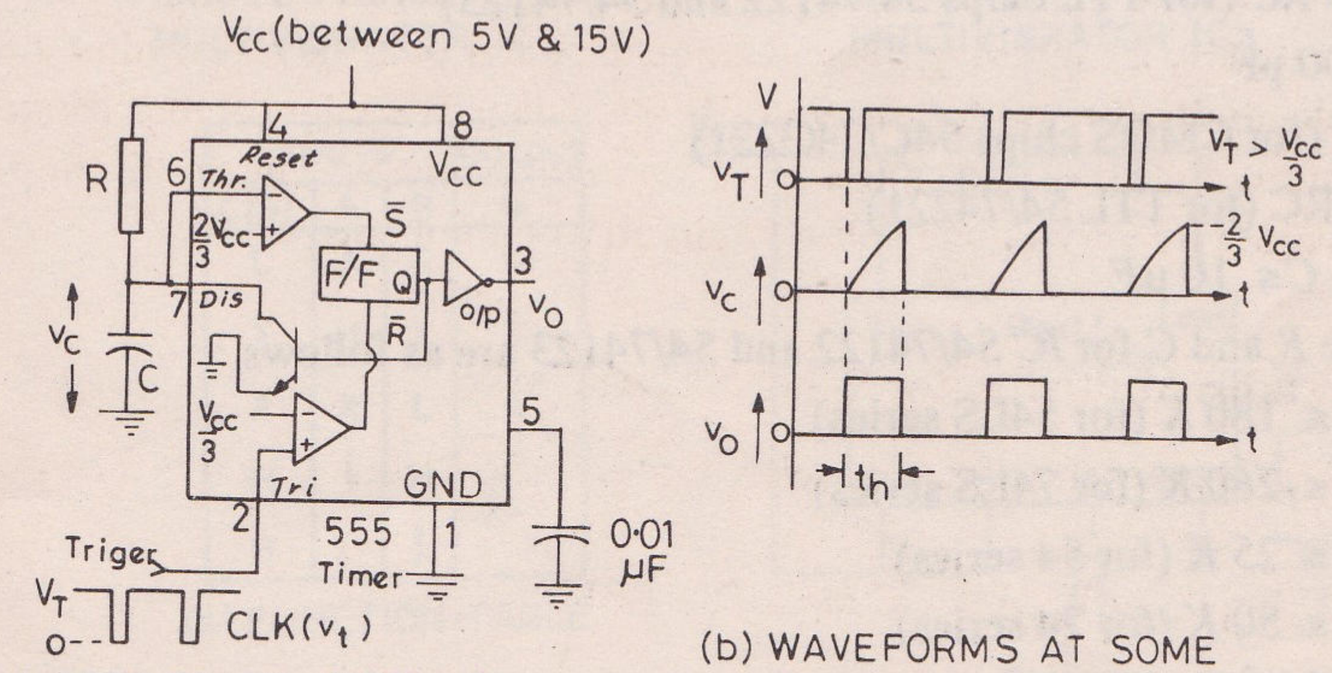


FIG.A.4.8: MONOSTABLE MULTIVIBRATOR USING NAND GATES



(a) 555 TIMER USED AS MONOSTABLE CIRCUIT

(b) WAVEFORMS AT SOME POINTS OF CIRCUIT

FIG.A.4.9 ONE-SHOT (MONOSTABLE) MULTIVIBRATOR USING A 555 TIMER

and V_{LH} : The input voltage (v_i) of the IInd gate for output high $\simeq 1.3V$ (for TTL-NAND gate 7400)

(ii) Monostable Multivibrator Using 555 IC

The monostable multivibrator using a NE-555 timer is shown in Fig. A.4.9. The generated pulse width (t_h; time period) is equal to

$$t_h = RC \ln [(V_{cc} - 0) / (V_{cc} - \frac{2}{3} V_{cc})]$$

or $\simeq 1.1\ RC$

(iii) Monostable Multivibrator Using a 54/74121 IC

Its circuit diagram and function table are shown in Fig. A. 4.10, where :

$t_h = 0.7\ RC$

The limits of the R and C are as follows :

$1.4K \leq R \leq 30\ K$ (for *IC* 54/54*L*121)

$1.4K \leq R \leq 40\ K$ (for *IC* 74/74*L*121)

and $0 \leq C_{ext.} \leq 1000\ \mu F$

Therefore, 't_h' varies between 30 *ns* to 28 sec.

(iv) Monostable Multivibrator Using 54/74122 or 54/74123 or 54C/74221 IC

The pin configuration and function table of *ICs* 54/74122, 54/74123 and 54*C*/74*C*221 are shown in Fig. A. 4.11(a, b and c). The connection diagram of above chips for monostable multivibrator is also shown in Fig. A.4.11.(d). In this circuit we are using (–)ve edge triggered monostable multivibrator, and we can use these chips as (+)ve edge triggered monostable with the help of function table. The time duration (t_h; pulse width) of the generated pulse is :

$t_h \simeq 0.45\ RC$ (for TTL chips 54/74122 and 54/74123)

when $C > 1000$ pF

$T_h \simeq RC$ (for CMOS chips 54*C*/74*C*221)

and $t_h \simeq 0.7$ RC (for TTL 54/74221)

when 10 pF $\leq C \leq 10\ \mu F$

The limits of the R and C for *IC* 54/74122 and 54/74123 are as follows :

$5K \leq R \leq 180\ K$ (for 54LS series)

$5K \leq R \leq 260\ K$ (for 74LS series)

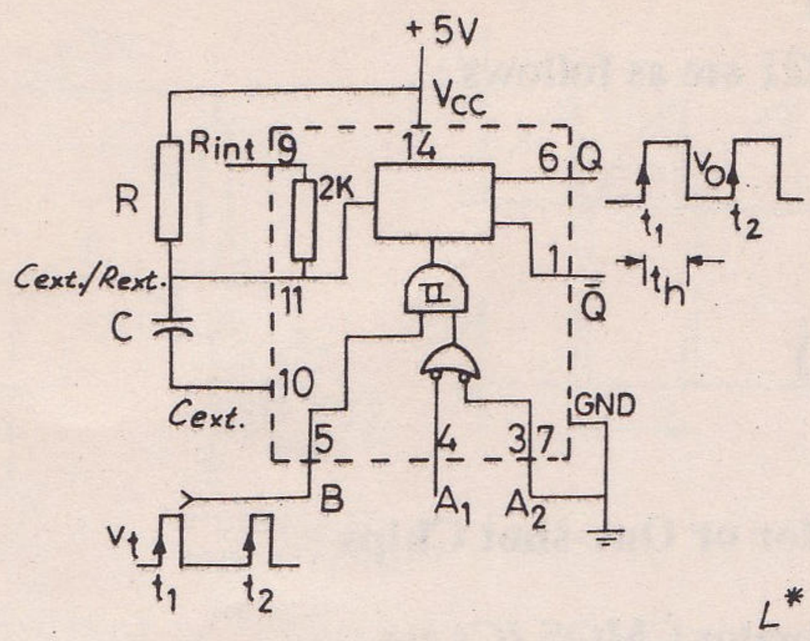
$5K \leq R \leq 25\ K$ (for 54 series)

$5K \leq R \leq 50\ K$ (for 74 series)

$C \rightarrow$ has no limit

The limits of the R and C for *IC* 54*C*/74*C*221 are as follows :

$R \leq 80\ V_{cc}\ (\Omega)$



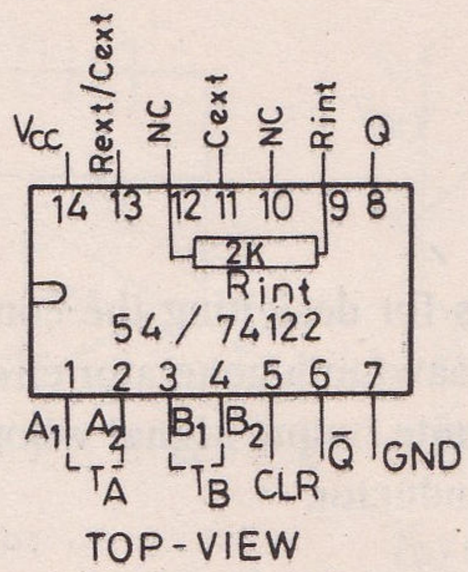
(a) MONOSTABLE CIRCUIT

TRUTH TABLE

Inputs			Outputs
B	A_1	A_2	Q
↑	X	L	
↑	L	X	
H	H	↓	
H	↓	H	
H	↓	↓	
H	L	X	L
H	X	L	L*
L	X	X	

L* : It state is validated after complete any output pulse started before.

FIG. A.4·10 : MONOSTABLE MULTIVIBRATOR USING AN IC 54/74121 WITH FUNCTION TABLE



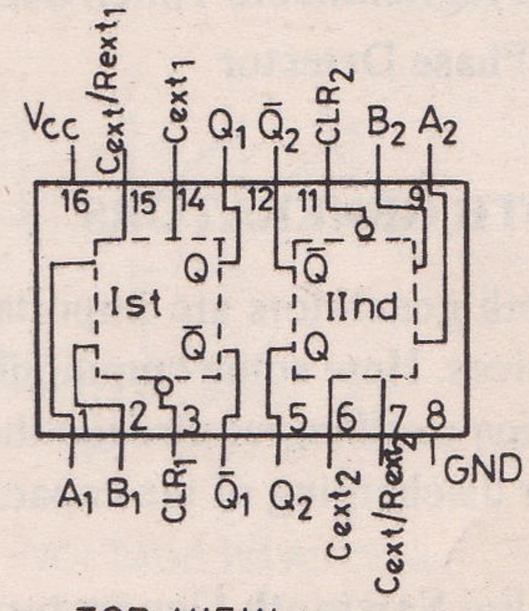
TOP-VIEW

*Note: Function Table in same as 54/74123; if shorted

A_1 with A_2 → A

B_1 with B_2 → B

(a) PIN CONFIGURATION OF SINGLE MONOSTABLE MULTIVIBRATOR IC



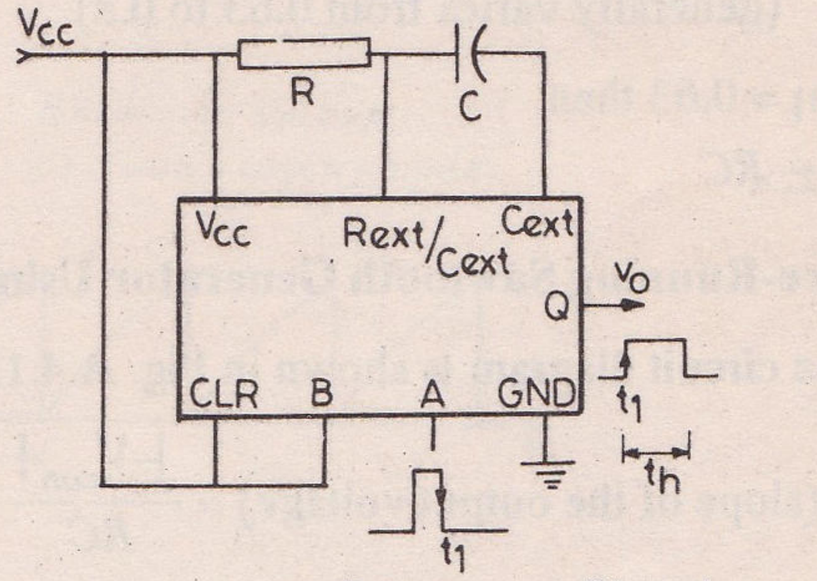
TOP-VIEW
Of 54/74123, 54C/74C221 & 54/74221

(b) PIN CONFIGURATION OF DUAL MONOSTABLE MULTIVIBRATOR ICs

Inputs			Output
CLR	A	B	Q
L	X	X	L
X	H	X	L*
X	X	L	L*
H	↓	H	
H	L	↑	

(c) FUNCTION-TABLE

L*: Same as in Fig. A.4·10



Triggering Signal

Where: R = Rext / Rint / (Rext + Rint)

(d) CIRCUIT DIAGRAM

FIG. A.4·11 : MONOSTABLE MULTIVIBRATOR USING ICs 54/74122 OR 54/74123 OR 54C/74C221 OR 54/74221

Max. duty cycle = R / (R+1000)

The limits of the R and C for *IC* 54/74221 are as follows :

$2K \leq R \leq 30K$ (for 54221)

$2K \leq R \leq 70K$ (for 54 LS 221)

$2K \leq R \leq 40K$ (for 74221)

$2K \leq R \leq 100K$ (for 74 LS 221)

and $0 \leq C \leq 1000\ \mu F$

(v) Other Monostable Multivibrator or One-shot Chips

Some other monostable multivibrator CMOS *ICs* are :

CD 4047 : Low Power Monostable/Astable Multivibrator

CD 4528 : Dual Monostable Multivibrator

CD 4538 : Dual Monostable Multivibrator

CD 4541 : Programmable Timer/Oscillator

54C932 : Phase Detector

3. SAWTOOTH GENERATORS

The sawtooth generators are important tools for designing the control circuit of the power semiconductor devices. Here some commonly used sawtooth generator circuits are given. These are also called *relaxation oscillators*; circuits that generate output signal whose frequency depends on the charging and/or discharging of the capacitor or inductor.

(i) Free-Running Sawtooth Generator Using a Unijunction Transistor (UJT)

It is shown in Fig. A.4.12. Where :

$T = RC \ln [1 / (1-\eta)]$

η = Intrinsic stand-off ratio of the UJT
(generally varies from 0.63 to 0.8)

If $\eta = 0.63$ then

$T \simeq RC$

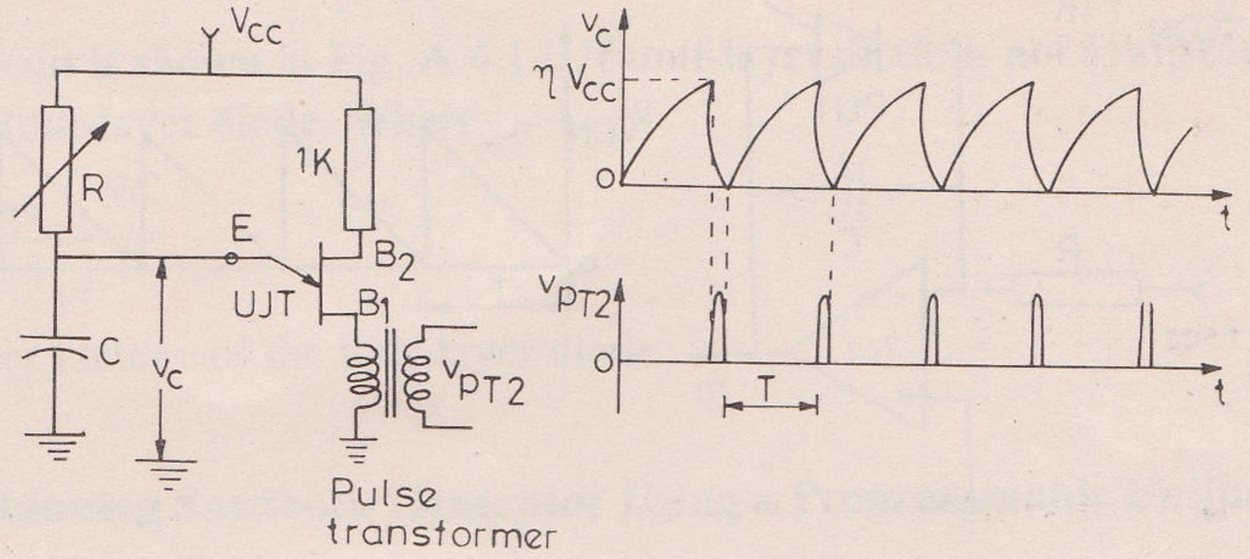
(ii) Free-Running Sawtooth Generator Using a Four-Layer Diode and a OP-AMP. (VCO)

The circuit diagram is shown in Fig. A.4.13. Where :

$$\text{m (slope of the output voltage)} = \frac{|-V_{con}|}{RC} = \frac{V_{BO}}{T}$$

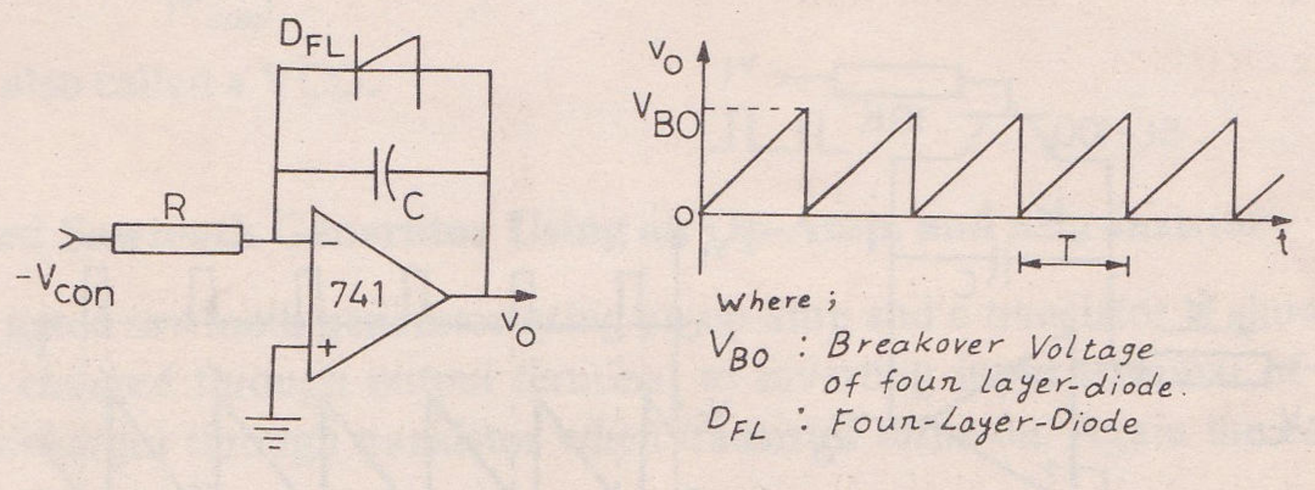
or $$T \simeq \frac{V_{BO} \cdot RC}{|V_{con}|}$$

It is also called voltage-controlled oscillator (VCO).



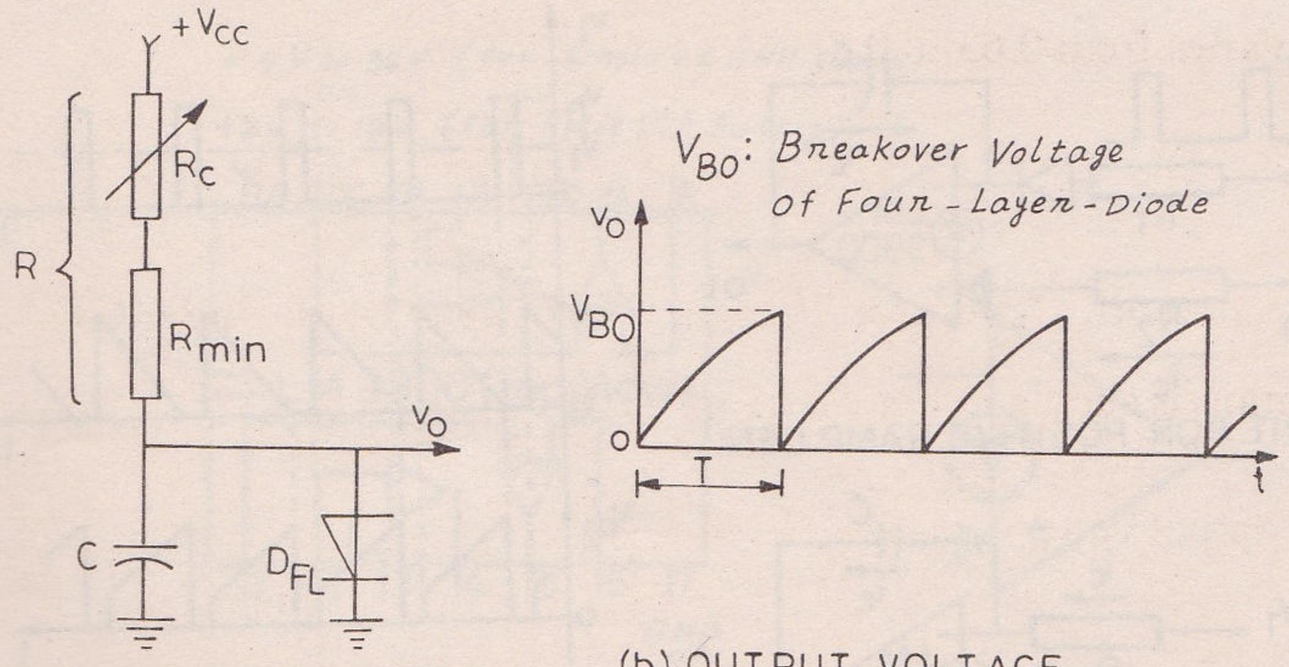
(a) CIRCUIT (b) WAVEFORMS

FIG. A.4.12: FREE RUNNING SAWTOOTH GENERATOR USING A UJT



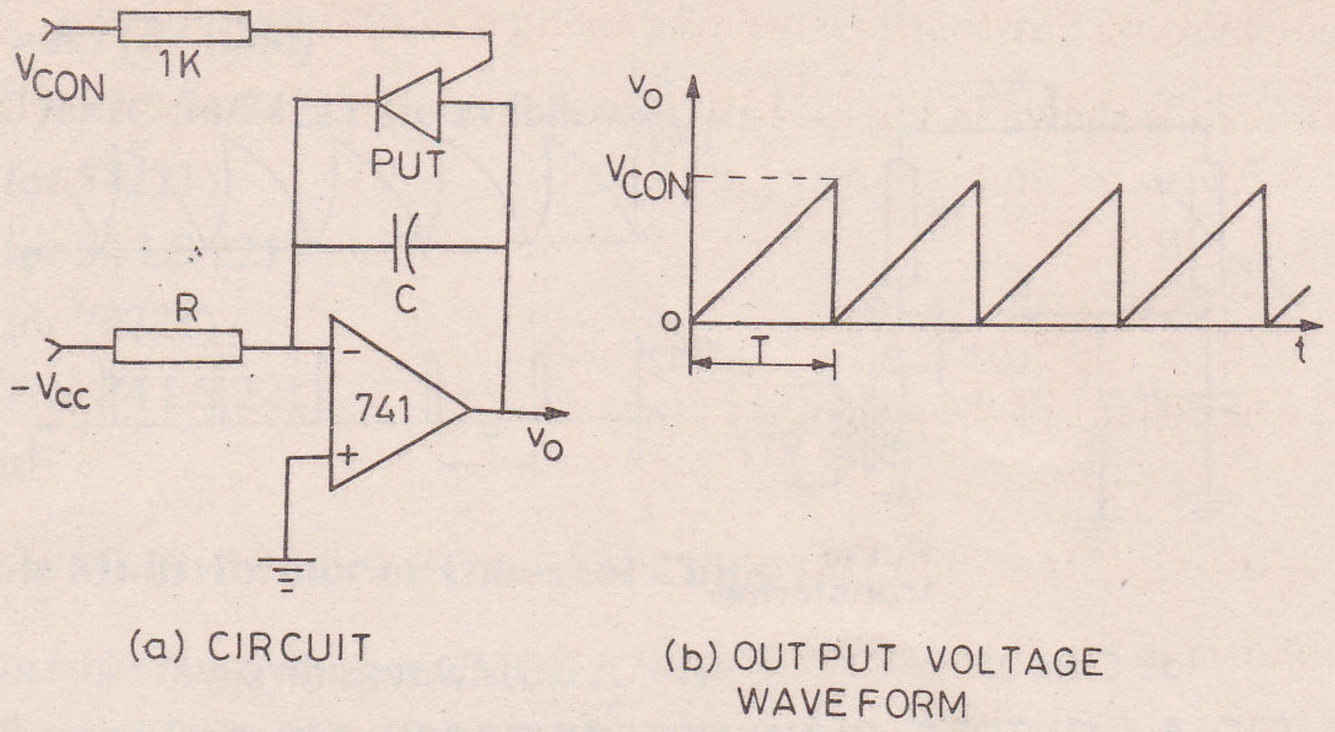
(a) CIRCUIT (b) OUTPUT-VOLTAGE WAVEFORM

FIG. A.4.13: FREE-RUNNING SAWTOOTH GENERATOR USING A FOUR LAYER DIODE AND A OP-AMP.



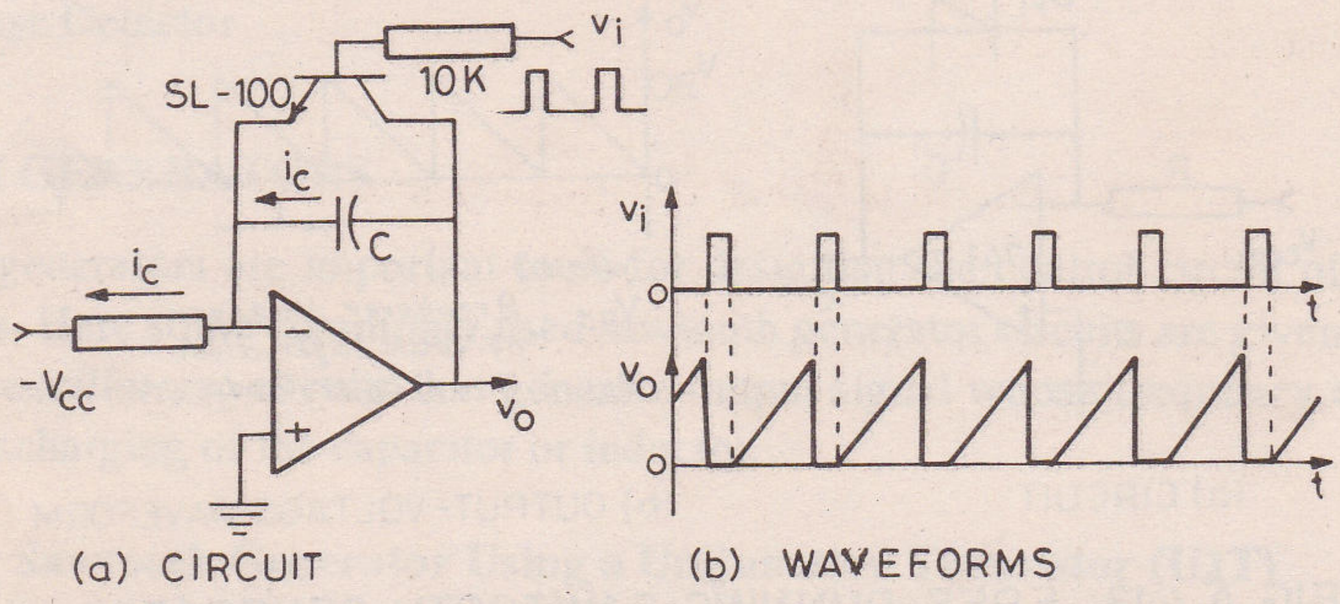
(c) CIRCUIT (b) OUTPUT VOLTAGE WAVEFORM

FIG. A.4.14: FREE-RUNNING SAWTOOTH GENERATOR USING A FOUR LAYER-DIODE



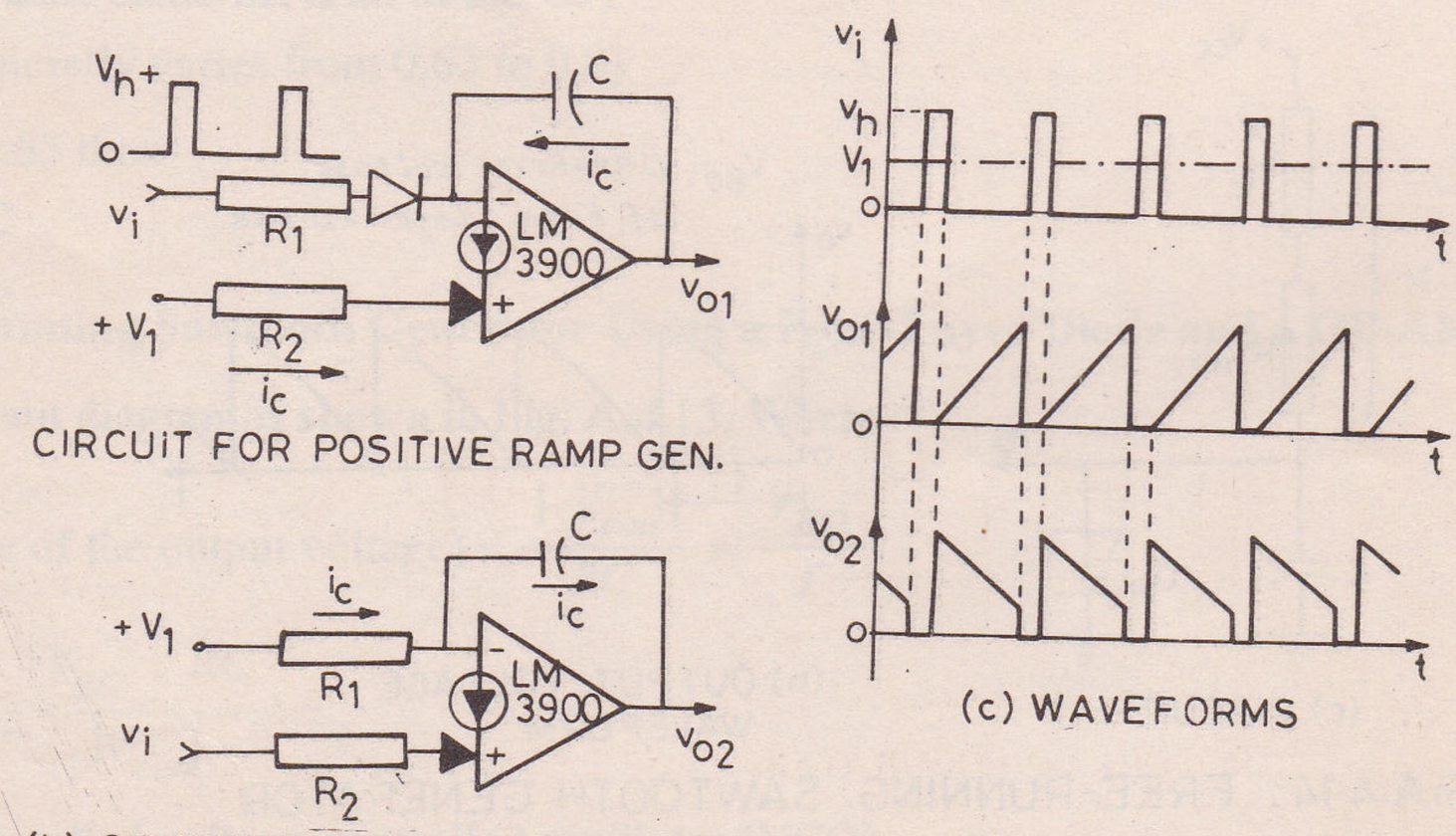
(a) CIRCUIT (b) OUTPUT VOLTAGE WAVEFORM

FIG. A.4.15: FREE-RUNNING SAWTOOTH GENERATOR USING A PUT AND A OP-AMP.



(a) CIRCUIT (b) WAVEFORMS

FIG. A.4.16: GATED (Triggered) SAWTOOTH GENERATOR USING AN OP-AMP AND A TRANSISTOR



CIRCUIT FOR POSITIVE RAMP GEN.

(b) CIRCUIT FOR NEGATIVE RAMP GENERATOR

(c) WAVEFORMS

FIG. A.4.17: GATED SAWTOOTH GENERATOR USING OP-AMP.

(iii) Free-Running Sawtooth Generator Using a Four-Layer Diode

The circuit is shown in Fig. A.4.14. If four-layer diode is not available, the diac can be used at the place of four-layer diode. Where :

$$T \simeq \frac{V_{BO} \cdot RC}{V_{cc}}$$

V_{BO} : Breakover voltage of the four-layer diode.

(iv) Free-Running Sawtooth Generator Using a Programmable Unijunction Transistor (PUT)

It is shown in Fig. A.4.15. Where :

$$m \text{ (slope)} = \frac{|V_{con}|}{RC} = \frac{V_{con}}{T}$$

or $$T = \frac{V_{con} \cdot RC}{|V_{con}|}$$

It is also called a VCO.

(v) Gated Sawtooth Generator Using an Op-Amp. and a Transistor

The gated sawtooth generator using an op-amp and a transistor is shown in Fig. A.4.16. The capacitor is charged through output terminal to inverting input terminal of the op-amp. And the capacitor discharges through transistor when transistor turns-on. Again the capacitor charges when the transistor turns-off.

(vi) Gated Sawtooth Generator Using a Current-Differencing Op-Amp

The positive ramp gated sawtooth generator and the negative ramp gated sawtooth generator are shown in Fig. A.4.17(a) and (b) respectively. The op-amp LM3900 is used in these circuits. The pins configuration of op-amp LM 3900 is shown in Fig. A.4.18.

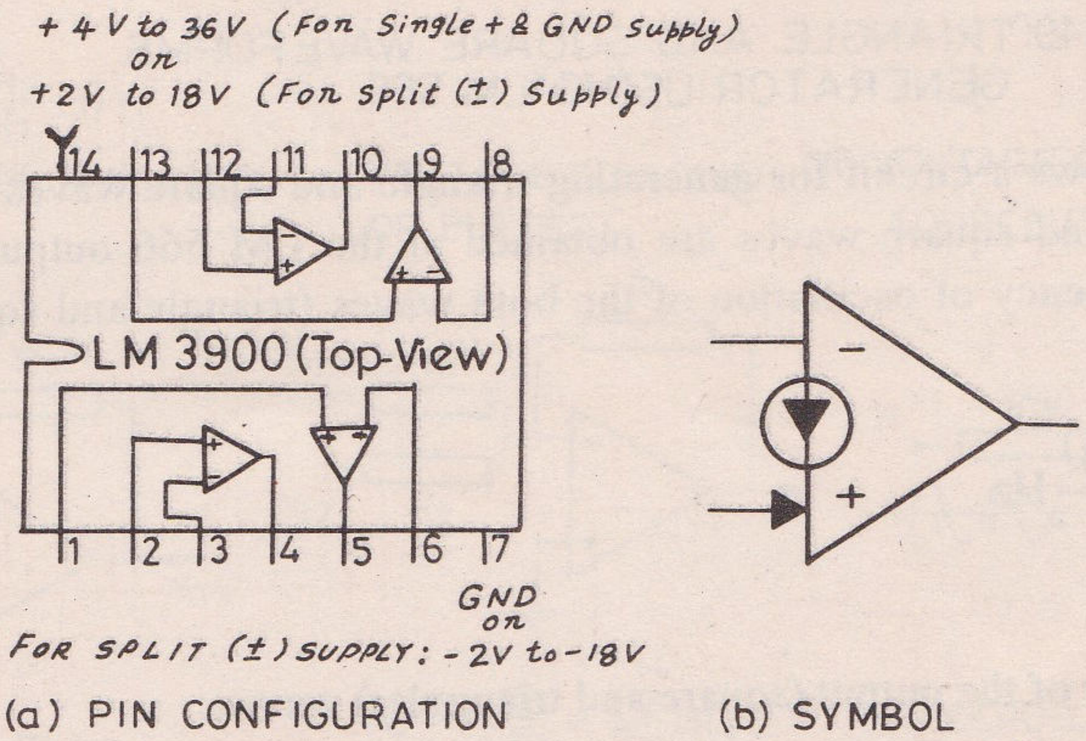

+4V to 36V (For Single + & GND Supply)
or
+2V to 18V (For Split (±) Supply)
14 13 12 11 10 9 8
LM 3900 (Top-View)
1 2 3 4 5 6 7
GND
or
For Split (±) Supply: -2V to -18V
(a) PIN CONFIGURATION
(b) SYMBOL

FIG. A.4.18: PIN CONFIGURATION AND SYMBOL OF OP-AMP LM 3900 ("NORTON" AMPLIFIER)

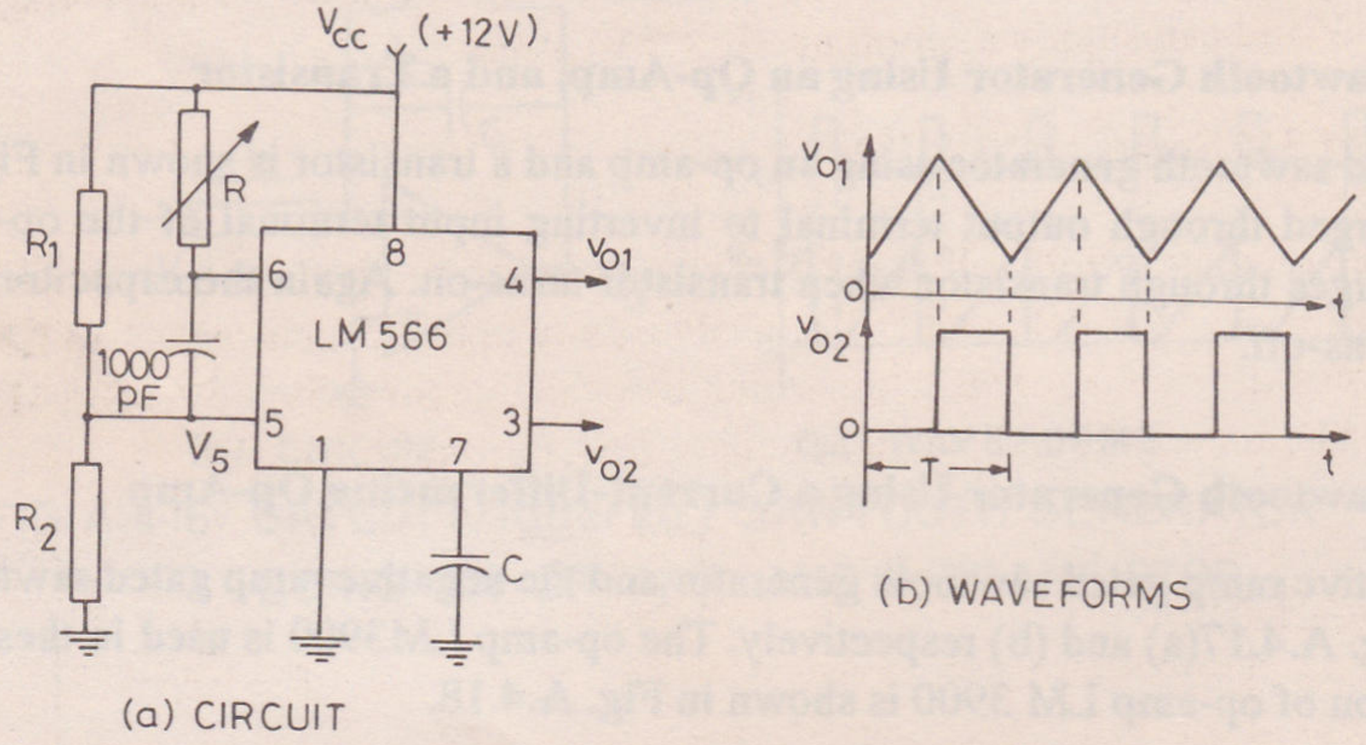
Op-Amp LM3900 (Quad)

Four op-amps have been fabricated on a single chip of 14 pin. It can be used with a single power supply voltage range of $+4V_{DC}$ to $+36V_{DC}$. It can also be used with the split power supply voltage range of $\pm 2V_{DC}$ to $\pm 18V_{DC}$. It is also called "NORTON Amplifier". The performance characteristics of each operational-amplifier of LM 3900 are listed below :

Four op-amp in a package and a Current Mirror to achieve a non-inverting input terminal.

Power-Supply (V_{cc})	:	$+4V$ to $36\ V$ or $\pm 2V$ to $18 \pm V$
Split power supply $[V_{cc} - 0 - (-V_{cc})]$	:	$\pm 2V$ to $18 \pm V$
Bias current drain per op-amp.	:	1.3 mA
Input resistance	:	1 MΩ
Output resistance	:	8 KΩ
Input bias current	:	30 nA
Unity-gain frequency	:	2.5 MHz
Slew rate	:	$0.5\ V/\mu S$

(vii) Triangle and Square Waveforms Generator Using an IC LM 566



(a) CIRCUIT (b) WAVEFORMS

FIG. A.4.19: TRIANGLE AND SQUARE WAVEFORMS GENERATOR USING LM 566

Fig. A.4.19 shows a circuit for generating triangle and square waves using an IC LM 566 (VCO). The triangle and square waves are obtained at the LM 566 outputs pins No. 4 and 3, respectively. The frequency of oscillation of the both waves (triangle and square) is given by the following equation :

$$f = \frac{2(V_{cc}^{+} - V_5)}{RCV_{cc}^{+}} \text{Hz}$$

where,

f : Frequency of the output (square and triangular) waves

V_{cc} : Supply voltage = +12 V

V_5 : Applied voltage at Pin No. 5 of LM 566.

According to the circuit of Fig. A.4.19 :

$$V_5 = \frac{V_{cc} \cdot R_2}{R_2 + R_1} .$$

4. APPLICATIONS OF OPERATIONAL AMPLIFIER

Some applications of the op-amps are shown in Fig. A.4.20. In differential amplifier shown in Fig. A.4.20(vii), for adjusting Common-Mode Rejection Ratio (CMRR); feed same voltage to both the inputs (inverting and non-inverting) of op-amp and adjust R_4 Pot for getting zero output voltage.

5. SOME VOLTAGE REGULATOR CIRCUITS

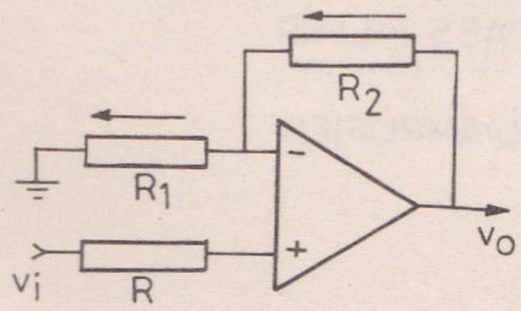
Some Voltage Regulator circuits are shown in Fig. A.4.21. Some important characteristics of some Voltage Regulators are listed below :

(i) LM 117 and LM 317

These voltage regulators are capable of giving regulated output voltage from 1.25V to 37V and can supply approximately 1.5A current.

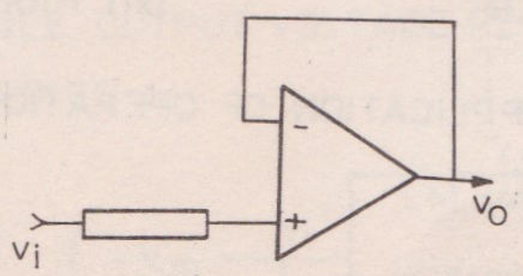
(ii) LM 340 Series and LM 320 Series

The regulators with following output voltage are available in the 340 series : 5V, 6V, 8V, 10V, 12V, 15V, 18V, and 24V and can supply upto 1.5A current. And LM 320 is a group of negative voltage regulators which are available for : –5V, –6V, –8V, –10V, –12V, –15V, –18V, and –24V, and can handle upto 1.5A current.



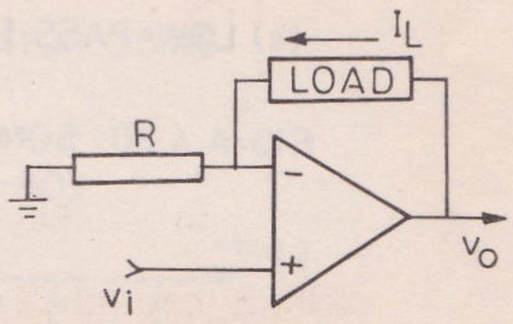
$v_o = (\frac{R_2}{R_1} + 1) v_i$

(i) NON-INVERTING AMPLIFIER



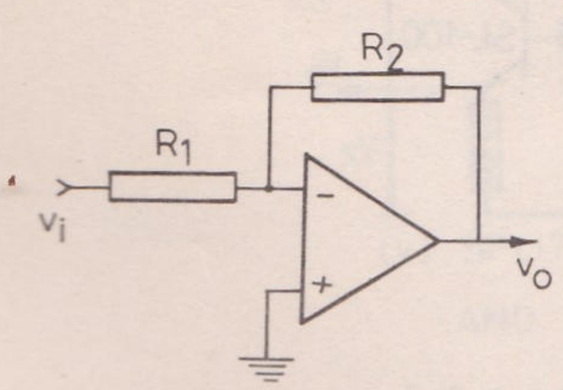
$v_o = v_i$

(ii) VOLTAGE FOLLOWER OR BUFFER



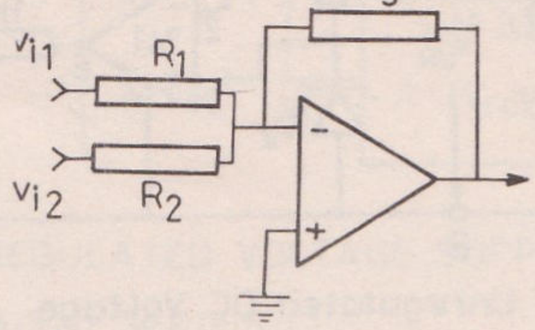
$I_L = v_i / R$

(III) VOLTAGE CONTROLLER CURRENT SOURCE (VCCS)



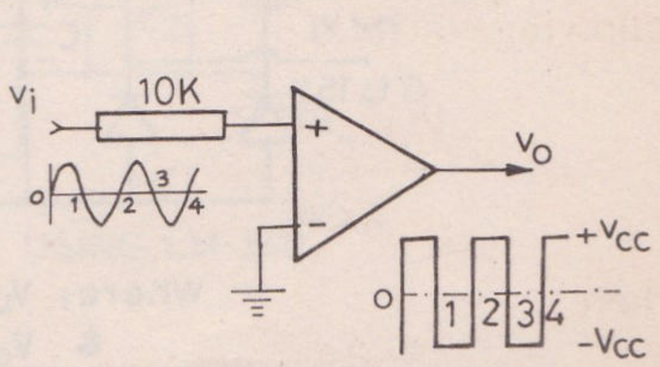
$v_o = -(R_2/R_1) v_i$

(iv) INVERTING AMPLIFIER



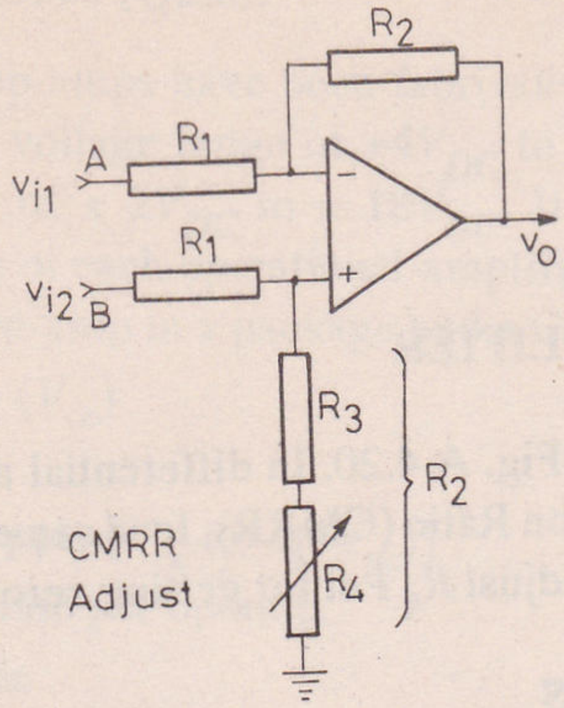
$v_o = -(\frac{v_{i1}}{R_1} + \frac{v_{i2}}{R_2}) R_3$

(v) SUMMING AMPLIFIER



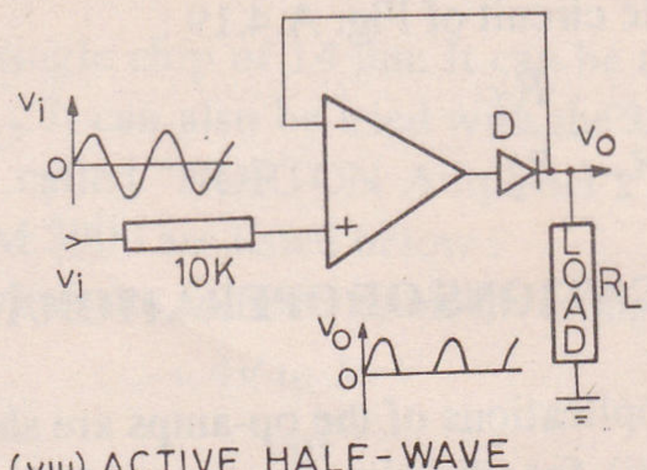
(vi) ZERO-CROSSING DETECTOR (COMPARATOR)

FIG. A.4.20. (CONT.)

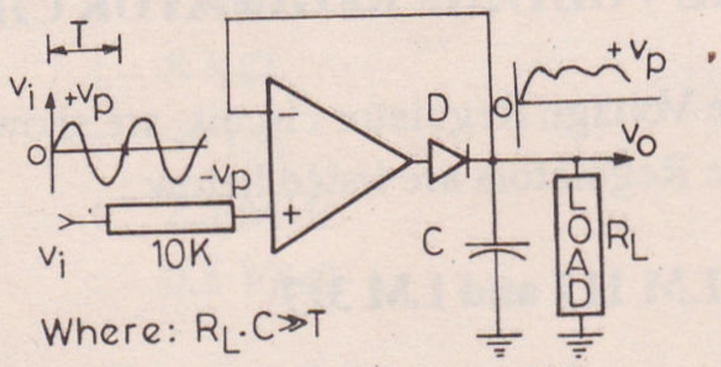


$$v_o = \frac{R_2}{R_1}(v_{i2} - v_{i1})$$

(vii) DIFFERENTIAL AMPLIFIER

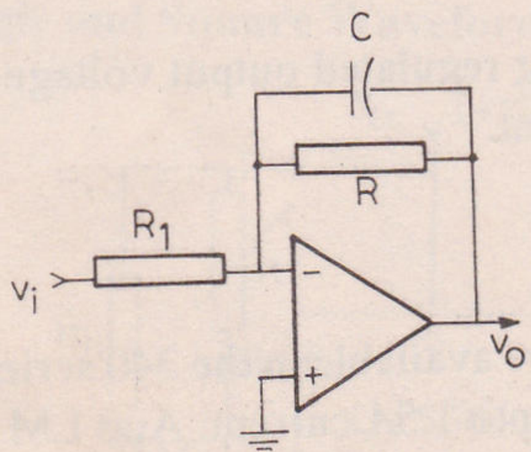


(viii) ACTIVE HALF-WAVE RECTIFIER (It eliminate diode offset voltage)



Where: $R_L \cdot C \gg T$

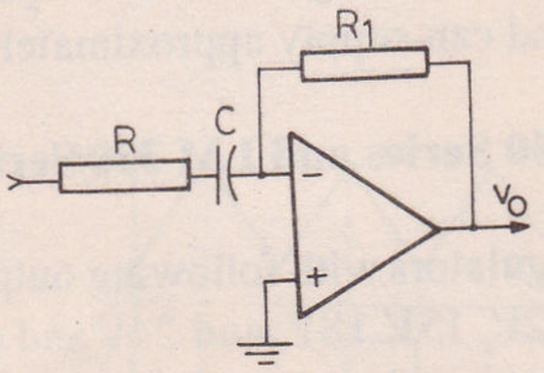
(ix) ACTIVE PEAK DETECTOR



f_p(Pass-freq.)$< f_c$ (cut-off freq.)

$f_c = 1/2\pi RC$

(x) LOW-PASS FILTER

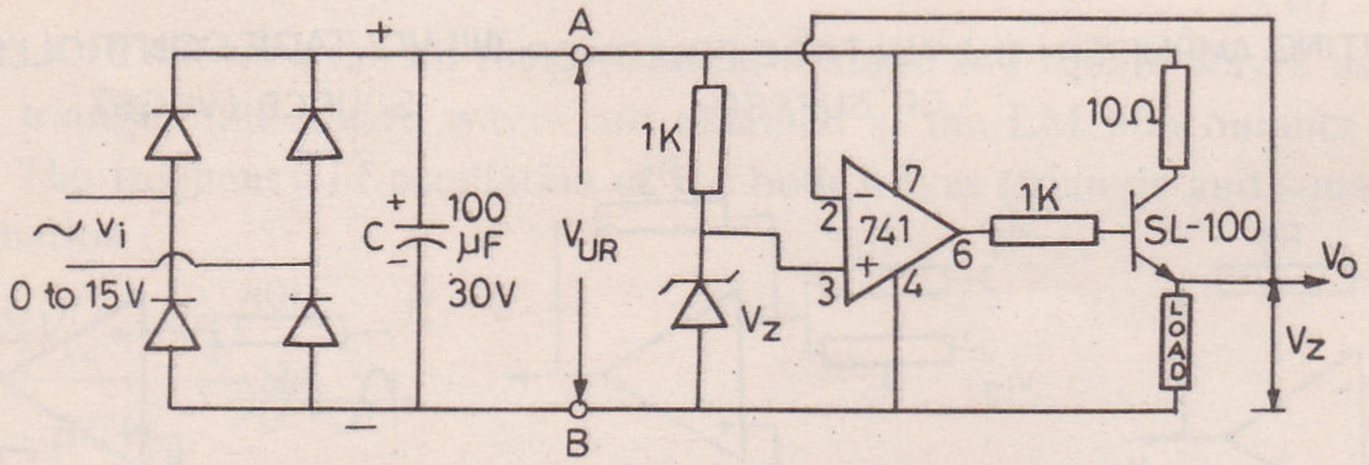


$f_p > f_c$

$f_c = 1/2\pi RC$

(xi) HIGH-PASS FILTER

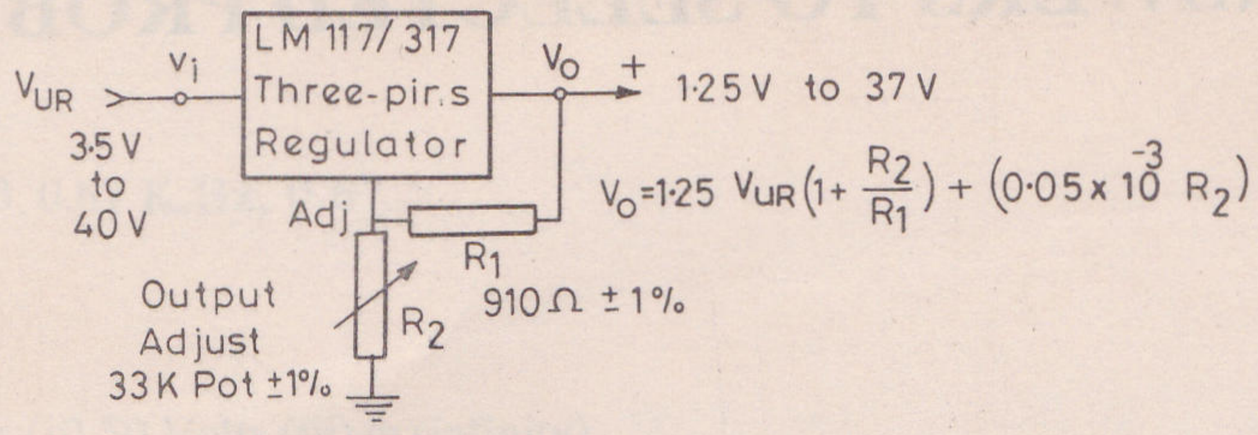
FIG. A.4.20: SOME APPLICATION OF OPERATIONAL AMPLIFIER (OP-AMP.)



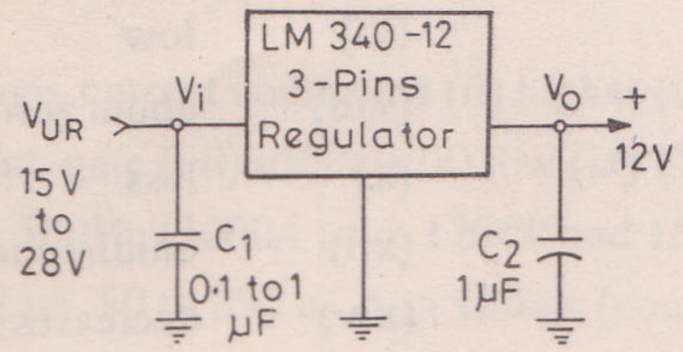
Where; V_{UR}: Unregulated DC Voltage
& V_o : Regulated DC Voltage

(i) AN OP-AMP. VOLTAGE REGULATOR

FIG. A.4.21 (CONT.)



(ii) THREE-TERMINAL VOLTAGE REGULATOR LM 117/LM 317

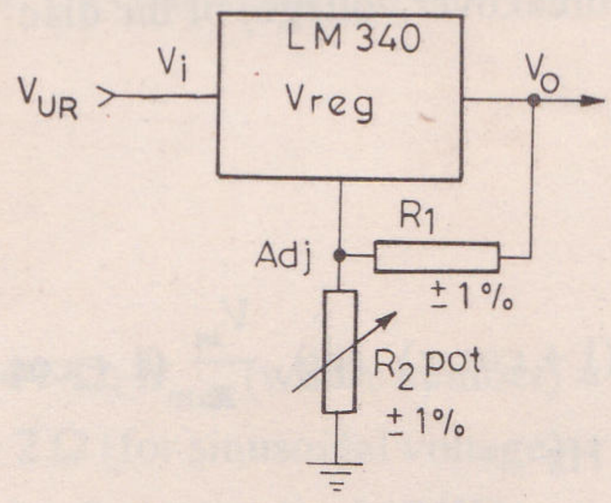


Where:

(1) $V_{UR} \geq (V_o + 3V)$

(2) C_1 & C_2 are connected for bypassing Oscillations produced by the supply

(iii) 12 VOLTS REGULATED VOLTAGE WITH LM 340 SERIES



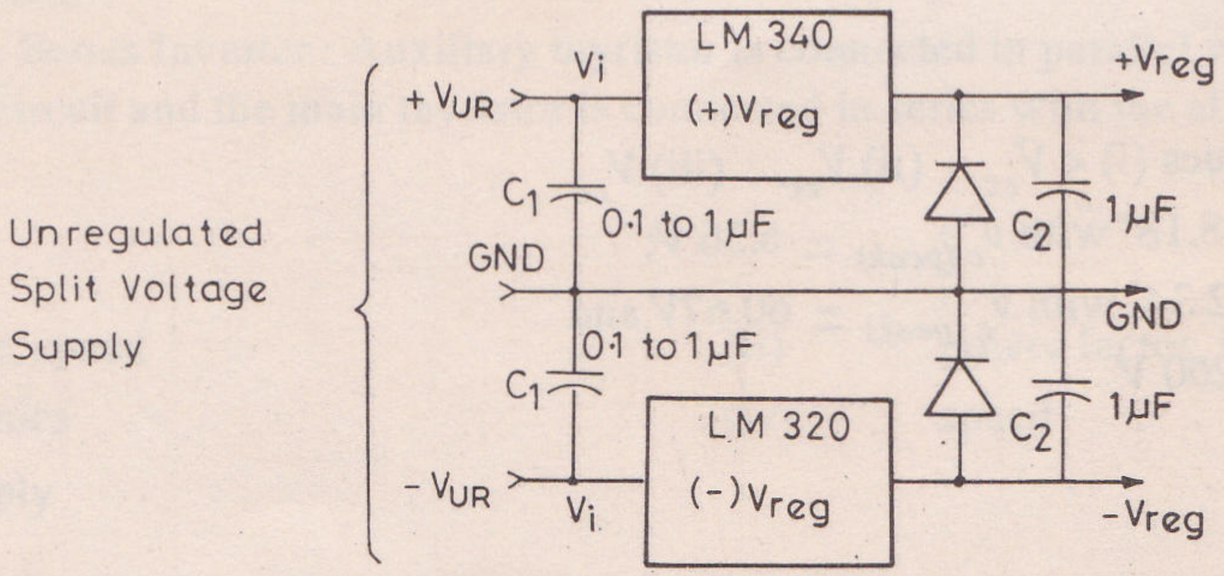
Where:

$V_o \simeq V_{reg} + \left(\frac{V_{reg}}{R_1} + 0{\cdot}0075\right)R_2$

$V_{UR} \geq (V_o + 3V)$

& V_{reg} = 5V, 6V, 8V, 10V, 12V, 15V, 18V or 24V Regulator of LM-340 series

(iv) ADJUSTABLE OUTPUT VOLTAGE REGULATOR USING LM-340 SERIES



(v) SPLIT REGULATED VOLTAGE SUPPLY USING LM-340 AND LM-320 SERIES

FIG. A.4·21: SOME REGULATED VOLTAGE SUPPLIES

ANSWERS TO SELECTED PROBLEMS

Experiment 1

1.1 (i) four, three (ii) SCR
(iii) three, Anode, Cathode, Gate (iv) Anode
(v) very high (vi) low
(vii) high (viii) about zero
(ix) low (x) less
(xi) less (xii) unidirectional, bidirectional
(xiii) holding current (xiv) decreases
(xv) heat sink

1.5 1.2V to 2.6V, 1.2V to 1.8V and $\pm V_{bo}$ (breakover voltage) of the diac

Experiment 2

2.3 : 0.63

2.5 : (i) V_m/π (ii) $2V_m/\pi$ (iii) $\frac{V_m}{2\pi}(1+\cos\alpha)$ (iv) $\frac{V_m}{\pi}(1+\cos\alpha)$

2.6 : $v_{c(peak)} = 7.8V$; $v_{c(av.)} = 3.9V$; $f_c \simeq 190$ Hz

2.7 : (i) about 0 to 90° (ii) about 0 to 180° (iii) ηV_{bb} (η : instrinsic stand-off ratio; V_{bb} : applied voltage)
(iv) resistance value of pot R_1

Experiment 3

3.2 : peak values (i) < V_{cc} (ii) V_{cc} (iii) V_{cc}

3.3 : $\phi_{max} = 88.18°$ with $v_{c\,(peak)} \simeq 6.36\ V$;
$\phi_{min} = 72.34°$ with $v_{c\,(peak)} \simeq 60.67V$ and
$e_{peak} \simeq 200\ V$

Experiment 4

4.1 : (i) antiparallel (ii) any (iii) triac (iv) bidirectional (v) positive (vi) four (vii) small positive

4.2 : $\frac{V_m}{\sqrt{2\pi}}\left[\pi - \alpha + \frac{1}{2}\text{Sin } 2\ \alpha\right]^{1/2}$

Experiment 8

8.4 : 6.67*V*, 33.33, 0.67 K.Hz, 0.67

Experiment 9

9.4 (i) 100 Volts (ii) 50 Volts (iii) ∞ (infinity)

Experiment 10

10.1 (i) Voltage, current controlled (ii) higher (iii) higher (iv) higher (v) very low (vi) negative current, gate (vii) *dV/dt* (viii) low (ix) (750*A*, 120*V* and 60*A*, 1000*V*), (72*A*, 100*V* and 26*A*, 500*V*), (3000*A* (*av*), 1200*V* and 1500*A*, 4000*V*) and (2000*A*, 2500*V*)

(x) 1 to 2 μs, 50 to 250 ns, 5 to 100 μs (converter grade 50 to 100 μs and inverter grade 5 to 25 μs), about 5 μs

(xi) thyristor, GTO thyristor

10.3 3.5 Volts

Experiment 11

11.2 0.126 μF

11.5 (i) $R < 8.944\ \Omega$; R_{max} (whole number) = 8 Ω;
Let R = 2 Ω (for sinusoidal voltage)
f_r (Ringing frequency) ≃ 347 KHz

(ii) $0.207\ A < 89.7°$ (iii) 90.04 *V*

(iv) 0.01 *V* (v) 3.933×10^{-4} W

(vi) 23.32 KHz

Simple Series Inverter : Auxiliary thyristor is connected in parallel with the L-R-C series circuit and the main thyristor is connected in series with the above circuit.

Experiment 13

13.1 (i) voltage, speed (ii) power factor, load current

(iii) harmonics (iv) speed

(v) dc supply

Experiment 14

14.1 (b) $\frac{V_m}{2\sqrt{\pi}} \left[2\pi - \alpha + \frac{1}{2} \text{Sin } 2\ \alpha\right]^{1/2}$

14.3 (i) 84.8° to 122.6° (ii) 84.8° to 63.6°

Experiment 15

15.5 135.05 *V*, 115.27 *V*, 101.29 *V*, 67.52 *V* and 9.05 *V*

Experiment 16

16.4 (i) 31.24° (ii) 0.816 (iii) 6.78 Ω

16.5 135.05 *V*, 95.49 *V*, 67.52 *V*, 0 *V*, – 46.19 *V*, –116.95 *V*, –134.53 *V*